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Characterization of silicon nanowire transistor

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Abstract

This paper analyses the temperature sensitivity of Silicon Nanowire Transistor (SiNWT) depends on the diameter (D.ch) of channel. In addition, it also investigates the possibility of utilizing SiNWT as a Nano- temperature sensor. The MuGFET simulation tool has been utilized to conduct a comprehensive simulation to evaluate both electrical and temperature characteristics of SiNWT. Current-voltage characteristics with different values of temperature and with a varying diameter of the Nano wire channel (D.ch = 80, 40, 20 and 10 nm), were simulated. Diode operating mode connection of the transistor is suggested for measuring the temperature sensitivity of SiNWT. As simulation results demonstrated, the best temperature sensitivity was occurred at lower temperature with increasing the channel diameter. We also illustrate the impact of varying temperature and channel diameter on electrical characteristics of SiNWT including, Subthreshold Swing (SS), Threshold voltage (V.th), and Drain-induced barrier lowering (DIBL), which were proportionally increased with the operating temperature.

Keywords: *channel diameter, temperature sensitivity, DIBL, SiNWT, SS, V.th*

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1. Introduction

The improvement of new technology is described by its prominence on miniaturization scale to ultra-micro dimensions [1]. That is the main principle of Nano technology which invaded the field of applied science, manufacturing, industrial, military, medical, agricultural and other fields [2, 3]. The most remarkable example for that is in Nano electronics and nanoscience, where the technological progress has come from reductions, downsizing transistors and adding more numbers of transistors per chip [4].

Recently, with the emergence of the Internet of Things (IoT) [5], sensors have become crucial components that can monitoring and continuously tracking various physical stimulus parameters and update information to the Internet [6-9]. Among numerous sensing and monitoring techniques, sensors based on Field Effect Transistors (FETs) have attracted considerable attention from both industry and academia [10-12]. Owing to their unique characteristics such as small size, light weight, low cost, flexibility, fast response, stability, and ability for further downscaling, silicon nanowire field effect transistor (SiNW-FET) can serve as an ideal nanosensor [13-16]. It is the most likely successor to FET-based nanoscale devices [17]. However, as the dimensions (channel length and diameter) of SiNWT channel are shrinking down, electrical and temperature characteristics of SiNWTs should be affected, thereby degrading transistor performance [18]. Although applications of SiNWTs as biological and/or chemical sensors have been extensively explored in the literature, less attention has been devoted to utilize such transistors as temperature sensors [19].

Temperature management is a growing issue, especially in electronics industry, and research is underway to develop the electronic devices network structures. In this case-temperature management- sensors are needed to measure these Nano effects. Temperature has a significant effect on the system performance and the expected life of electronic products especially with the increasingly dense circuitry in a single chip [20, 21]. The remaining part of this paper is organized as follows: the next section presents an overview about SiNWT structure, which followed by the adopted methods for this work. Section 4 discusses simulation results and main findings. Finally, a conclusion is drawn up in section 5.

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2. Silicon Nanowire Transistor Structure

Driving by a wide variety of nanotechnology applications, Nanowire transistors (NWTs) are regarded as one of the key technologies particularly for CMOS scaling beyond the 5-nm node [22-24], this returns to their superior electrostatic integrity with the ability to serve as a respectable nanosors at nano-scale measurements. SiNWTs have excellent flexibility, stretch ability and stability. Hence, there is a real need for deeper insight into SiNWTs structure and operation, and enable the devices' applications. Simulation methods are among the possible options to investigate technological potentials of such nanoscale devices [25, 26]. As depicted in Figure 1, nanowire structure is an extremely thin wire identical material or configuration with a length on a demand of some nanometer s (nm) or more less.it is also a nanostructure, with the span of the demand of a nanometer (10^{-9} meters). Then again, nanowires can be defined as tool that have a thickness or diameter controlled to tens of nanometers or less and an unconfined length. Numerous diverse types of nanowires exist, including metallic (Ni, Pt, Au), semiconducting (Si, InP, GaN), and insulating like SiO_2, T iO_2.

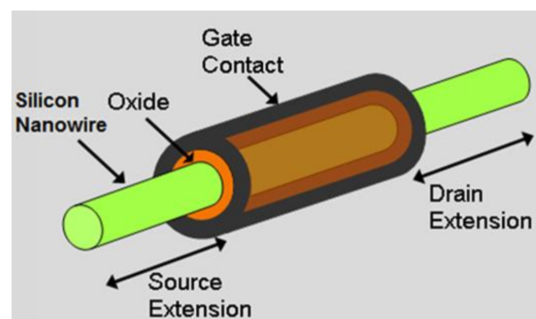

Figure 1. SiNWT structure

Accordingly, design and characterization of SiNWT as a temperature nanosensor for enabling continuous temperature monitoring with superior detection capabilities, high sensitivity, mechanical flexibility, and low-cost fabrication processes, is highly demanded. Therefore, this work proposes designs and characterizes of SiNWT as a temperature nanosensor based on temperature properties. The performance of these new devices, with a wide array of the additional applications, will depend on the characteristics of these devices in Nano-dimensions. A new more powerful electronics device's chips generation with ultra-small transistors could be more trustable in the future after more finds and detection too, by researchers for these tiny structures. The designing of FET in Nano dimensions with new structures is still a technology understudying and improving as well as that requires further innovations.

3. Materials and Methods

This study is simulation-based which used MuGFET [27] simulation to analyze the output characteristics of SiNWT, and it is limited to the considered parameters, including I-V characteristics and channel dimensions of SiNWT. In particular, it investigated the temperature and electrical characteristics of SiNWTs based on varying channel diameter. Simulation tool is the proper option to determine the strong points and weakness of the SiNWT characteristics and to examine the effect of temperature on transfer characteristics such as drain induced barrier lowering (DIBL), sub-threshold swing (SS) and threshold voltage (Vth). The output characteristic curves of the transistor under different conditions and with different parameters are considered. VDD(V). MuGFET can select either PADRE or PROPHET simulation. PROPHET is a partial differential equation profiler for 1, 2, or 3 dimensions. PADRE is a device-oriented simulator for 2D or 3D device with arbitrary geometry. This software provides many powerful characteristic curves for FETs for engineers and for deeply understanding Physics. The MuGFET simulation tool also provides self-consistent solutions to the Poisson and drift-diffusion equation. MuGFET is used to simulate the motion of transport objects in

the calculation of the characteristics for Nanowire. The gaining curve is the difference between the value of drain voltage (VD) with the value of drain current (Id) at a specific voltage gate value (Vg). The curve describes two focal states. The first state is a linear state characterized by low resistance value. The second state is a saturation region, which has a highly resistance value. The assignment curve the transfer is the variable value results for Vg and Id at a fixed value of VD. It observes the impinge of input voltage on the output currents. Several significant factors are getting from this curve such as SS, and DIBL. Transistor performance is regularly calculated by using several fundamental parameters, including VT, SS, DIBL, gm, and ION/IOFF.

4. Results and Discussion

4.1. Temperature Characteristics

In the first simulation scenario, the impact of varying temperature and operation voltages, Vg along with channel diameter have been investigated. The Id-Vg characteristics of Nanowire at a temperature (T = 225, 250, 275, 300, 325, 350, 375, 400, 425 and 450 K) were simulated with different gate base and drain base operating voltages. The considered diameter values were D.ch = 80, 40, 20 and 10 nm. The details simulation parameters are listed in Table 1.

Table 1. Simulation Parameters

Parameters	Value
Channel length (L)	105 nm
Oxide thickness	2.5 nm
Gate Bias initial to final value, Vg	0 to5 volt step 0.25 volt
Drain Bias initial to final value, V_{DD}	0 to5 volt step 0.25 volt
Source and Drain lengths	50 nm
Channel height	30 nm
Channel concentration p -type	10^{16} cm^{-3}
Channel concentration N -type	10^{19} cm^{-3}

For each channel diameter, we have simulated 20 values of each operating voltages, Vg and VDD in each simulation run based on variable temperature. Figure 2 illustrates the impact of varying channel diameter. The changing in ∆Id with increasing of temperature at the VDD ranges from 0 V to 5 V, step 0.25 V, that is for diameter (D.ch) = 80, 40, 20 and 10 nm. It's noticeable that the highest temperature sensitivity- max. ∆Id- are achieved at the lowest temperature, the values decreased linearly as the temperatures increased for all VDD. Temperature sensitivity (max ∆Id) increased remarkably with increasing channel diameter and the highest sensitivity was achieved with D.ch = 80 nm for T = 250 K and VDD = 3 V. The following maximum sensitivity were observed with other diameters: VDD = 2.5 V at D.ch = 40 nm, VDD = 1.75 V at D.ch = 20 nm and VDD = 1.25 V at D.ch = 10 nm respectively.

Figure 3 shows the optimized operating voltage V_{DD} based on best temperature sensitivity with channel diameter. So, the best increments in current (ΔI_d) with temperature will increase by increasing of diameter respectively, i.e. the best sensitivity is occurred by increasing the diameter and increasing temperature accordingly.

4.2. Electrical Characteristics

In the second simulation scenario, the effect of changing temperature on the electrical Characteristic has been evaluated. Three electrical performance metrics were considered in this scenario, SS, DIBL, and V.th. As shown in Figure 4 (a), the Subthreshold Swing (SS) proportionally increases with the surrounding temperature and the channel diameter as well. Perfect SS values are achieved at lower diameter values, where the obtained SS are closer to the ideal value specially when D.ch = 10 and 20 nm. The SS value was significantly increased with D.ch = 80 at higher temperature values. Figure 4 (b) presents the threshold voltage (V.th) of Si-NWT for various temperatures and channel diameters. It is obvious that V.th increased slightly with increasing the temperature, i.e. the higher the temperature is the higher V.th. Meanwhile, the threshold voltage inversely proportional to the channel diameter and the highest values of V.th are obtained at D.ch = 10 nm. Therefore, smallest channel diameter outperforms

the biggest ones in terms of both SS and threshold voltage regardless of operating temperature. Similarly, the increasing temperature causes a noticeable increment in DIBL metric as shown in Figure 4 (c). However, with increasing channel diameter the DIBL also increases except for the case with D.ch = 10 nm where the DIBL reaches a very high value. For the sake of figure clarity, the DIBL curve at 10 nm is omitted in this figure.

Figure 5 depicts all electrical characteristics, V.th, SS and DIBL with increasing SiNWT channel diameter (D.ch = 80, 40, 20 and 10 nm), at T = 300 K. It can be notice that V.th decreases with increasing channel diameter and nearly reached saturation beyond 40 nm; SS increases and nearly reached the best value at (60 mV/dec) between 20 and 40 nm and DIBL decreases strongly between 10 and 20 nm and increased slightly beyond 80 nm. Thus, as presented by this figure, the perfect channel diameter for the SiNWT under the conditions considered in this research is 20 nm.

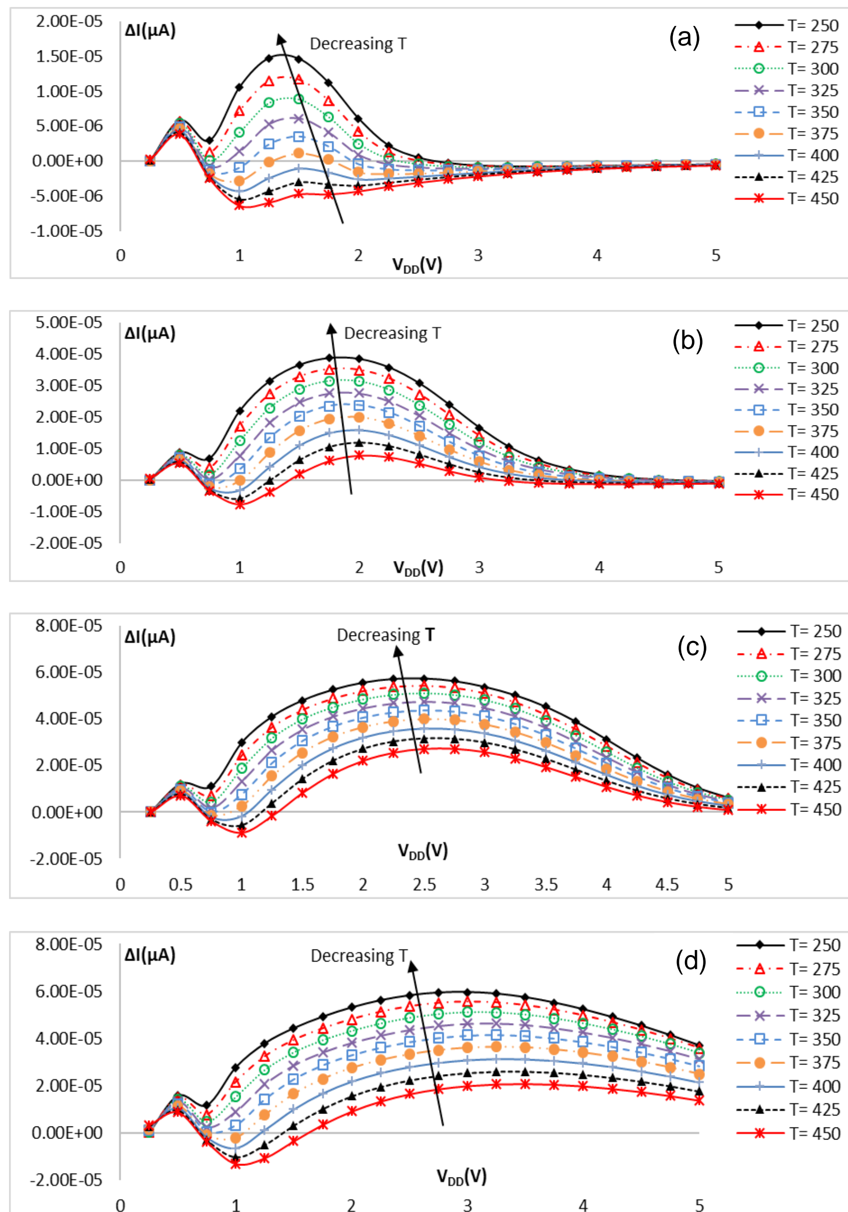

Figure 2. ΔI_d-V_{DD} characteristics of SiNWT with temperature for various channel diameter, (a) at Dch= 10 nm, (b) at Dch= 20 nm, (c) at Dch= 40 nm, (d) at Dch= 80 nm

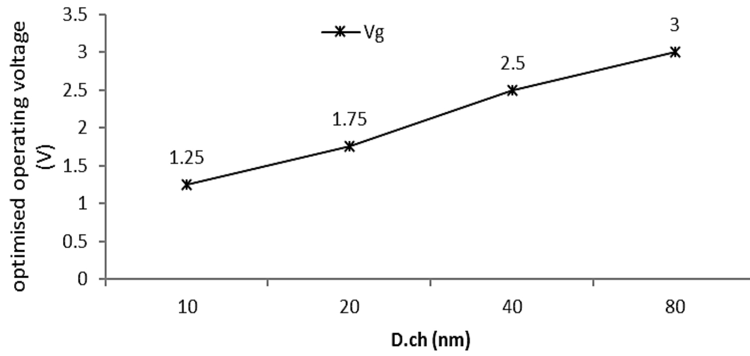

Figure 3. Optimized operating voltage V_{DD} with diameter channel based on best temperature sensitivity

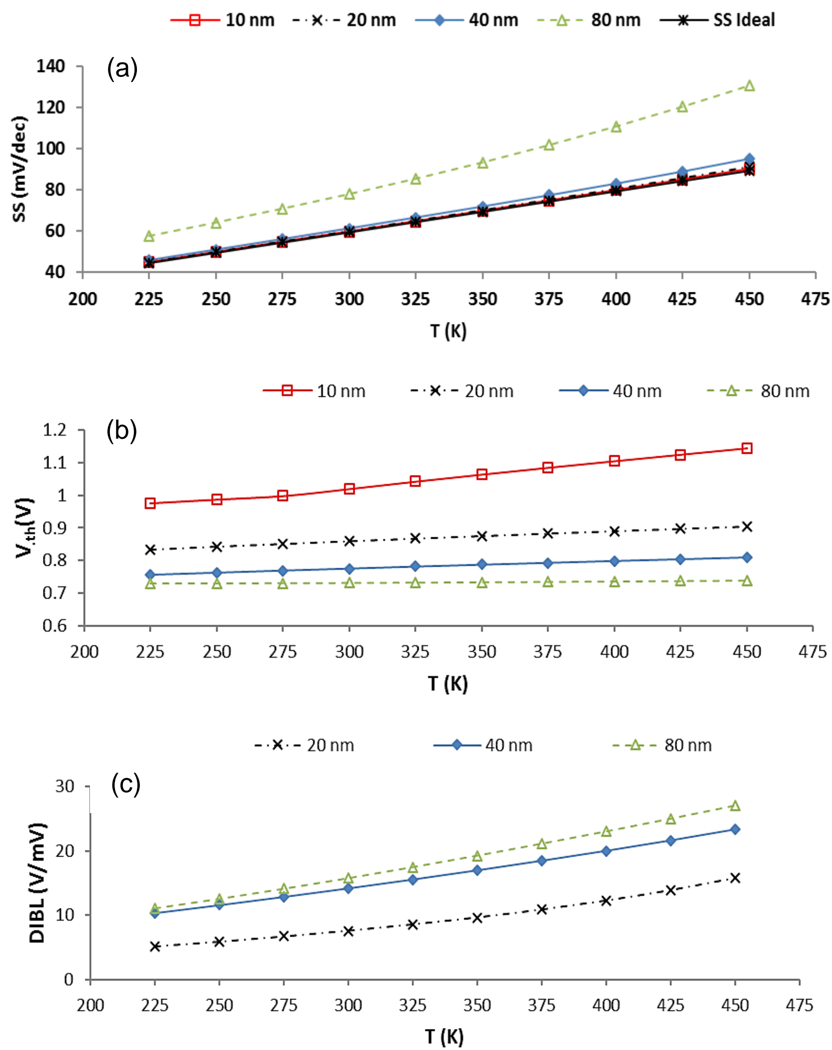

Figure 4. Electrical characteristics of SiNWT, (a) Subthreshold Swing vs. Temperature for varying channel diameter; (b) V.th vs. Temperature for varying channel diameter; (c) DIBL vs. Temperature for varying channel diameter

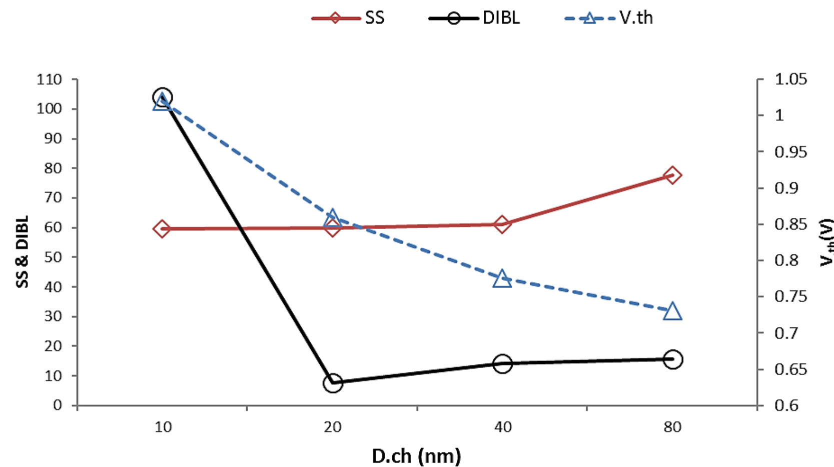

Figure 5. Electrical characteristics of SiNWT SS, DIBL and V.th vs. channel diameter

5. Conclusion

The effects of varying channel diameter of Si-NWT on the temperature and electrical characteristics were investigated. Thermal sensitivity increased remarkably with increasing various channel diameter and operating temperature. The impacts of operating temperature (T) of Si-NWT on its electrical characteristics (V.th, SS, DIBL) were analyzed. All the considered metrics were increased proportionally in a different degree, with increasing T. The highest V.th was achieved with the lowest channel diameter of 10 nm, whereas the lowest and best DIBL was achieved at 20 nm which also has a very close SS to the ideal (60 mV/dec).

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References

[1] HT AlAriqi, WA Jabbar, Y Hashim, HB Manap. Temperature Characteristics of Silicon Nanowire Transistor Depending on Oxide Thickness. *Journal of Nano and Electronic Physics.* 2019; 11(3): 1-4.
[2] P Clarke. Intel enters billion-transistor processor era. EE Times. 2005; 14.
[3] A Mahmood, WA. Jabbar, Y Hashim, HB Manap. Electrical Characterization of Ge-FinFET Transistor Based on Nanoscale Channel Dimensions. *Journal of Nano and Electronic Physics.* 2019.
[4] MM Waldrop. The chips are down for Moore's law. *Nature News*. 2016; 530: 144.
[5] WA. Jabbar, MH. Alsibai, NSS Amran, SK Mahayadin. *Design and Implementation of IoT-Based Automation System for Smart Home*. in 2018 International Symposium on Networks, Computers and Communications (ISNCC). 2018; 1-6.
[6] IF Akyildiz, M Pierobon, S Balasubramaniam, Y Koucheryavy. The internet of bio-nano things. *IEEE Communications Magazine.* 2015; 53: 32-40.
[7] WA Jabbar, M Ismail, R Nordin. *Evaluation of energy consumption in multipath OLSR routing in Smart City applications.* in 2013 IEEE 11th Malaysia International Conference on Communications (MICC). 2013; 401-406.
[8] WA Jabbar, M Ismail, R Nordin. *MBA-OLSR: a multipath battery aware routing protocol for MANETs*. in 2014 5th International Conference on Intelligent Systems, Modelling and Simulation. 2014; 630-635.
[9] WA Jabbar, WK. Saad, M. Ismail. MEQSA-OLSRv2: A Multicriteria-Based Hybrid Multipath Protocol for Energy-Efficient and QoS-Aware Data Routing in MANET-WSN Convergence Scenarios of IoT. *IEEE Access.* 2018; 6: 76546-76572.
[10] HF Atlam, RJ Walters, GB Wills. *Internet of nano things: security issues and applications.* in Proceedings of the 2018 2nd International Conference on Cloud and Big Data Computing. 2018; 71-77.
[11] PJ Vikesland. Nanosensors for water quality monitoring. *Nature nanotechnology.* 2018; 13: 651.

[12] S Mangesh, P Chopra, KK Saini. A Trapezoidal Cross-Section Stacked Gate FinFET with Gate Extension for Improved Gate Control. *International Journal of Advanced Computer Science and Applications*. 2019; 10: 189-194.
[13] WA Jabbar, M Ismail, R Nordin. *Framework for enhancing P2P communication protocol on mobile platform*. Proceedings of the ICIA. 2012; 12.
[14] O Lupan, V Postica, F Labat, I Ciofini, T Pauporté, R Adelung. Ultra-sensitive and selective hydrogen nanosensor with fast response at room temperature based on a single Pd/ZnO nanowire. *Sensors and Actuators B: Chemical*. 2018; 254: 1259-1270.
[15] KM Musick, JR Wendt, PJ Resnick, MB Sinclair, DB Burckel. Assessing the manufacturing tolerances and uniformity of CMOS compatible metamaterial fabrication. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*. 2018; 36(1): 011208.
[16] J Watson, G Castro. A review of high-temperature electronics technology and applications. *Journal of Materials Science: Materials in Electronics*. 2015; 26: 9226-9235.
[17] M Li, G Chen, R Huang. High Performance GAA SNWT with a Triangular Cross Section: Simulation and Experiments. *Applied Sciences*. 2018; 8: 1553.
[18] A Emadi. *Handbook of automotive power electronics and motor drives*. CRC press. 2005.
[19] H Khan, A Razmjou, M Ebrahimi Warkiani, A Kottapalli, M Asadnia. Sensitive and Flexible Polymeric Strain Sensor for Accurate Human Motion Monitoring. *Sensors. 2018;* 18: 418.
[20] IS Arafat, N Balamurugan, SB Khan. *Influence of Temperature in Scattered SiNW MOSFET*. Proceedings of the National Academy of Sciences, India Section A: Physical Sciences. 2019; 89: 35-40.
[21] E Hunt-Schroeder, D Anand, J Fifield, M Roberge, D Pontius, M Jacunski. 14nm FinFET 1.5 Mb Embedded High-K Charge Trap Transistor One Time Programmable Memory Using Differential Current Sensing. *IEEE Solid-State Circuits Letters*. 2019.
[22] Y Jiang, W Wang, Z Wang, JP Wang. Incorporation of Phosphorus Impurities in a Silicon Nanowire Transistor with a Diameter of 5 nm. *Micromachines*. 2019; 10: 127.
[23] A Mahmood, WA. Jabbar, WK. Saad, Y Hashim, HB Manap. *Optimal Nano-Dimensional Channel of GaAs-FinFET Transistor*. in 2018 IEEE Student Conference on Research and Development (SCOReD). 2018; 1-5.
[24] A Mahmood, WA Jabbar, Y Hashim, HB Manap. Effects of downscaling channel dimensions on electrical characteristics of InAs-FinFET transistor. *International Journal of Electrical and Computer Engineering (IJECE)*. 2019; 9: 2902-2909.
[25] AA Almohammedi, NK Noordin, A Sali, F Hashim, WA. Jabbar, S Saeed. Modeling and analysis of IEEE 1609.4 MAC in the presence of error-prone channels. *International Journal of Electrical and Computer Engineering (IJECE)*. 2019; 9: 3531-3541.
[26] Y Atalla, Y Hashim, ANA Ghafar, WA. Jabar.Temperature Characterization of (Si-FinFET) based on Channel Oxide Thickness. *TELKOMNIKA Telecommunication, Computing, Electronics and Control*. 2019; 17: 2475-2480.
[27] *MuGFET Simulation Tool* (Access on March 2019). Available: https://nanohub.org/