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A highly effective and simplified DPWM algorithm for NPC inverters for high power factor load applications

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ABSTRACT

In recent years, high-power three-level neutral point clamped (NPC) inverters have significantly increased, particularly in the renewable energy sector and industries. These inverters are crucial in applications such as offshore wind farms and high-power motor drives, where reducing switching losses and improving the overall longevity, efficiency, and reliability of inverter systems are key. While conventional space vector pulse width modulation (SVPWM) has been used to reduce switching losses, it also increases the computational burden in the αβ coordinates. Our study introduces an effective and highly efficient carrier-based discontinuous pulse width modulation (DPWM) method specifically designed for high power factor loads to address this challenge. This approach significantly reduces computational execution time by adding the zero-sequence function into the fundamental signals. The efficiency of our new method is evident in the results: the proposed DPWM has successfully reduced switching losses, leading to a substantial enhancement of system efficiency. Our space vector analysis and simulation results, achieved using MATLAB and PLECS software, further validate the efficiency of our approach. Additionally, experimental results with a small-scale three-phase NPC inverter were conducted to validate the effectiveness and efficiency of the proposed DPWM.

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1. INTRODUCTION

Primary goals in industrial applications revolve around optimizing power capacity and minimizing manufacturing costs. Achieving a balance between maximizing power rating and minimizing manufacturing expenses is challenging and often requires a compromise. In low-voltage scenarios, the two-level inverter is a popular choice due to its cost-effectiveness and simplicity of control [1]-[3]. However, it's important to note that the two-level inverter does suffer from high output voltage harmonics, which in turn necessitates an expensive, bulky power filter [4], [5]. This financial burden, coupled with the limitation of voltage stress in the semiconductor switches, means that two-level inverters are typically restricted to low-voltage applications [6]-[8].

The challenges posed by the issues have been tackled through the three-level inverter [9], [10]. Compared to the two-level inverter which has only two voltage levels $+V_{DC}/2$ and $-V_{DC}/2$, the three-level inverter offers three output voltage levels of $+V_{DC}/2$, 0 and $-V_{DC}/2$ [11]. As a result, conventional three-level inverters distribute a lower voltage stress per switch. In industrial applications, ensuring low electromagnetic interference (EMI) is crucial as it helps to maintain signal integrity, prevent disruptions in sensitive equipment,

and comply with stringent regulatory standards. For these issues, the three-level neutral-point-clamped (NPC) inverter has been advantageous for its low EMI and superior efficiency [12], [13].

Pulse width modulation (PWM) has been a practical approach [14], [15] to control a three-level NPC inverter. Two essential PWM control strategies are multi-carrier PWM and space vector PWM (SVPWM) [16]. In the approach of multi-carrier PWM, the process of generating switch-gating signals includes comparing the modulation signal with carriers [17]. In contrast, space vector modulation (SVM) is a more sophisticated technique that determines reference vector location, active voltage vectors, and their corresponding dwelling times in αβ coordinates [18], [19]. The SVM method enables flexible control of the inverter output voltages by continuously controlling the voltage vector sequences and their timings. However, its implementation necessitates burden calculations involving trigonometric functions on the microprocessor. This complexity also appears from the dynamic manipulation of voltage vectors in a multi-dimensional coordinate system, underscoring the challenges of enhancing power electronics systems' performance.

The primary difficulty with the high-power three-level NPC inverter is switching losses and high computation burden, even though several PWM approaches, such as multi-carrier PWM, selective harmonic elimination, and SVM, have been proposed to enhance output voltage quality. This work proposes a simplified discontinuous pulse width modulation algorithm (DPWM) using a carrier-based approach to improve PWM control further [20], [21]. The proposed technique minimizes computational complexity by injecting zero-sequence functions into the fundamental signals. The proposed method is to select offset voltage to the adjusted control signal to regulate the dwelling times of switching states. Additionally, in terms of sensor usage, measuring load currents is unnecessary for high-power factor load, which reduces the cost of high-performance microcontrollers and overall system expenses. This advancement enhances the method's adaptability to low-cost microcontrollers, making power inverter control more accessible and cost-effective for industrial systems. The study employs space vector analysis and uses MATLAB and PLECS models to conduct carrier-based PWM simulations. Additionally, experimental validation using a small-scale three-phase NPC inverter shows the efficacy and feasibility of the proposed DPWM technique.

2. THREE-LEVEL NPC INVERTER SCHEMATIC AND MODULATION ANALYSIS

The three-level NPC inverter is gaining much attention for its use in renewable energy power conversion and motor drive applications. This topology is advantageous for its efficiency and simplicity. This topology reduces the number of components needed and makes it economical and suitable for a wide range of high-power applications [22]. NPC inverter structures can be either diode-clamped type using diodes to control voltage levels or T-type incorporating switches for improved efficiency and reduced component count. Figure 1 shows the schematic of a three-level T-NPC inverter, which presents a typical 3 level inverter used in practice, with twelve insulated-gate bipolar transistor (IGBT) switches organized into three inverter legs. These legs connect to the three-phase load via midpoints A, B, and C, as illustrated in the diagram [23].

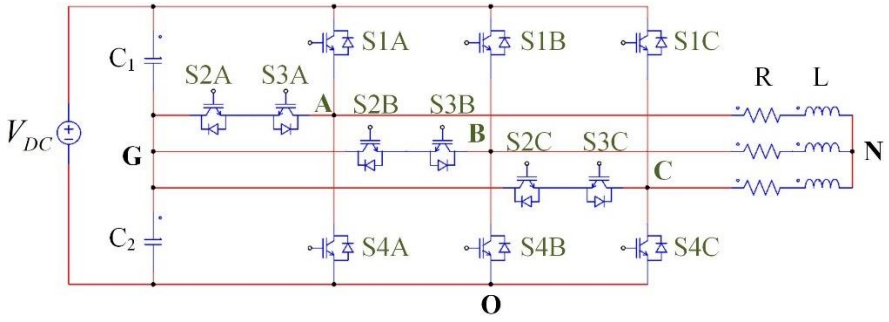


Figure 1. The three-level T-NPC inverter topology

The instant voltage values can be deduced by analyzing the switching states of the IGBT switches. There are 27 switching vectors: six large, six medium, twelve small, and three null or zero. If the two capacitors C_1 and C_2 in the three-level NPC inverter are the same, the capacitor voltage V_{C1} and V_{C2} will be equal ($V_{C1} = V_{C2}$). The shared voltage across both capacitors is half the magnitude of the DC bus voltage. Table 1 shows the phase-to-G point voltage values (V_{XG}; X=A, B, C) and phase-to-O point voltage (V_{OG}) corresponding to each switching state. In the table, a value of 1 indicates the switch is in the ON position, while 0 signifies that the IGBT is in the OFF position. The mathematical equation represents the switching state as (1):

$$\begin{cases} S_{2X} \geq S_{1X} \\ S_{1X} + S_{3X} = 1 \\ S_{2X} + S_{4X} = 1' \\ X = A, B, C \end{cases} \quad (1)$$

Within (1), S_{JX} represents the switching state of the switch S_{JX}, S_{JX}=1 if S_{JX} is on and S_{JX}=0 if S_{JX} is off, where X stands for A, B, or C and J=1,2,3,4. The phase-to-neutral point voltage V_{XG} exhibits three voltage levels: $+V_{DC}/2$, $-V_{DC}/2$ and 0. The calculation of its value is as (2):

$$V_{XG} = \frac{(S_X - 1)}{2} V_{dc} \quad (2)$$

where $S_X=S_{1X}+S_{2X}$.

Table 1. NPC inverter switching states

S_x	The switching states				V_{XO}	V_{XG}
	S_{1X}	S_{2X}	S_{3X}	S_{4X}		
2	1	1	0	0	$+V_{DC}$	$+V_{DC}/2$
1	0	1	1	0	$+V_{DC}/2$	0
0	0	0	1	1	0	$-V_{DC}/2$

3. CONVENTIONAL PULSE WIDTH MODULATION TECHNIQUE

Among PWM techniques, phase disposition pulse width modulation (PD-PWM) is often preferred due to its simple implementation and high output voltage quality [20], [21]. The PD-PWM approach generates voltage output by using two level-shift in-phase carriers. For example, switches S_{1X} and S_{3X} receive their pulse switching signals from the upper carrier signal (V_{car1}), while switches S_{2X} and S_{4X} receive their switching signals from the lower carrier signal (V_{car2}).

Figure 2 illustrates the basic concept of a PD-PWM method using two triangular carriers. However, the conventional PD-PWM technique poses a significant challenge—unavoidable switching losses due to the sinusoidal nature of the modulation signal compared to a carrier wave [24], [25]. The constant switching of the three-phase legs in each sampling period increases switching losses, particularly in high-power load applications.

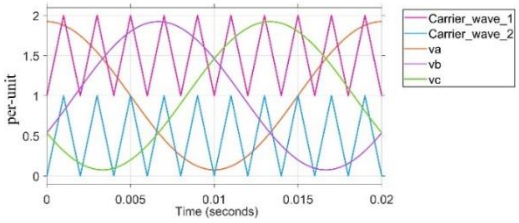
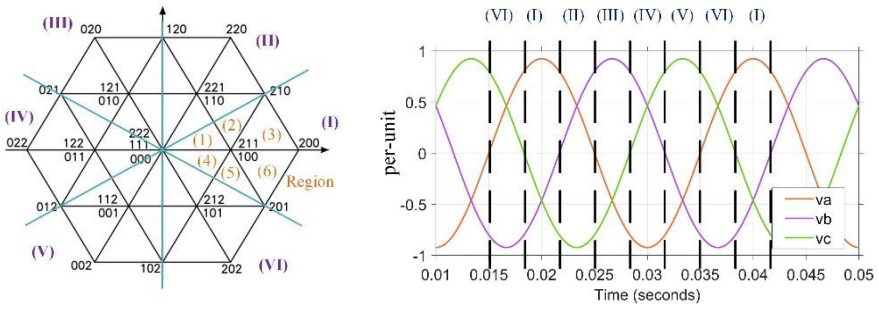


Figure 2. Carriers and modulation signals in conventional PD-PWM scheme

4. PROPOSED DPWM TECHNIQUE USING ADDITIONAL OFFSET VOLTAGE CONTROL

DPWM, a key PWM strategy in the field of power electronics, is often used to reduce switching loss in voltage source inverters. One effective way to minimize switching loss is to strategically avoid switching for the phase leg with the highest current. This strategic approach can be extended to high-load power factor converter systems, where the avoidance of switching to the phase with the highest voltage amplitude is a significant breakthrough. The hexagonal diagram of the three-level NPC inverter is divided into six sectors labeled from I to VI, as shown in Figure 3(a). Figure 3(b) depicts the corresponding output voltage waveforms, highlighting specific sections for better understanding and correlation with Figure 3(a). In Figure 3(b), the highest voltage amplitude consistently corresponds to the maximum phase voltage in sectors I, III, and V.

Conversely, in the remaining sectors, the highest voltage amplitude consistently displays the minimum phase voltage. For instance, phase A voltage and current reach their highest amplitude values in sector I. Here, the necessity of preventing phase A commutation becomes apparent, as it is a crucial step to optimize switching loss.



(a) (b)

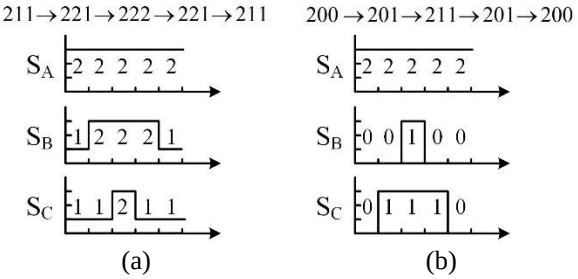
Figure 3. Proposed sector definitions labelled from I to VI; (a) sector and region definitions in the space vector diagram and (b) sectors I to VI and its corresponding three phase voltage reference

This can be achieved using the offset voltage ($V_{DC} - v_a$), equivalent to the function ($2 - v_a$). Similarly, voltages and currents reach their minimal levels in phase C-sector II. Minimizing switching loss requires preventing phase C commutation by holding the C phase leg voltage to 0. It makes the offset voltage value ($-v_c$) and the related extra offset value ($-v_c$). By defining sectors, I to VI related to the three-phase voltage reference in Figure 3(b), a sector detection block diagram is proposed to identify the sector. This method is of significant importance as it is based on simple comparing three-phase voltage reference values.

In the proposed control scheme, each sector can be divided into discrete zones labeled from 1 to 6, as illustrated for sector I in Figure 3(a). A description of switching states related to region 1 of sector I is carried out to demonstrate the idea in the the maximum voltage value (v_a). Table 2 shows that throughout region I, the value of v_a^* is always the greatest, indicating that $v_a^* > v_b$ and $v_a^* > v_c$ during this time. During the entire switching cycle, switch S_A remains unchanged, which is state 2. In sector I, the optimal switching sequence for the least losses is shown in Figure 4(a) for region 1 and Figure 4(b) for region 6. Consequently, by maintaining the switching state S_A=2 unchanged throughout the sector I, the proposed control strategy enhances the efficiency of the NPC inverter. A similar analysis can be applied to the remaining sectors.

Table 2. Proposed offset voltage function for sectors I to VI

	Sector (I)	Sector (II)	Sector (III)	Sector (IV)	Sector (V)	Sector (VI)
Offset voltage (v_0)	$2 - v_a^*$	$-v_c^*$	$2 - v_b^*$	$-v_a^*$	$2 - v_c^*$	$-v_b^*$
Conditions	Max =v_a^*	Min = v_c^*	Max =v_b^*	Min = v_a^*	Max =v_c^*	Min = v_b^*



(a) (b)

Figure 4. An examination of the switching states and sequence related to region 1 and region 6 of sector I; (a) S_A, S_B, and S_C states in region 1 and (b) S_A, S_B, and S_C states in region 6

To implement carrier based PWM method, a voltage offset v_0 will be proposed. The modulating signals corresponding to the leg voltage v_i can be expressed as (3):

$$v_i = v_i^* + v_0, \quad (3)$$

where v_i^*, i=a,b,c are reference fundamental voltages. The main issue now is determining the voltage offset. v_0. For sectors I, III and V, the offset voltage is derived as (4):

$$v_0 = 2 - v^*_{max} \quad (4)$$

where $V^*_{max} = max(v^*_a, v^*_b, v^*_c)$. For the remaining sectors, the offset voltage is derived as:

$$v_0 = -v^*_{min}.$$

where $V^*_{min} = min(v^*_a, v^*_b, v^*_c)$. The offset functions proposed for all sectors are described completely in Table 2.

The block diagram of proposed DPWM in Figure 5. The sinusoidal reference waveforms v^*_a, v^*_b, and v^*_c are sent as inputs to the offset generator block, which defines the offset with some comparison operators of phase voltage reference. After that, the relevant voltage offset adds to the fundamental references. Periodically, the modulating signals are compared with carrier waves for gererating pulse signals.

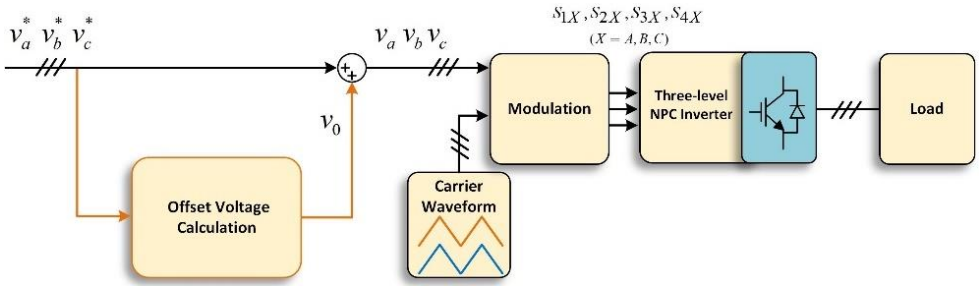
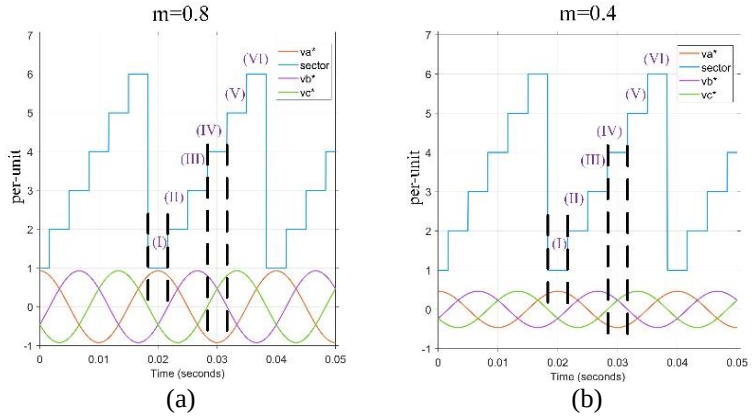


Figure 5. The block diagram of proposed DPWM

5. SIMULATION RESULTS AND DISCUSSION

To obtain the performance of the proposed DPWM approach, simulated implementation has been carried out using MATLAB software. The simulation will be conducted with specified system parameters, including a DC supply voltage of v_{DC}= 300 V, and the output fundamental frequency (f_{NPC}) of 50 Hz. For the load parameters, load resistance (R) is 1.5 Ω, and load inductance (L) is 1 mH. The carrier frequency or switching frequency is $f_{carrier}$=3 kHz. The reference voltage waveforms and indexes of related sectors for two modulation index values, m=0.8 and m=0.4, are shown in Figures 6(a) and (b). As seen in Figures 6(a) and (b), the additional offset is easily determined from the maximum and minimum voltage values as described in Table 2. For demonstration, the simulated sector index changes in a sequence from sector I to sector VI, which is identical to the sector analysis in section 4. The modulating (or leg) voltages are shown in Figures 7(a) and (b), and the offset voltages are shown in Figures 7(c) and (d). The IGBT gate signals are then produced by comparing these modulating leg voltages with carrier waves, which is set at 3 kHz.



(a) (b)

Figure 6. The sector detection performance and its corresponding voltage reference; (a) modulation index is set as 0.8 and (b) modulation index is set as 0.4

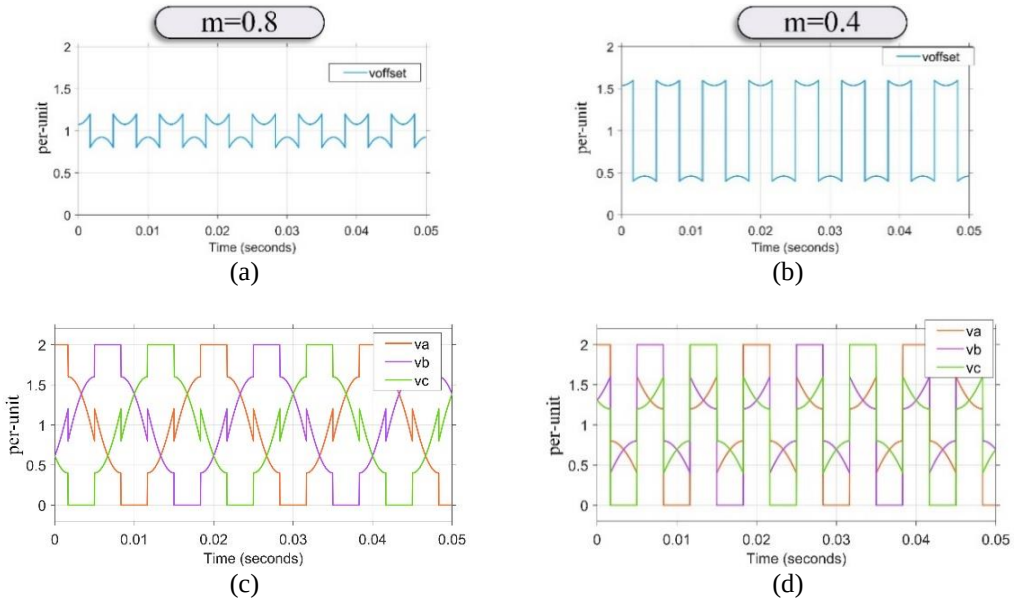


Figure 7. The shifted offset voltage waveform and the modulating waveform; (a) modulation index is set as 0.8, (b) modulation index is set as 0.4, (c) offset voltage waveform with modulation index is set as 0.8, and (d) offset voltage waveform with modulation index is set as 0.4

Figures 8(a) and (b) display the output voltage V_{AG}, the leg voltage V_{AN}, and phase A current (i_a) for modulation index values (m) of 0.8 and 0.4. It can be seen that there are no commutations in phase A during sector I and sector IV when phase A output current reaches its largest and lowest values, respectively and the inverter voltage V_{AG} maintains constant as shown in Figures 8(a) and (b). These simulation results, confirm that by avoiding switching at highest current, the proposed DPWM enables reducing switching losses and improving inverter efficiency.

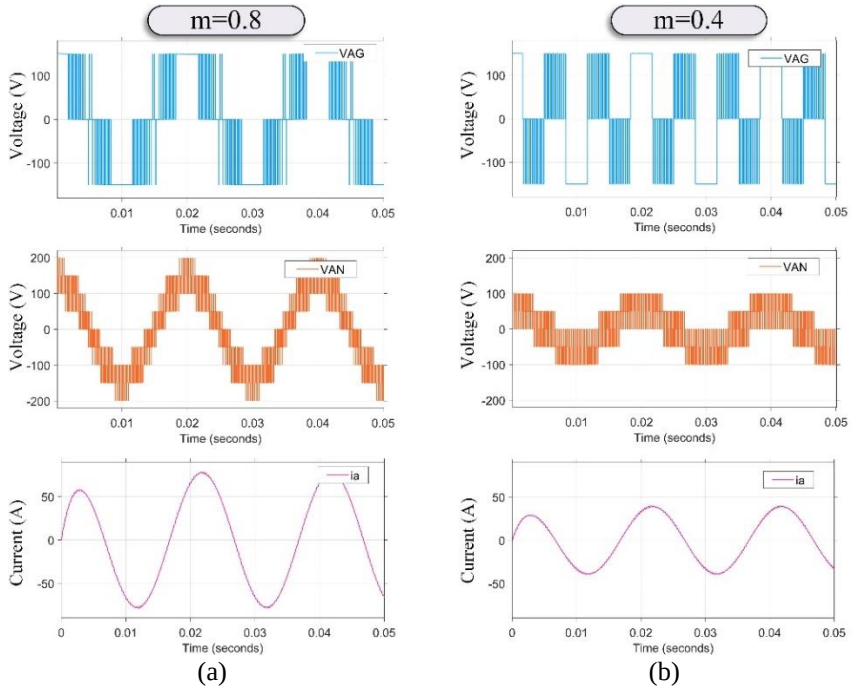
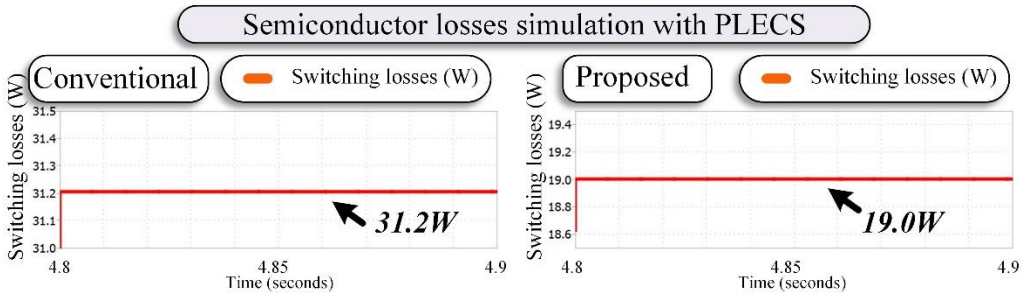


Figure 8. Voltage between A and G points (V_{AG}), voltage between A and N points (V_{AN}), and phase A current (i_a); (a) modulation index is set as 0.8 and (b) modulation index is set as 0.4

A PLECS loss simulation platform was performed to calculate switching loss. Figures 9(a) and (b) display the averaging value of switching losses of all switches in NPC inverter for the conventional PDPWM method [20] and for the proposed DPWM method. The IGBT and diode datasheet from PLECS model in [26] are used. The modulation index and fundamental frequency are set as m=0.8 and f=50 Hz, respectively. As shown in Figures 9(a) and (b), the switching losses of the proposed DPWM, equal to 19W are reduced significantly compared with 31.2 W of the conventional sinusoidal PWM method.



(a) (b)

Figure 9. Switching losses simulation using PLECS platform with modulation index is set as 0.8; (a) conventional method and (b) proposed method

6. EXPERIMENTAL RESULTS AND DISCUSSION

In order to verify the proposed method effectively, the small-scale experimental system is set up with system parameters listed in Table 3. In the experiment, the microcontroller Texas instrument (TI) 28379D is used, and the sampling frequency is set to be equal to that of the switching frequency ($f_{sampling}$=3 kHz). The voltage reference and detected sector waveforms are calculated by the TI microcontroller TMS320F28379D, and it is exported to display in the oscilloscope using a digital-to-analog converter (DAC) module. The laboratory three phase NPC experimental system is shown in Figure 10.

Table 3. Small-scale experimental system parameters

Parameter	Value
Input power and control parameters	
DC source voltage (V)	75 V×2 sources=150 V
Microcontroller	TI TMS320F28379D
DAC module	DAC A and B of 28379D launchpad
Output frequency	50 Hz
Carrier frequency (switching frequency)	3 kHz
Controller sampling frequency	3 kHz
Oscilloscope specs	
Bandwidth	100 MHz
Voltage probe	10 X/100 MHz
Modulation index testing cases	
Case 1	Modulation index m=0.8
Case 2	Modulation index m=0.4

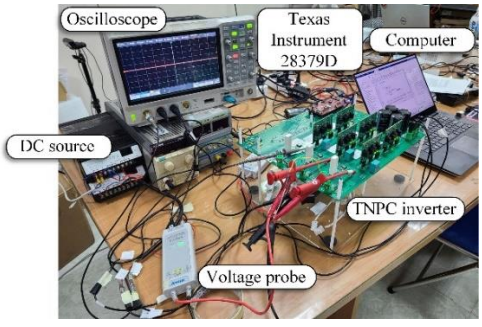
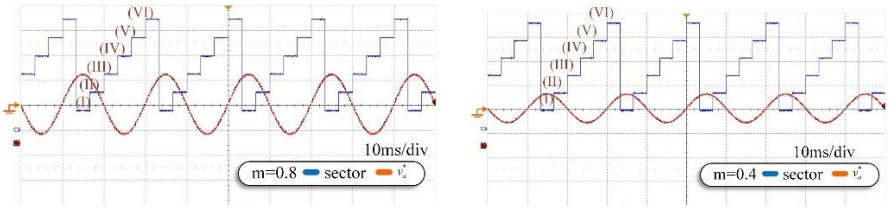


Figure 10. The laboratory three phase NPC experimental system

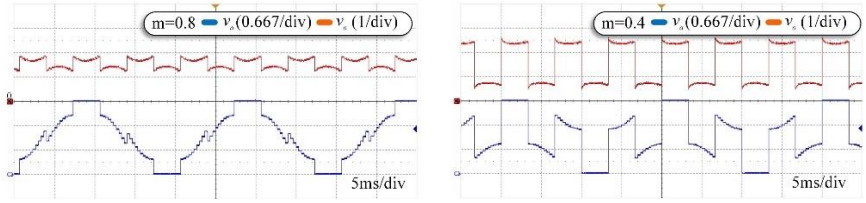
Figures 11(a) and (b) show the experimental results of voltage reference when the modulation index values are set as 0.8 and 0.4, respectively. For illustration, sector index number is also presented in a sequence from sector I to sector VI, which is identical with the analysis in section 4. Figures 12(a) and (b) show the offset voltage waveforms exported from the TI microcontroller. Figures 12(a) and (b) present the modulation signal deduced by adding the reference voltage with the proposed offset voltage. Both the offset voltage and modulation voltage have waveforms similar to that of the simulation results.

For modulation indices m=0.8 and m=0.4, Figures 13(a) and (b) show the VAG waveform of the sinusoidal PD PWM and Figures 13(c) and (d) show the VAG waveform of the proposed DPWM method. For example, in the case of m=0.8, there is no switching to appear, and VAG maintains constant in phase A during sectors I and IV, corresponding to the peak and minimum values of phase A output current. Similarly, it can be explained for case of m=0.4. The results of the experiment demonstrated in Figures 11-13, show the advantages of the proposed control approach in terms of reducing switching losses and increasing inverter efficiency.



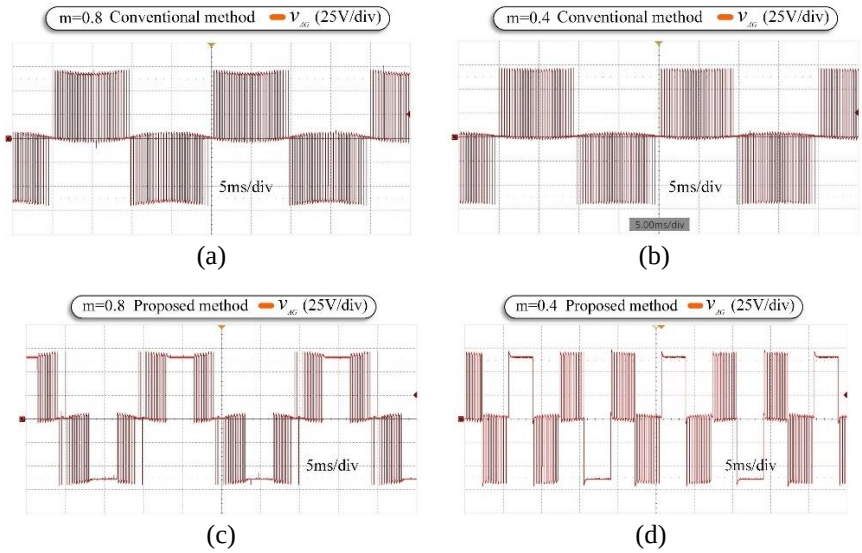
(a) (b)

Figure 11. Experimental results of sector detection and voltage reference exported from microcontroller; (a) modulation index is set as 0.8 and (b) modulation index is set as 0.4



(a) (b)

Figure 12. Experimental waveforms of offset voltage and modulation voltage; (a) modulation index is set as 0.8 and (b) modulation index is set as 0.4



(a) (b)

(c) (d)

Figure 13. Experimental waveform of V_{AG} with the conventional and proposed control methods; (a) conventional method with modulation index 0.8, (b) conventional method with modulation index 0.4, (c) proposed method with modulation index 0.8, and (d) proposed method with modulation index 0.4

7. CONCLUSION

This paper investigates a simplified DPWM algorithm for an NPC inverter, a method that can be effectively applied to high-power loads with power factors close to unity. In contrast to the complexity of SVPWM in αβ coordinates, we propose a new carrier-based PWM approach using an additional offset voltage. This offset voltage is added to fundamental voltages to create the reference three-phase voltages. The proposed control approach effectively reduces switching losses, increasing efficiency. The simplicity of the proposed DPWM strategy makes the method more accessible and cost-effective for industrial applications, particularly for low-cost microcontrollers. Finally, the simulation and experimental results have validated the effectiveness of the proposed method.

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