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# A low power wideband varactorless VCO using tunable active inductor

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**ABSTRACT**

This paper presents a wideband varactorless voltage controlled oscillator (VCO) based on tunable active inductor in 90 nm CMOS process which yields a tuning range of 1.22 GHz to 3.7 GHz having a tuning scope of 100.5%. The designed VCO can be used for wideband wireless applications. The proposed VCO consumes a very low power (1.05~2.5) mW with the change of tuning voltages (0.3~0.9) V and provides a differential output power of (1.17~-5.13) dBm. The VCO exhibits phase noise of -80.50 dBc/Hz @ 2.74 GHz and the Figure of merit (FOM) is -147.73 dBc/Hz @ 2.74 GHz at 1MHz offset frequency. Achievement of high tuning range by altering the inductance of inductor which paves the way for eliminating the MOS varactor that recedes the overall silicon area consumption, is the noteworthy outcome of the proposed VCO. Furthermore, considering the dc power consumption, Figure of merit (FOM) and consistency of performance parameters over tuning range, the proposed VCO outstrips the other referred VCOs.



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## 1. INTRODUCTION

In the modern era of communication, voltage controlled oscillator has grabbed a significant position, gradually has become indispensible in many cases. Phase Locked Loop (PLL) which is used for frequency multiplier, divider and FM detector, has an unavoidable component, VCO [1-3]. Moreover, frequency jammer, function generator, analog to digital converter, RFID has an inevitable element, which is voltage controlled oscillator [4-10]. VCO can be implemented in two major ways: LC VCO and Ring VCO [11]. Power consumption, tuning range, phase noise, silicon area consumption and output power are the basic parameters for characterizing a VCO. The phase noise is a kind of impurity of frequency spectrum, which evolved from the VCO's elements [12-13]. Ring VCO consumes less silicon area and also consumes less power, where LC VCO consumes a large silicon area due to the presence of spiral or passive inductor [11].

The substitution of the spiral or passive inductor with active inductor will be the best solution in case of large silicon area consumption. Basic active inductor is the two back to back connected transconductors with one port connected to a capacitor. CMOS active inductor provides several advantages such as high and tunable inductance as well as quality factor, low silicon area consumption and can be implemented in wide tuning ranged VCO [14]. On the contrary, poor phase noise performance and dc static

power consumption are the two major disadvantages of the active inductor [15]. However, the minimization of both of these two disadvantages will be the ultimate goal of a good design.

The main pivotal point of this proposed research is that making the active inductor tunable by altering the parameters that control the inductance of the inductor without any physical change, which is not possible for spiral inductor. Moreover, tuning capability of inductor will provide a good opportunity to tune the oscillation frequency of the LC-VCO. The most common technique to tune the oscillation frequency of VCO is obtained by imbedding MOS varctors, which adds to the total silicon area consumption. However, if high tuning range can be achieved by altering the inductance of the active inductor, then the varactors can be eliminated, which ultimately reduces the total silicon area consumtion.

## 2. LIANG FEEDBACK RESISTANCE REGULAR CASCODE ACTIVE INDUCTOR

Liang utilizes the Manetakis regulated cascode active inductor [16] by adding an additional resistance. Manetakis reduced the loss evolved from the series resistance by adding an additional regulated cascode, which is also further improved by Liang where a feedback resistor $R_f$ was added from the drain output of the $M_3$ to the gate input of $M_2$ as shown in the Figure 1 [17].

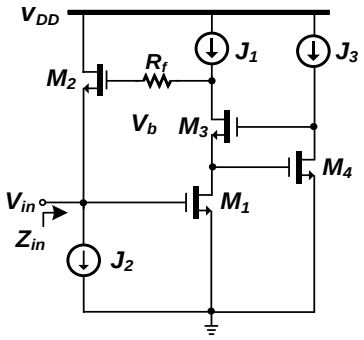


Figure 1. Schematic diagram of Liang feedback resistance regular cascode active inductor

The corresponding equation of the inductance, series resistance, capacitance and conductance are given below:

$$\begin{aligned} L &\approx \frac{C_{gs2}(1+R_f g_{o1})}{g_{m1}g_{m2}} \\ R_s &\approx \frac{g_{o3}g_{o4}}{g_{o1}g_{m1}g_{m2}g_{m3}g_{m4}} \\ C &\approx C_{gs1} \\ G &\approx g_{o2} + \frac{g_{m1}}{1+R_f g_{o1}} \end{aligned} \quad (1)$$

similarly, the self-resonant frequency and quality factor at self-resonant frequency is:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}(1+R_f g_{o1})}} \quad and \quad Q(\omega_o) = \frac{\omega_0 L}{R_s} = \frac{g_{o1}g_{m3}g_{m4}}{g_{o3}g_{o4}}\sqrt{\frac{g_{m1}g_{m2}C_{gs2}}{C_{gs1}(1+R_f g_{o1})}}$$

## 3. PROPOSED TUNABLE ACTIVE INDUCTOR

As ideal current source cannot be implemented practically so it should be replaced by MOS operated in saturated region. Figure 2 represents the proposed tunable active inductor where the ideal current sources $J_1$, $J_2$ and $J_3$ are replaced by MOSs $M_7$, $M_6$ and $M_5$, which are operated in saturation region. Now the inductance of the inductor given by

$$L \approx \frac{C_{gs2}(1+R_f g_{o1})}{g_{m1}g_{m2}} \quad (2)$$

So the inductance is directly proportional to the gate to source capacitance of MOS $M_2$ and inversely proportional to transconductance of MOS $M_1$ and $M_2$ and the change of the any of these three parameters will result in the change of inductance. The current through a MOS operated in the saturation region is given by:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(\mathrm{v_{gs}} - v_{th})^2 \quad (3)$$

The increment of the gate to source voltage will cause the increment of the drain current $I_{D_6}$ of the MOS $M_6$ . The increase of the drain current $I_{D_6}$ will cause the increase of the drain current of MOS $M_2$, finally the transconductance $g_{m2}$ according to the following equation.

$$g_m = \sqrt{\mu_n C_{ox}\frac{W}{L} I_D} \quad (4)$$

The inductance will be decreased and the reduction of the inductance will increase the oscillation frequency, when the inductor will be implemented in LC oscillator. Now, if a good tuning range can be achieved from altering the inductance only there will be a noteworthy opportunity to eliminate the varactors as a tuning parameter. An implemented varactor is nothing but mosfet with shorted drain, body and source. So, the integration MOS varactor will boost up the silicon area consumption. So, the elimination of MOS varactor will recede the silicon area consumption.

Tuning the inductance by changing the $g_m$ will result in a disadvantage that is the variation of dc power consumption. This will alter the phase noise of LC VCO as according to the equation given below phase noise has dependence on the dc power dissipation [18].

$$L(\Delta\omega) = 10\log\{\frac{2FkT}{P_s}[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2](1 + \frac{\Delta\omega_1/f^3}{\Delta\omega})\} \quad (5)$$

where,
$\Delta\omega =$ Frequency offset from the oscillation frequency $\omega_0$
$Q =$ Quality factor of the oscillator
$F =$ Excess noise factor
$k =$ Boltzmann constant
$T =$ Absolute Kelvin temperature
$P_s =$ Power dissipation

Similarly, the alternation on dc power dissipation will also alter the Figure of merit, which defines the overall performance of LC VCO by counting three major parameters: power consumption, oscillation frequency and phase noise [19].

$$FOM = L(\Delta\omega) + 10\log\left(\frac{P_{diss}}{1mW}\right) - 20\log\left(\frac{\omega_o}{\Delta\omega}\right) \quad (6)$$

The reduction of the variation of these two performing parameters (phase noise and Figure of merit) will be the major target of this proposed design. A significantly low value and low variation of DC power consumption will pave the way for the achievement of this goal.

Table 1 shows the W/L ratios for all the mosfets used in the proposed tunable active inductor depicted in Figure 2. Figure 3 shows the variation of the inductance value of the proposed tunable active inductor with the variation of tuning voltage ranging from 0.3 V to 0.9 V. Finally the Table 2 represents the numerical value of inductance for different frequencies with the variation of tuning voltages.

Table 1. Widths and lengths of implemented transistors

| MOS | Width (μm) | Length (nm) |
|---|---|---|
| $M_1$ | 12 | 120 |
| $M_2$ | 22 | 140 |
| $M_3$ | 25 | 140 |
| $M_4$ | *4.2* | *300* |
| $M_5$ | 4 | 120 |
| $M_6$ | 6 | 300 |
| $M_7$ | 4 | 120 |

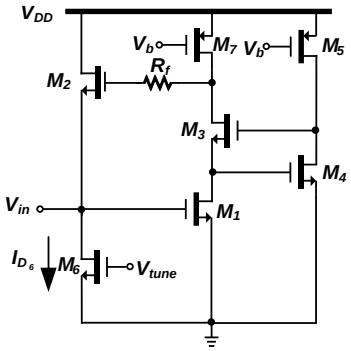


Figure 2. Liang feedback resistance regular cascode active inductor with saturated MOS as current source

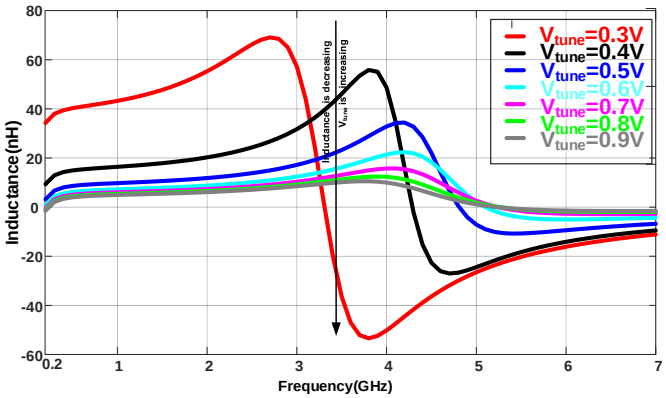


Figure 3. Variation of inductance with the variation of the control voltage $V_{tune}$

Table 2. Inductance at diffeent frequencies for different tuning voltages

| $V_{tune}$ | Inductance(nH) @ 1GHz | Inductance(nH) @ 2GHz | Inductance(nH) @ 3GHz | Inductance(nH) @ 4GHz | Power Consumption of AI (mW) |
|---|---|---|---|---|---|
| 0.3 | 43.3 | 55.3 | 57.3 | -50.2 | 0.259 |
| 0.4 | 16.4 | 20.3 | 31.7 | 48.7 | 0.331 |
| 0.5 | 9.77 | 11.8 | 17.2 | 32.8 | 0.446 |
| 0.6 | 7.24 | 8.76 | 12.4 | 21.4 | 0.588 |
| 0.7 | 6.03 | 7.34 | 10.3 | 15.7 | 0.737 |
| 0.8 | 5.36 | 6.57 | 9.21 | 12.3 | 0.878 |
| 0.9 | 4.95 | 6.11 | 8.50 | 99.9 | 1.007 |

## 4. PROPOSED TUNABLE ACTIVE INDUCTOR BASED VCO

NMOS LC VCO topology, which has cross coupled pair of NMOS transistors, with a tail current source is the most commonly used topology. The LC tank circuit is loaded at the drain terminal and a couple of LC tank forms the differential configuration. The back to back connected NMOSs are in common source configuration, so that a large voltage gain can be achieved, which is one of the fundamental conditions of the Barkhausen criteria for sustaining oscillation. Another condition regarding the total phase shift that it should be 0º or 360º is provided by these NMOSs which provides 180º phase shift as they are in common source configuration. Figure 4 presents the proposed active inductor based voltage controlled oscillator based on most commonly used NMOS LC VCO topology. The indicated dotted section is Liang regular cascade active inductor and the presence of two active inductors indicates the differential configuration. $V_{con}$ at the gate terminal of the MOS $M_6$ is the tuning voltage which changes the gate voltage and finally the inductance of the active inductor. $M_{neg}$s are the two MOSs, used as negative resistor whom resistance is controlled by MOS $M_8$ operated in saturation region. The overall contribution of these elements will result a differential output which are taken from the two output terminals *Out1* and *Out2*. Supply voltage $V_{DD}$ is used 1 V and the W/L ratios of all MOSs are given in Table 3.

Table 3. Widths and lengths of implemented transistors for the proposed VCO

| MOS | Width (μm) | Length (nm) |
|---|---|---|
| $M_1$ | 12 | 120 |
| $M_2$ | 22 | 140 |
| $M_3$ | 25 | 140 |
| $M_4$ | 4.2 | 300 |
| $M_5$ | 4 | 120 |
| $M_6$ | 6 | 300 |
| $M_7$ | 4 | 120 |
| $M_{neg}$ | 30 | 100 |
| $M_8$ | 30 | 100 (multipliers = 3) |

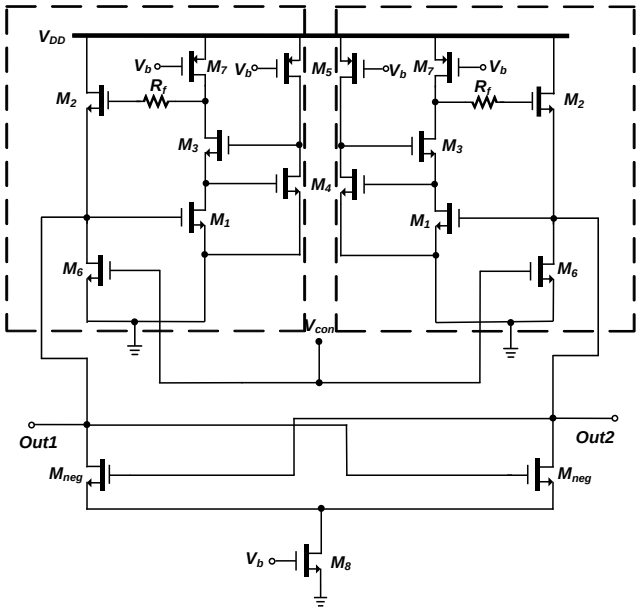


Figure 4. Proposed tunable active inductor based VCO

## 5. SIMULATION RESULTS

Transient, pss (with 5 harmonics), pnoise, dc analysis had been performed to achieve output oscillation, oscillation frequency, phase noise, output power and dc power dissipation of the proposed VCO. The oscillator shows an oscillation frequency ranging from 1.22 GHz to 3.7 GHz with the variation of control voltage ranging from 0.3 V to 0.9 V. The tuning scope is 100.5% and the oscillator yields a phase noise of -77.01 dBc/Hz to -76.44 dBc/Hz in the whole tuning range. The dc power dissipation is 1.05 mW to 2.50 mW where the $V_{DD}$ is 1V. The dc power consumption is very low which is one of the major focal points of the proposed VCO. The proposed VCO provides differential output power of 1.17 dBm to -5.13 dBm with the increment of tuning frequency. Table 4 shows the performance parameters of the proposed active inductor based differential VCO for the variation of control voltage.

Table 4. Performance parameters for different tuning voltage $v_{con}$

| $V_{con}$ (V) | Freq. (f) GHz (PSS | Output Oscillation Differential (P-P) mV | Voltage (PSS) @f Differential +ve -ve mV | Phase Noise @ 1MHz offset dBc/Hz | Power Diss. @1V (mW) | Output Power (50-ohm R) Differential +ve -ve (dBm) | Figure of merit (FOM) @ 1 MHz Offset dBc/Hz | dBF |
|---|---|---|---|---|---|---|---|---|
| 0.3 | 1.224 | 396.5 to -395.8 | 361.6 | -77.01 | 1.0496 | 1.165 | -138.555 | 288.555 |
| | | | 181.0 180.6 | | | -4.846 -4.866 | | |
| 0.4 | 2.123 | 366 to -366 | 344.4 | -80.02 | 1.19091 | 740.7 | -145.8 | 295.8 |
| | | | 172.3 172.1 | | | -5.274 -5.286 | | |
| 0.5 | 2.735 | 337.5 to -337.9 | 326.2 | -80.50 | 1.41426 | 269.9 | -147.734 | 297.734 |
| | | | 163.3 162.9 | | | -5.740 -5.761 | | |
| 0.6 | 3.141 | 295 to -294.5 | 289.0 | -79.97 | 1.68951 | 782.3 | -147.634 | 297.634 |
| | | | 144.7 144.3 | | | -6.790 -6.816 | | |
| 0.7 | 3.404 | 250.5 to -250.8 | 246.8 | -78.83 | 1.97745 | -2.154 | -146.509 | 296.509 |
| | | | 123.6 123.2 | | | -8.162 -8.187 | | |
| 0.8 | 3.578 | 210.5 to -211 | 208.3 | -77.54 | 2.25122 | -3.625 | -145.089 | 295.089 |
| | | | 104.4 103.9 | | | -9.628 -9.664 | | |
| 0.9 | 3.696 | 176.9 to -177 | 175.2 | -76.44 | 2.50185 | -5.131 | -143.812 | 293.812 |
| | | | 87.78 87.38 | | | -11.13 -11.17 | | |

Figure 5 shows the differential output oscillation for the control voltage $V_{con}$ = 0.6 V, where Figure 6 represents phase noise vs frequency offset for tuning voltages of 0.3 V, 0.6 V and 0.9 V and the phase noises are -77.01, -79.97 and -76.44 dBc/Hz at 1 MHz offset respectively. Figure 7 shows the variation of tuning frequency with the change of tuning voltage. The accieved frequency range is 1.22 to 3.7 GHz.

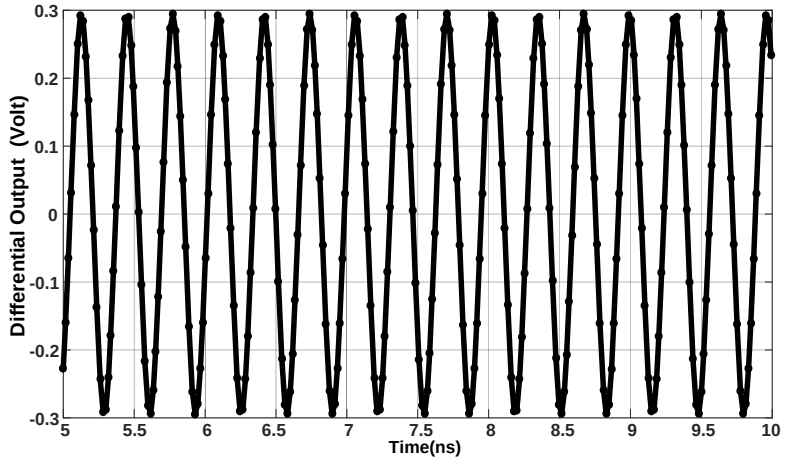


Figure 5. Differential output oscillation for tuning voltage $V_{con}$ = 0.6 V

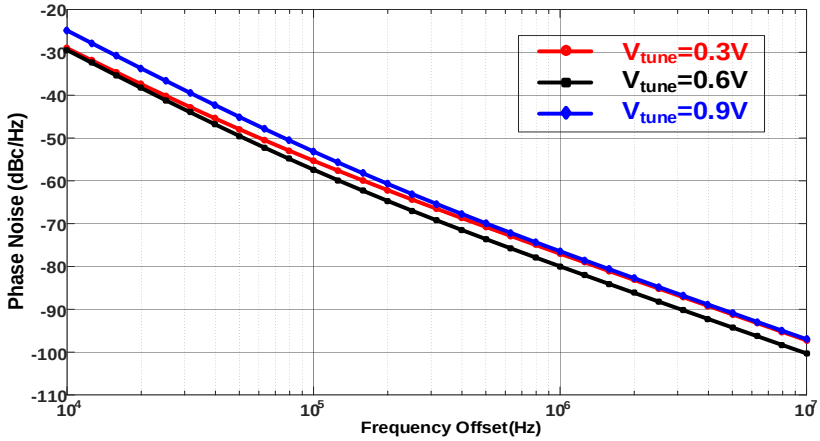


Figure 6. Phase noise vs frequency offset for various tuning voltage

A performance parameter, Figure of merit defined by (6), considering phase noise, dc power consumption and oscillation frequency which is depicted in Figure 8 with the variation of tuning voltages. The plot shows that the Figure of merit (FOM) is almost constant with the alteration of oscillator's oscillation frequency which is the outcome of the proposed design. The Figure of merit can also be defined in terms of dBF which is given by (7) [20].

$$FOM(dBF) = 20\log(freq) - phase\ noise - 10\log(P_{diss}) \quad (7)$$

Finally, the main contribution of the proposed VCO is the elimination of MOS varactors which are used for the tuning purpose. MOSFET with shorted drain, source and body can be used as capacitor. The change of the gate voltage of MOSFET results in the change of the capacitance of this MOS varactor. To achieve higher value of capacitance, we have to multiply the number of MOS which ultimately increases the silicon area consumption. So, the elimination of MOS varactor, under some conditions can be possible, if high tuning range can be achieved. But tuning of the inductor engenders the variation of performance parameter such as dc power consumption, phase noise and ultimately the Figure of merit. The data table and the plots presented clearly point out that the variations are highly limited. After all, reduction of the silicon area consumption by eliminating MOS varactor and at the same time the limitation of variation of performance parameters are the yielding of the proposed design which outdoes the other designs as referred in Table 5.

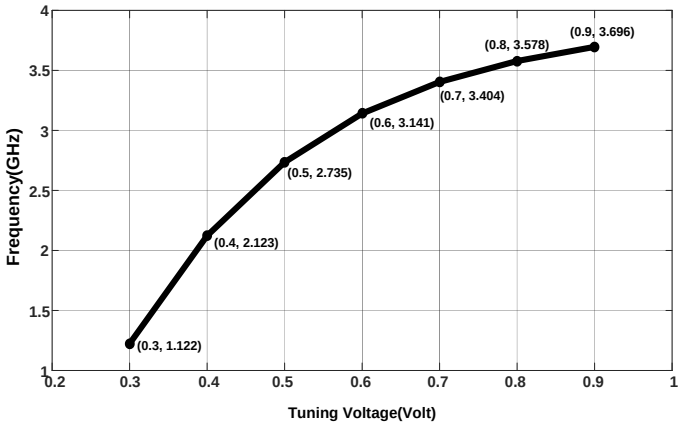


Figure 7. Frequency vs tuning voltage for the proposed VCO

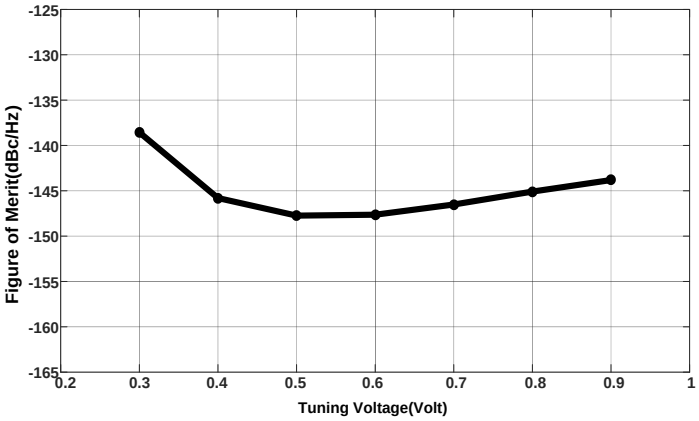


Figure 8. Figure of merit (FOM) vs tuning voltages for the proposed VCO

Table 5. Performance comparison of VCO with other designs

| References | [21] | [22] | [23] | [24] | [25] | This work |
|---|---|---|---|---|---|---|
| CMOS Technology | 180 nm | 180 nm | 180 nm | 180 nm | 130 nm | 90 nm |
| Supply Voltage (V) | 1.8 | 1.8 | 1.8 | 1.8 | 1.2 | 1 |
| Power (mW) | 44.6 | 16.27 | 29.38 | 11.9 | 3.2 | 1.05~2.5 |
| Tuning Range (GHz) | 1.26~2.98 | 0.1~2.5 | ---- | 0.55~3.8 | 1.913~2.491 | 1.22~3.69 |
| Tuning Range (%) | 81.13 | 184.6 | ---- | 149 | 26.24 | 100.5 |
| Output Power(dBm) | -5.3~-18.7 | 5~15 | 0.21 @ 5.5GHz | 3~-11 | ---- | 1.16~5.13 (differential) |
| PN@1MHz (dBc/Hz) | -90 | –93~-80 | -80.31 | -89~-78 | -80.23 | -80.50 @ 2.74 GHz |
| FOM (dBc/Hz) @1MHz | -141.11 @ 2.4 GHz | -120.88~ 135.84 | -140.43 @ 5.5 GHz | -133.5~ -138.84 | -140.81~ -143.106 | -147.734 @ 2.74 GHz |

## 6. CONCLUSION

A low power tunable active inductor based voltage controlled oscillator for wireless applications has been proposed in this research which provides a tuning range of 1.22 GHz to 3.7 GHz having a tuning scope of 100.5%. The proposed VCO exihibts low dc power dissipation characteristics (1.05~2.5) mW with the change of tuning voltages (0.3~0.9) V along with a good differential output power of (1.17~-5.13) dBm. Furthermore, elimination of MOS varactor which has been achivevd by tuning the inductance only, has faciliated the way to reduce the silicon area consumption. Low power consumption, stabilty of performance parameters and finally the good Figure of merit (FOM) are the specific outcomes of the proposed design which outperform the other referred designs.

**REFERENCES**


[1] K. N. Minhad, Z. Kazemi, M. Bin Ibne Reaz, J. Jalil, and N. Kamal, "Design of a Current Starved Ring Oscillator Based VCO for Phase-Locked Loop," *TELKOMNIKA (Indonesian Journal of Electrical and Engineering)*, vol. 12, no. 9, pp. 6667-6672, 2014.

[2] S. Suman, K. G. Sharma, and P. K. Ghosh, "Design of PLL using improved performance ring VCO," *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, Chennai, 2016, pp. 3478-3483.

[3] X. Zou, X. Jiang, D. Xiao, and S. Liu, "Wide capture range PLL with LC-VCO," in *2005 IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications*, Beijing, vol. 2, pp. 953-956, 2005.

[4] D. Halder and A.K. Gupta, "Ultra low power ring VCO based tuneable signal generator for neural stimulation," *2015 4th International Conference on Reliability, Infocom Technologies and Optimization (ICRITO) (Trends and Future Directions)*, Noida, pp. 1-6, 2015.

[5] M. Siripruchyanun and P. Wardkein, "A temperature-insensitive VCO and derivative PWM signal generator," in *ASICON 2001. 2001 4th International Conference on ASIC Proceedings (Cat. No.01TH8549)*, Shanghai, China, pp. 224-227, 2001.

[6] G. Blasco, E. Isern, and E. Martin, "Design of a stable pulse generator system based on a Ring-VCO Phase-Locked Loop using 180nm CMOS technology," *2015 Conference on Design of Circuits and Integrated Systems (DCIS)*, Estoril, pp. 1-6, 2015.

[7] D. Raiteri, P. V. Lieshout, A. V. Roermund, and E. Cantatore, "An organic VCO-based ADC for quasi-static signals achieving 1LSB INL at 6b resolution," *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, pp. 108-109, 2013.

[8] J. Park, H. Ryu, and D. Baek, "77 GHz signal generator with CMOS technology for automotive radar application," in *2011 International SoC Design Conference*, Jeju, pp. 444-445, 2011.

[9] W. Lai, J. Huang, C. Hsu, and P. Yang, "Low Power VCO and Mixer for Computing Miracast and Mobile Bluetooth Applications," *2014 International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery*, Shanghai, pp. 425-428, 2014.

[10] Y. Zhou, Z. Cheng, K. Fu, J. Li, and X. Zhou, "Design of low phase noise LC VCO for UHF RFID reader," *2009 15th Asia-Pacific Conference on Communications*, Shanghai, pp. 414-417, 2009.

[11] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 245-252, Jan 2017.

[12] M. T. Amin, "On the selection of passive elements for low phase noise LC tank VCO in 65 nm process," *2016 3rd International Conference on Electrical Engineering and Information Communication Technology (ICEEICT)*, Dhaka, pp. 1-5, 2016.

[13] M. Hsu, R. Jhong, and Y. Lee, "Phase noise reduction of CMOS VCO based on cross-coupled topology with shunt capacitor," *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Singapore, pp. 586-589, 2015.

[14] M. M. Reja, I. M. Filanovsky, and K. Moez, "Wide tunable CMOS active inductor," *Electronics Letters*, vol. 44, no. 25, pp. 1461-1463, 4 December 2008.

[15] R. Mehra and R. C. Gurjar, "LC VCO Using Active Inductor for Low Phase Noise and Wide Tuning Range," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 5, no. 7, pp. 13345-13350, July 2016.

[16] K. Manetakis, S. Park, A. Payne, and S. Setty, A. Thanachayanont and C. Toumazou, "Wideband CMOS analog cells for video and wireless communications," *Proceedings of Third International Conference on Electronics, Circuits, and Systems*, Rodos, Greece, vol. 1, pp. 227-230, 1996.

[17] J. Liang, C. Ho, C. Kuo, and Y. Chan, "CMOS RF band-pass filter design using the high-quality active inductor," *IEICE Trans. on Electron*, vol. E88-C, no. 12, pp. 2372–2376, Dec 2005.

[18] F. Yuan, *CMOS Active Inductors and Transformers*, 1st ed. United States: Springer, 2008.

[19] M. B. I. Reaz, M. A. M. Ali, T. G. Chang, and J. Jalil, "A Low Power 3-Stage Voltage-Controlled Ring," *Elektronika Ir Elektrotechnika*, vol. 19, no. 8, 2013.

[20] T. I. Ahrens and T.H. Lee, "A 1.4-GHz 3-mW CMOS LC low phase noise VCO using tapped bond wire inductances," *International Symposium on Low Power Electronics and Design*, Monterey, pp. 16-19, 1998.

[21] J. T. Yang, S. K. Hsieh, and P. J. Tsai, "A Wide Tuning Range Voltage-Controlled Oscillator with Active Inductors for Bluetooth Applications," *CSS'10 Proceedings of the 4th international conference on Circuits, systems and signals*, pp. 39-42, 2010.

[22] H. B. Kiaa, A. K. A'aina, and I. Groutb, "Wide tuning-range CMOS VCO based on a tunable active inductor," *International Journal of Electronics*, vol. 101, no. 1, pp. 88-97, December 2014.

[23] N. C. Shirazi, E. Abiri, and R. Hamzehyan, "A 5.5 GHz Voltage Control Oscillator (VCO) with a Differential Tunable Active and Passive Inductor," *International Journal of Information and Electronics Engineering*, vol. 3, no. 5, pp. 493-497, September 2013.

[24] A. Saberkari and S. Seifollahi, "Wide tuning range CMOS Colpitts VCO based on tunable active inductor," *Majlesi Journal of Telecommunication Devices*, vol. 1, no. 1, pp. 11-15, March 2012.

[25] Ghorbel, F. Haddad, W. Rahajandraibe, H. Barthélemy, M. Loulou, and H. Mnif, "Design and implementation of an active inductor-based LC oscillator," *ICM 2011 Proceeding*, pp. 1-4, 2011.