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A temperature characterization of (Si-FinFET) based on channel oxide thickness

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Abstract

This paper presents the temperature-gate oxide thickness characteristics of a fin field-effect transistor (FinFET) and discusses the possibility of using such a transistor as a temperature nano-sensor. The investigation of channel oxide thickness–based temperature characteristics is useful to optimized electrical and temperature characteristics of FinFET. Current–voltage characteristics with different temperatures and gate oxide thickness values (T_{ox}=1, 2, 3, 4, and 5 nm) are initially simulated, and the diode mode connection is considered to measure FinFET's temperature sensitivity. Finding the best temperature sensitivity of FinFET is based on the largest change in current (∆I) within a working voltage range of 0–5 V. According to the results, the temperature sensitivity of FinFET increases linearly with oxide thickness within the range of 1–5 nm, furthermore, the threshold voltage and drain-induced barrier lowering increase with increasing oxide thickness. Also, the subthreshold swing (SS) is close to the ideal value at the minimum oxide thickness (1 nm) then increases and diverges with increasing oxide thickness. So, the best oxide thickness (nearest SS value to the ideal one) of FinFET under the conditions described in this research is 1 nm.

Keywords*: FinFET, nano-sensor, oxide thickness, temperature*

1. Introduction

Many new field-effect transistor (FET) structures have been extensively explored [1-6] because metal oxide semiconductor FET (MOSFET) technology is approaching its downscaling limits. One of the relatively new FETs is the fin field-effect transistor (FinFET) as shown Figure 1 [7], a transistor-structured FET that is a popular research subject in the academe and semiconductor industry [8-10]. The ideal example of sensors for subsumed electronic applications (i.e., used within equipment) is the semiconductor temperature sensor [11-15]. Transistor-based temperature sensors are designed based on the temperature characteristics of the current–voltage (I–V) curves of FinFET transistors [16-20]. A bipolar transistor can be utilized as a temperature sensor by connecting its base and collector and operating them in diode mode. Similarly, a transistor with a MOSFET structure can be used as a temperature sensor by connecting oxide thickness to either the source or drain as shown in Figure 2. Electronic devices with nano-dimensions, such as diodes, transistors, capacitors, and resistors, have recently become popular in the electronics industry due to their extremely small electronic circuits.

The performance of new devices, which may correspond to various new applications, commonly depends on the nano-dimensional characteristics of such devices. The chip generation of these relatively new and powerful electronic devices with ultra-small transistors may even be regarded as trustworthy if new findings from future research are consolidated. However, new nano-dimensional FET designs and structures are still novel technologies and thus necessitate additional studies and improvements. Moreover, they require further innovations despite the limitations in MOSFET science.

Electronic device simulation has become increasingly important in understanding the physics behind the structures of new devices. Thus, simulation tools were adopted in this research for the analysis and evaluation of the performance limits of FinFET structures. Experimental work can be supported by simulation tools to explore further the development of

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multiple-gate field-effect transistors (MuGFETs) for nano-dimensional characterization [21]. Simulation tools can also help identify device strengths, weaknesses, and retrenchment costs and illustrate the extensibility of these devices in the nm range [22, 23].

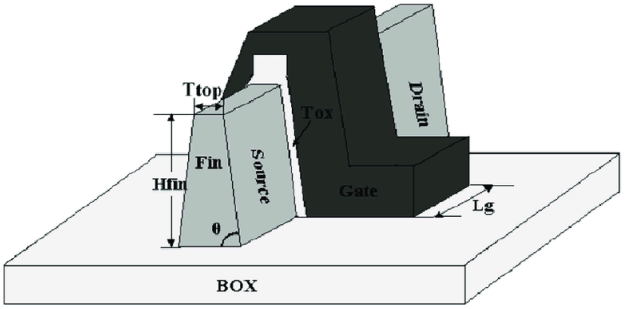

Figure 1. FinFET structure [7]

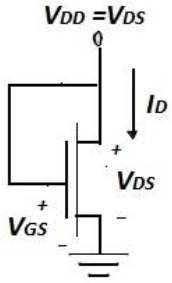

Figure 2. MOSFET as a temperature sensor (Vg=Vd=V_{DD})

2. Results and Discussion

In this research, MuGFET was utilized as the simulation tool to investigate the characteristics of FinFET. The output characteristic curves of the transistor under different conditions and parameters were considered. The effects of varying temperature and oxide thickness values on FinFET were determined based on the I–V characteristics derived from the simulation. The MuGFET [24, 25] simulation tool used for FET with a nano-dimensional structure was developed and designed by Purdue University.

MuGFET adopts either PADRE or PROPHET for simulation, both of which were developed by Bell Laboratories. The PROPHET is a partial differential equation profiler for one, two, or three dimensions, and PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry [24, 25]. The software can generate useful characteristic FET curves for engineers to help them fully explain the underlying physics of FETs. MuGFET also provides self-consistent solutions to Poisson and drift-diffusion equations [24, 25] and can be used to simulate the motion of transport objects when calculating FinFET characteristics as shown in Figure 1 [25].

In this research, the Id–Vg characteristics of FinFET at different temperatures of 250, 275, 300, 325, 350, 375, and 400 K were simulated with the following parameters: channel width = 40 nm, channel concentration (P-type) =10^{16} cm^{-3}, source and drain lengths = 50 nm, source and drain concentrations (N-type)=10^{19} cm^{-3}, and channel length=85 nm. The oxide thickness values were T_{ox}=1, 2, 3, 4, and 5 nm. The change in current (∆I) have been calculated when the temperature increased in the V_{DD} range of 0–5 V at 0.25 V steps for T_{ox} values of 1, 2, 3, 4, and 5 nm. The ∆I was calculated depending on the relation:

$$\Delta I(T_{n+1}, Tox) = I(T_{n+1}, Tox) - I(T_n, Tox) \quad (1)$$

the maximum sensitivities (with max ∆I) became evident to relatively low temperatures, and the values decreased linearly as temperature increased for all V_{DD}. The calculations of ∆I show that the maximum temperature sensitivity values at V_{DD}=2 V (with T_{ox}=1 nm), V_{DD}=2.75 V (with T_{ox}=2 nm), V_{DD}=3.75 V (with T_{ox}=3 nm) and V_{DD}=4.75 V (with T_{ox}=4 nm), and V_{DD}=5 V (with T_{ox}=5 nm).

Figure 3 presents the optimized operating voltage $V_{DD(opt)}$ based on the maximum temperature sensitivity and oxide thickness, in which the optimized V_{DD} is related to the temperature sensitivity peaks. Temperature sensitivity increased remarkably until oxide thickness reached 4 nm then increased only slightly from 4 to 5 nm. Hence, a linearly increasing relationship was observed between temperature sensitivity and oxide thickness up to about 5 nm.

Figure 4 presents the threshold voltage (V_T), subthreshold swing (SS), and drain-induced barrier lowering (DIBL) of FinFET. These temperature characteristics were obtained at T=250, 275, 300, 325, 350, 375, and 400 K at T_{ox}=1 nm. As presented in this figure,

V_T decreased linearly with increasing temperature, such that V_T=0.48 V at a low temperature of 250 K and V_T=0.44 V at a high temperature of 400 K. SS began at 56.63 mV/dec at the lowest temperature (the nearest value to the ideal SS at 49.6 mV/dec) at 250 K and increased until it reached 94.88 mV/dec (the farthest value from the ideal SS at 79.4 mV/dec) at 400 K. DIBL increased as temperature increased. Figure 5 presents the V_T, SS, and DIBL of FinFET. These temperature characteristics were obtained at T=250, 275, 300, 325, 350, 375, and 400 K at T_{ox}=2 nm. V_T decreased linearly with increasing temperature. Hence, V_T=0.49 V at a low temperature of 250 K and V_T=0.45 V at a high temperature of 400 K. SS began at 60.12 mV/dec at the lowest temperature (the nearest value to the ideal SS at 49.6 mV/dec) at 250 K and increased until it reached 102.34 mV/dec (the farthest value from the ideal SS at 79.4 mV/dec) at 400 K. DIBL increased as temperature increased.

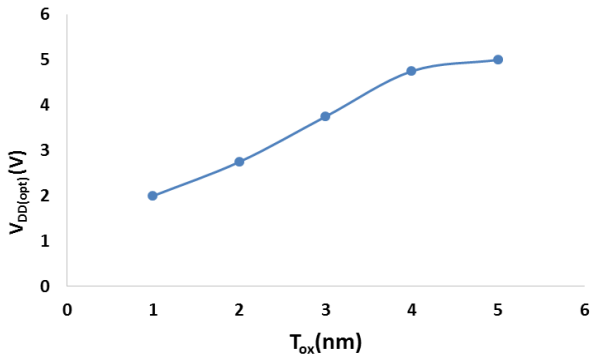

Figure 3. Optimized operating voltage V_{DD} with different oxide thickness values on the basis of the best temperature sensitivity

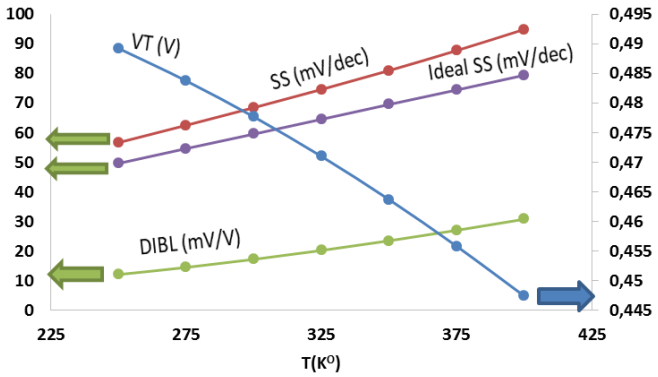

Figure 4. V_T, SS, and DIBL at T_{ox} = 1 nm

Figure 6 illustrates the V_T, DIBL, and SS[characteristics of the FinFET at T=250, 275, 300, 325, 350, 375, and 400 K at T_{ox}=3 nm. Temperature increased with oxide thickness. This linear relationship implies that fat reduces fermentation from 250 K to 400 K. Hence, at 250 K and 400 K, V_T=0.49 and 0.45 V, SS=63.95 and 110.90 mm/dec, and DIBL=54.73 and 60.23 mm/V, respectively. In addition, when temperature increased to 400 K, SS=63.95 mm/dec, which approached the ideal SS=49.6 mm/dec. Figure 7 presents the changes in V_T, SS, and DIBL and their effects on FinFET properties when temperature was increased from 250 K to 400 K at T_{ox}=4 nm. V_T decreased linearly with increasing temperature. Hence, for 250 K and 400 K, V_T=0.49 and 0.45 V, SS=69.20 and 120.44 mV/dec, and DIBL=103.06 and 79.4 mV/V, respectively. The figure also illustrates that the obtained value, SS=69.20 mV/dec, is close to the ideal SS = 49.6 mV/dec at 400 K.

Figure 8 shows the change in V_T, SS, and DIBL and their effect on FinFET properties when temperature was increased from 250 K to 400 K at T_{ox}=5 nm. V_T, SS, and DIBL decreased

with increasing temperature. This figure particularly presents the limits of the decrease from 250 K to 400 K. Hence, for 250 K and 400 K, V_T=0.50 and 0.46 V, SS=72.43 and 130.91 mV/dec, and DIBL=139.52 and 97.11 mV/V, respectively. By contrast, the SS values decreased with increasing temperature until they approached the ideal values. Figure 9 presents the properties of V_T, SS, and DIBL with increasing oxide thickness of FinFET at T=300 K, with 1–5 nm at 1 nm steps, V_T increased hyperbolically, DIBL increased exponentially, and SS increased linearly with increasing oxide thickness. SS was close to the ideal value at 1 nm, beyond which it increased with increasing oxide thickness. So, according to these results, the best oxide thickness of FinFET under the conditions described in this research is 1 nm.

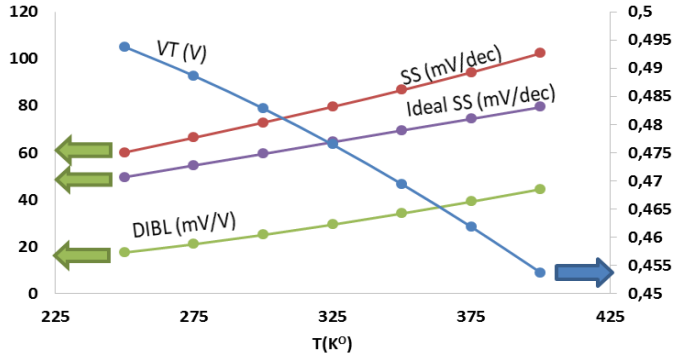

Figure 5. V_T, SS, and DIBL at T_{ox} = 2 nm

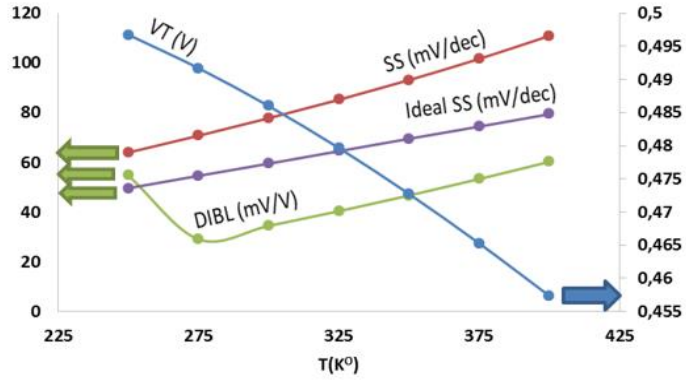

Figure 6. V_T, SS, and DIBL at T_{ox} = 3 nm

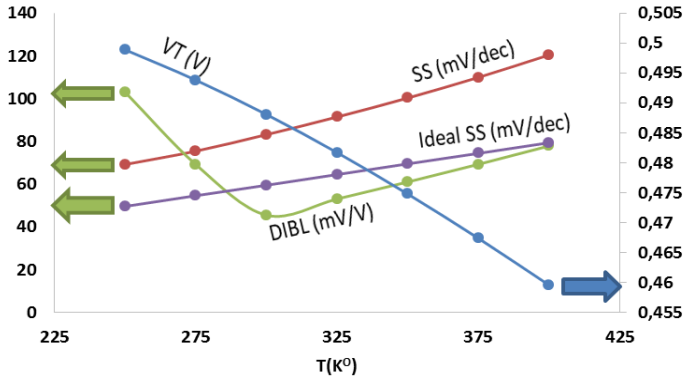

Figure 7. V_T, SS, and DIBL at T_{ox} = 4 nm

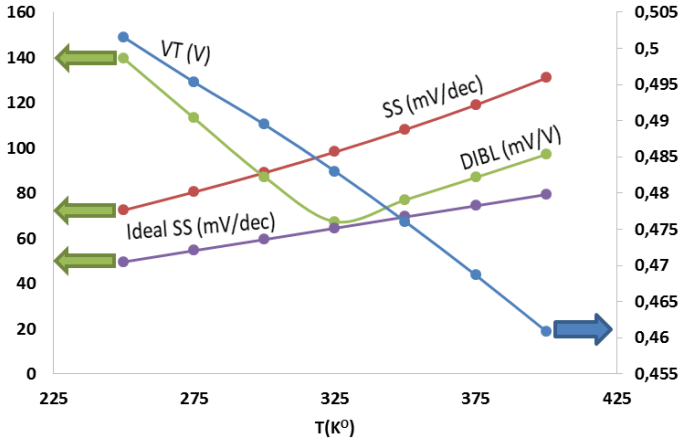

Figure 8. V_T, SS, and DIBL at T_{ox} = 5 nm

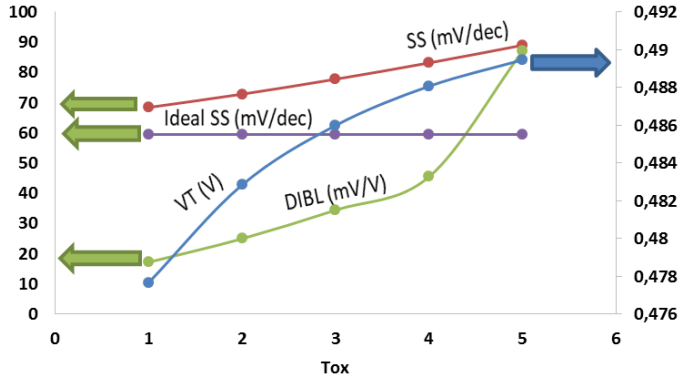

Figure 9. VT, SS, and DIBL characteristics T_{ox}

3. Conclusion

The effects of working temperatures (250, 275, 300, 325, 350, 375, and 400 K) on FinFET characteristics were studied by considering different oxide thickness values (T_{ox}=1, 2, 3, 4, and 5 nm). According to the results of optimized operating voltage V_{DD} with respect to the best temperature sensitivity and oxide thickness, temperature sensitivity increased remarkably until oxide thickness reached 5 nm, then increased only slightly from 4 to 5 nm oxide thicknesses. Hence, a linearly increasing relationship was not observed between temperature sensitivity and oxide thickness beyond 5 nm. V_T increased hyperbolically, DIBL increased exponentially, and SS increased linearly with increasing oxide thickness of FinFET from 1–5 nm at 1 nm steps. SS was close to the best value at 1 nm then increased with increasing oxide thickness. Therefore, the ideal oxide thickness (low SS) of FinFET under the conditions described in this research is 1 nm. The best oxide thickness of FinFET with excellent V_T, DIBL and SS under the conditions described in this research is 1 nm.

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