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A new factor for fabrication technologies evaluation for silicon nanowire transistors

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ABSTRACT

This paper reviews the fabrication technologies of silicon nanowire transistors (SiNWTs) and rapidly development in this area, as this paper presents various types of SiNWT structures, development of SiNWT properties and different applications until nowadays. This research provides a good comparison among fabrication technologies of SiNWTs depending on a new factor DIF, this factor depends on the size of channel and power consumption in channel. As a result of this comparison, the best technology to use in the future to fabricate silicon nano transistors for future ICs is AFM nanolithography.

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1. INTRODUCTION

Nowadays, nanowires have many applications in nanoelectronics engineering. The structure of nanowires includes rectangular or circular cross-sectional nanostructure with a diameter (or thickness) of tens of nanometers or less. There are many types of existing nanowires depending on its materials, such as semiconducting, insulating, and metallic nanowires for different applications of electronic devices. These types are important for nanoelectronics devices applications. In research of nanoelectronic fields, active devices in nano dimension fabricated with semiconducting nanowires [1], the nano-capacitors fabricated using an insulating nanowire, and the contacts among nano devices depends on metallic nanowires.

The electronics industry has been focused on the Si nanowires because of its ability to lead the progress of ever-smaller electronic devices, such as capacitors, resistors, diodes, and transistors. The characteristics of all of these nanodevices with broad types of new applications will be based on the characteristics of the main unit of these nanodevices which is nanowire. Si nanowire transistors (SiNWT) will be more usable in the future after making its large amount of investigation of its characteristics by researchers. The researchers predicted that the future of electronics devices will highly depends on advancement in research of nano dimensional transistors as a roadmap [2-10].

Electronic engineering has played a significant function in the cognitive development of human beings in various fields of sciences and, most importantly, in the manufacturing evolution of integrated

circuits (ICs). The latter occurred as a result of the revolution in the minimization of transistors, the basic unit of the IC chips, which have emerged in the tens nanometer or less. According to the international technology roadmap for semiconductors (ITRS), the number of transistors in ICs quadrupled every three years with the size of the transistor shrinking to half [11].

Nanowires are still under research and experimental fields in laboratories. A number of early studies have shown how nanowires can be used to build the next generation of electronics devices [12]. In order to create active electronic devices, an important step is to dope a semiconductor nanowire to create p-type and n-type semiconductors [13, 14]. This process has already been performed on individual nanowires. Over the last decade, there have been many researches focused on SiNWTs fabrication [15-18] with different parameters such as semiconducting materials, insulating materials and various fabrication technologies developed to predict the SiNWT performance.

Nanowires can be prepared for electronic device applications, like SiNWT, by catalyst-assisted growth technologies, electron beam lithography (EBL), and atomic force microscope (AFM) nanolithography to obtain a smallest dimension for silicon nanowire. The EBL can be prepared SiNWT by "top-down" approaches using advanced nano-lithographic technology tools [19] or by the technology of synthesis of semiconductor nanowires using "bottom-up" approaches, such as the vapor–liquid–solid (VLS) growth technique [20]. These technologies need to evaluate based on the improvements of the characteristics and the minimum size of the SiNWT. So, this paper reviews the fabrication technologies of silicon nanowire transistors (SiNWTs) and rapidly development in this area, as this paper presents various types of SiNWT structures, and also suggests a new factor to evaluate these technologies depending on the better characteristics with minimal size.

2. FABRICATION TECHNOLOGIES

SiNWTs could be fabricated by either top–down method using advanced lithography tools like deep UV steppers [21, 22] and electron beam lithography [23], or bottom-up methods with catalyst-assisted growth [24-26].

2.1. Catalyst-assisted growth technologies

The vapor liquid solid (VLS) technique has beed explained firstly by Wagner and Ellis [27]. The VLS is consedered as the most general method of manufacturing involves the chemical vapor deposition (CVD) of a gas including silicon and the following growth of silicon nanowires. Au catalyst and Silane gas has been used to growth the Si nanowires at low temperature of 300-600 ^{o}C depending on VLS technique. This method will depend on the silane gas decomposition at low temperature [28-30]. The metal catalyst droplet has been appeared on top end on the Si nanowires as a result of VLS technique [31].

The mechanism that has been excessively used in the fabrication of amorphous and nanocrystalline silicon thin films is the plasma enhanced chemical vapor deposition (PECVD) mechanism. The production of Si nanowires depending on the PECVD technique [32] will be used with metal catalyst covered substrate at higher deposition rate [33]. PECVD has been improved to pulsed PECVD (PPECVD) which uses modulated plasma to support the deposition process. Parlevliet and Cornish [34, 35] group have shown that PPECVD technique could be produced Si nanowires at higher area density more than normal PECVD. The PPECVD grows Si nanowires using metal catalysts like Al, Ag, Cu, Au, Sn and In. According to the results of Parlevliet and Cornish [34, 35] group, the Ag was the best effective catalysts under conditions of growth temperatures, and also Ag catalysts could be produced Si nanowires with substrate coverage of seven to eight times greater than the other catalysts.

In the vapor liquid solid (VLS) technique, the main function of the metal catalyst is to induce the outgrowth of Si nanowires with single crystal. The important condition for Si to be growthed as a nanowire by the metal catalyst it must be quite soluble in the chosen metal. Furthermore, the metal catalyst must be chosen to impact the electrical characteristics of resulting nanowires [33, 35]. The metal induced growth (MIG) method provides nanowires without using a gas silicon source (silane) and Au catalyst. This has potential to use the nanowires as a 1-dimensional building block in nanoelectronics. The growth temperature of MIG nanowires of 575 ^{o}C is still a low temperature, competitive with other groups, without requiring silane and Au catalyst at 900-1200 ^{o}C [36-39] or using silane gas at 800 ^{o}C [40].

Doping SiNW can be done by vapor phase doping method after SiNW synthesis, to make n-type SiNW, phosphorus-doped into SiNW, and to make p-type SiNW, boron-doped into SiNW. Yi Cui et al. [41] reports boron-doped (p-type) SiNWs. A SiNWs single crystal with radius of 5-10 nm has been growth by a nanocluster mediated method. Later, the SiNWs were put onto Si substrates toped by 600 nm SiO_2 growthed by thermal oxidation. Yi Cui et al. [41] investigate the characteristics behavior of the SiNWT by testing the effect of source and drain contacts annealing and surface passivation on parameters of transistor

characteristics. The annealing process and chemical amendment for oxide defects passivation were lead to improve the average mobility from 30 to 560 cm^2/Vs and improve the average transconductance from 45 to 800 nS with maximum values of 1350 cm^2/Vs and 2000 nS, respectively. Comparison the results of transconductance, mobility and other important electrical characteristics of SiNWT with planar MOSFET shows essential merit for the SiNWs as structure units. The 5-10 nm radius boron-doped (p-type) SiNWs has been used in the study of Yi Cui et al., where the source and drain contacts were made using Ti metal. Figure 1 [41] illustrates the output characteristics of SiNWT (drain current (I) vs. source-drain voltage (V_{sd})) with Ti source and drain contacted with SiNW device after and before annealing. This figure shows that after annealing, the I-V_{sd} characteristics be more symmetrical and linear, 3-fold conductance increasing, and the behavior of transport were considered more stable.

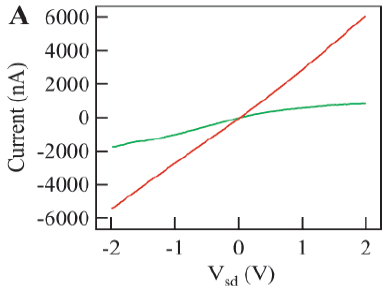


Figure 1. The output characteristics of SiNWT after (red) and before (green) thermal annealing [41]

J. Goldberger et al. [42] fabricated vertically oriented Si nanowires as shown in Figure 2 [42]. Figure 2 (A) shows the image of Si nanowires that grown vertically, and Figure 2 (B) illustrates the image of cross-section of Si nanowire coated by SiO_2 as an insulator. While Figure 2 (C) explains the high-resolution image of a Si nanowire with an inner reduced diameter to ≈ 4.5 nm. These nanowires were grown on degenerately boron-doped p-type ($\rho < 0.005$ Ω cm) Si (111) substrates as described in [43]. The wires were synthesized via the vapor-liquid-solid (VLS) growth mechanism in a chemical vapor deposition (CVD) reactor using a $SiCl_4$ precursor, a BBr_3 dopant source, and metal nanoparticle growth-directing catalysts. Figure 2 (A) is a scanning electron microscopy (SEM) image of Si nanowires grown from 50 nm Au colloids. Transmission electron microscopy (TEM) analysis confirmed that these nanowires are single crystalline and grow along the (111) direction. Si nanowire arrays grown by the above method exhibit narrow diameter distributions with standard deviations (typically ≤ 9%) equal to those of the colloid catalysts [42, 43]. As a good example for fabrication of SiNWT with top gate structure we can take [44], and Table 1 shows the fabrication summary of all layers of this SiNWT. Finally, the resulting SiNWT was annealed in ambient forming gas (5% H_2 in N_2) at 380 ºC for 15 minutes by using a rapid thermal annealing tool. This step is critical for achieving better electrical performance due to the following two reasons:

– The forming gas annealing can greatly reduce the nanowire device interface states, which can seriously deteriorate the device performance, such as the transistor subthreshold slope.
– To improve Al contact with nanowire.

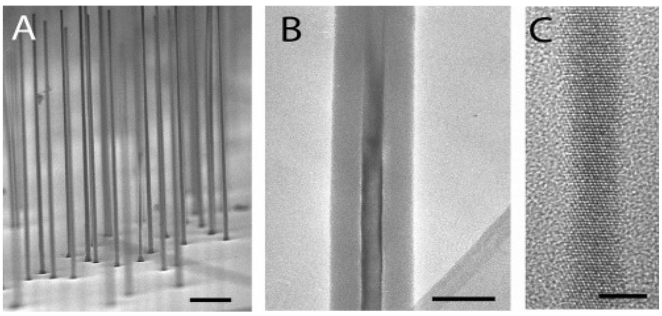


Figure 2. (A) Si nanowires that grown vertically, (B) cross-section of Si nanowire coated by SiO2, (C) Si nanowire with an inner reduced diameter to ≈ 4.5 nm [42]

Table 1. The fabrication summary of all layers of SiNWT

Layer	Dimensions	Conditions
Nanowire	20nm diameter 20 µm ~ 30 µm in length	420 ºC, under 500 mTorr SiH4 via a (VLS) mechanism
Oxide	1 nm ~ 2 nm	Thermally oxidized at 700ºC for 30 minutes
Source and drain electrodes	A layer of Al with spacing 3 µm	Deposited by thermal evaporation
Gate electrode	HfO_2 (~ 25 nm) Al top gate electrode	Atomic layer deposition at 250 ºC Deposited by thermal evaporation

The Al in the source/drain regions forms Schottky barrier contacts to the SiNWs. Figure 3 (a) shows the output characteristics of fabricated SiNWT with top gate structure. Figure 3 (b) display the scanning electron microscopic images of the fabricated SiN WT and the top gate is very clear in this image as explained in [44]. Improving the electrical characteristics of SiNWTs by minimizing contact resistance values has been studied by C. Celle et al. [45]. This will tend to enhance carrier injection by reducing the contact resistance values as a result of high doping at both ends of the Si nanowires. It is well recognized that for highly doped Si nanowires transistor, at transconductance measurement, the contact resistance will be neglected, while it makes an essential improvement for Si nanowire transistor with light doping. According to the study reported by C. Celle et al. [45], the VLS technique has been used in the synthesis of SiNWs. The SiNWs has been doped at the ends of nanowires only directly during the synthesis by adding 1% PH3 in hydrogen. The ratio of P:Si has been set to $2*10^{-2}$ for the doped ends of the NWs [46, 47]. Figure 4 shows the structure and image of a flexible Si nanowire transistor, where the axial doping of Si nanowires is in the form of n^{++}-i-n^{++}.

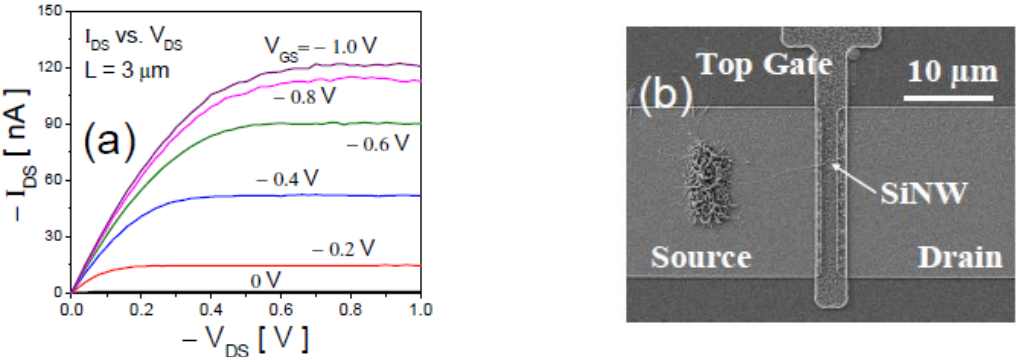


Figure 3. (a) Output characteristics of SiNWT,
(b) the images of (top gate) SiNWT with 1 µm gate-source/drain [44]

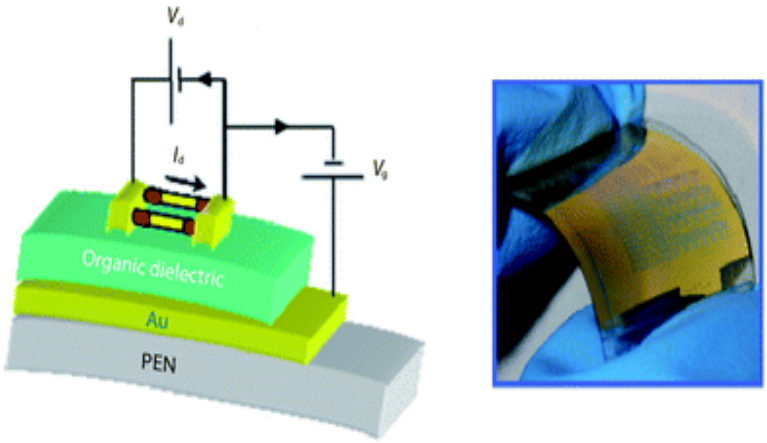


Figure 4. The structure and image of a flexible Si nanowire transistor,
the axial doping of Si nanowires with form n^{++}-i-n^{++} [45]

2.2. EBL technology

H. W. Yoon et al. [48] have been developed a new fabrication technology for SiNW FET for bio-sensing applications. Figure 5 (a) displays the structure of simple back-gate configuration SiNWT on silicon-on-insulator (SOI) substrate. This design is directed the fabrication process to be low cost. There are no source and drain doping, and also this design has no top metal contact to the back gate. The important key for this transistor is the manufacturing of Si nanowires. The fabrication processes of the Si nanowires have been conducted using two electron beam lithography (EBL). Nano dimensiontrenches in polymethyl methacrylate has been patterned using EBL, followed by liftoff process using Cr and then etching of Si by ICP plasma. Another alternative EBL procedure has been developed using hydrogen silsesquioxane (HSQ) resists. This EBL fabrication method produces SiNWTs with 12-50 nm diameters, 30-70 nm high, and 10 μm length Si nanowires on Silicon-on-insulator substrates, while the SiO_2 layer was about 140 nm. Figure 5 (b) illustrates the drain to gate current ratio (I_d/I_g) with gate voltage (V_g) characteristics of a fabricated SiNWT at V_{ds} bias of 6 V. For such SiNWTs that fabricated using EBL, the ON/OFF current ratio is of about 1000 and reasonable small gate leakage current is observed, while the conductance of the SiNWTs is about 10 nS.

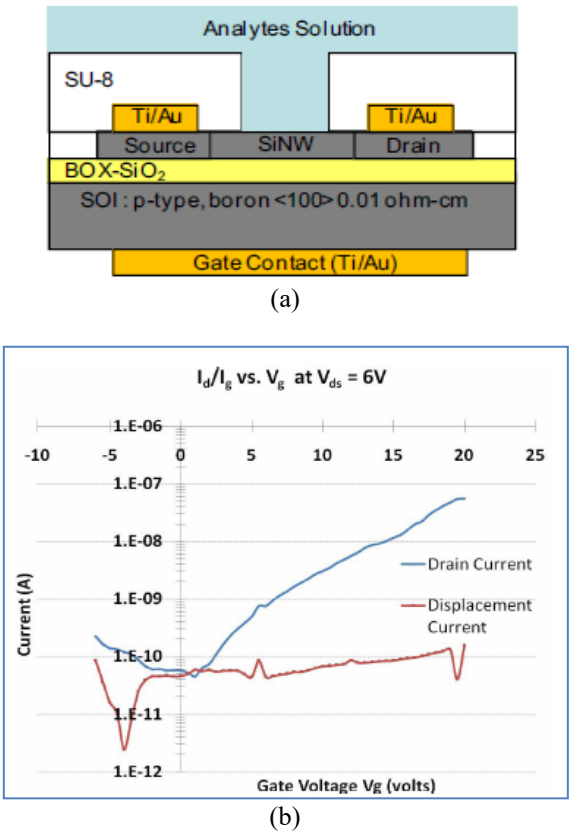
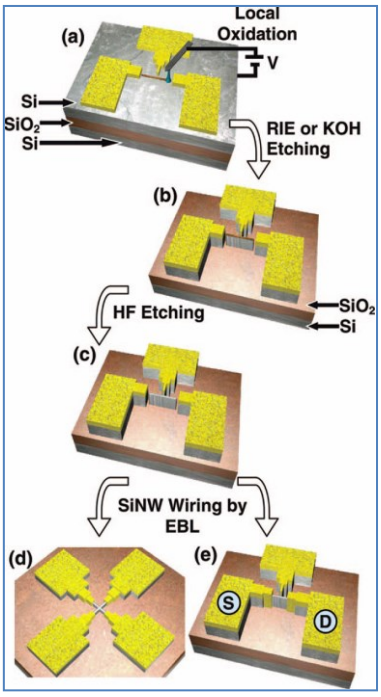


Figure 5. (a) SiNWTs on SOI substrate cross-section structure and (b) SiNWT drain to gate current ratio (I_d/I_g) with gate voltage (V_g) characteristics of a fabricated SiNWT at V_{ds} bias of 6 V [48]

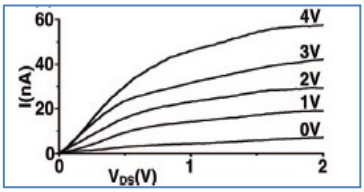
2.3. AFM technology

J. Martinez et al. [49] discusses the SiNWT with using another technology of atomic force microscope (AFM) nanolithography to obtain a smallest dimension (4 nm) for silicon nanowire. They investigate the fabrication of 4 nm channel width SiNWTs with AFM nanolithography depending on the local oxidation of a SOI surface with a range of resistivity (ρ) of 10-20 Ω cm. The atomic force microscope has been used to make a narrow mask of SiO_2 on top of a SOI substrate. The long and narrow sector of SiO_2 that represents mask has been fabricated by giving pulses of voltage between the probe of AFM and the surface of silicon. The pulses of voltage encourage the forming of water and later the anodic oxidation of the Si surface. The following step is etching of the unmasked silicon by either wet or dry chemical etching processes. After etching, the local oxide mask has been removed by HF, and then the metal contacts (platinum or gold) for source and drain of SiNWs has been formed by electron beam lithography.

Table 2 presents all main steps of atomic force microscope (AFM) nanolithography processes of SiNWT. Figure 6 (A) shows the fabrication steps of 4 nm channel width SiNWT using AFM nanolithography and Figure 6 (B) illustrates the output characteristics of the SiNWT with 4nm width of channel that fabricated by AFM nanolithography.



(A)



(B)

Figure 6. (A) The 4nm SiNWT fabrication steps using AFM,
(B) The output characteristics of the SiNWT with 4 nm width of channel [49] (continue)

Table 2. The main steps of atomic force microscope (AFM) nanolithography processes of SiNWT

Layer	Dimensions	Conditions
Nanowire	4 nm width, 55 nm high, 10 μm in length	AFM nanolithography followed by wet etching to form nanowire and side gate
Oxide	140 nm side gate gap	
Source and drain electrodes	A layer of gold	

3. COMPARISION AND RESULTS

As a result of many different factors among all technologies to fabricate the nanowire transistors, it is note that the difficulties to choose an accurate tool to measure and evaluate the best preference among all these nanowire transistors, we note that there is a difference in manufacturing technology, there is also a difference in the cross-section of nanowires. Since the main purpose of fabrication NWT with different technologies and scaling down nanowire transistors is the possibility of putting it into an electronic circuit in IC with the consumption of less value of power, and this tow principles has been chosen to develop a new measurement preference factor. This factor will show the ability of putting a transistor in ICs, this factor will call device integration factor (DIF).

Device integration factor (unit less) is proportional inversely with power dissipated in the channel (W_{ch}) and channel area (A_{ch}):

$$DIF \propto \frac{1}{W_{ch} * A_{ch}} \quad (1)$$

$$DIF = \frac{k}{W_{ch} * A_{ch}} \quad (2)$$

Power W_{ch} chosen to be at V_D=V_G=1 V as a reference voltage for all SiNWTs, and the power consumption in channel will be the current flow in channel I_D multiply by voltage across it V_D, then:

$$DIF = \frac{k}{I_D * V_D * A_{ch}} \quad (3)$$

We assumed that K constant will be calculated at DIF = 1 and at the following parameters: I_D = 1 μA, V_D = 1 V, D = 1 nm and L = 1 μm, then k will be: K=1*10^{-21} watt m^2.

DIF calculated for three transistors fabricated with three types of technology, first transistor had chosen from reference [44]. This device fabricated using VLS technology as mentioned in section 2.1, according to (3) the DIF for this device is 0.138. Second sample taken from reference [48], this transistor fabricated using EBL as mentioned in section 2.3, DIF for this devise is 0.833. The last sample fabricated using AFM lithography and DIF factor is 1.923 for this transistor from [49]. Table 3 concludes these results the last two columns are the important columns to make a comparison among these three technologies to fabricate SiNWTs, the best technology has an ability to fabricate SiNWT with an ability to be a part of an IC is AFM technology.

Table 3. Results comparison of SiNW fabrication technologies

SiNW fabrication technology	Structure features	Important improvement	DIF factor
(VLS) mechanism Down-up [44]	Top gate structure	Low temperature chemical vapor deposition (420ºC)	0.138
(EBL) top-down [48]	Back-gate structure	1-low cost fabrication process 2-the (ON/OFF) current ratio is about 1000	0.833
(AFM) top-down [49]	Side-gate structure	Smallest dimension (4nm) for silicon nanowire	1.923

4. CONCLUSION

This study is designed to review the most technologies that used to fabricate SiNWTs and make a comparison among these technologies, a new factor was invented to make this comparison depending on minimum size of device and minimum consumption power and this factor called DIF. The results show that the best technology to use in the future to fabricate silicon nano transistors for future ICs is AFM nanolithography.

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