TELKOMNIKA Telecommunication, Computing, Electronics and Control
Vol. 18, No. 1, February 2020, pp. 519~529
ISSN: 1693-6930, accredited First Grade by Kemenristekdikti, Decree No: 21/E/KPT/2018
DOI: 10.12928/TELKOMNIKA.v18i1.12440

PWM control techniques for three phase three level inverter drives

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Article Info

Article history:

Received Jan 26, 2019
Revised Jun 2, 2019
Accepted Jul 18, 2019

Keywords:

Multi-level converters
Neutral-point-clamped inverter
Space vector pulse width modulation
Three-level inverter

ABSTRACT

In this paper two very efficient pulse width modulation techniques were discussed named Sin pulse width modulation and space vector pulse width modulation. The basic structure of the three-level inverter neutral-point clamped is introduced and the basic idea about space vector pulse width modulation for three-level voltage source inverter has been discussed in detail. Nearest three vectors space vector pulse width modulation control algorithm is adopted as the control strategy for the three phase three level NPC inverter in order to compensate the neutral-point shifting. Mathematical formulation for calculating switching sequence has determined. Comparative analysis proving superiority of the space vector pulse width modulation technique over the conventional pulse width modulation, and the results of the simulations of inverter confirm the feasibility and advantage of the space vector pulse width modulation strategy over sin pulse width modulation in terms of good utilization of dc-bus voltage, low current ripple and reduced switching frequency. Space vector pulse width modulation provides advantages better fundamental output voltage and useful in improving harmonic performance and reducing total harmonic distortion.

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1. INTRODUCTION

Multilevel inverter topologies [1, 2] have got special attention during the earlier two decades due to their significant advantages compared to the classical two level inverters. As compared with two-level inverters, multilevel inverters have multiple advantages, for example, low harmonics in output voltages and current, less dv/dt, lower power losses across switching devices, less common mode voltages, and higher quality output waveform [3-7]. Therefore a new family of multilevel inverters has emerged as the solution for different applications; such as, AC power supplies, large powerful engine drivers, transmission, distribution systems and medium voltage grid [8-12].

Different types of topologies of power conversion have been proposed with the aim of improving the total harmonic distortion (THD) and efficiency, and reducing the complexity of control. The most known are: cascaded H-bridge (CHB) inverter, flying-capacitors (FC) converter, packed U cells, [13-16] and neutral point clamped (NPC) inverter [1]. This paper uses the NPC topology because it has the advantages such as: low switching frequency, DC-link capacitors are common to three phases and reactive current can be controlled [14]. The diode-clamped three level neutral-point clamped (NPC) topology has been the most

widely used one among all multilevel inverter topologies due to their use of a unique DC source of voltage compared with the CHB inverters and higher performance when compared to the FL inverters [17, 18].

On the other hand, several methods of modulation techniques have been proposed for this type of converter. The most known techniques are: selective harmonic elimination pulse width modulation (PWM), sinusoidal PWM with and without harmonic injection**,** space vector modulation, sigma delta PWM, and closed loop modulation techniques exist to control the inverter [19-22]. Among the possible multilevel topologies, the sine triangle PWM (SPWM) and space vector PWM (SVPWM) are probably the most popular modes and the most common PWM generation techniques for three-level three-phase multilevel inverters. The SVPWM is basically divided into two classifications: the nearest three vectors (NTV) method and the Hexagons method. The SVPWM includes the reference voltage space vector synthesis for the NTV approach, by switching between the nearest three voltage space vectors [23-26]. The output voltage vector is synthesized for the hexagon's approach using a method similar to the traditional two-level converter.

This paper modeling and simulation of a three-level NPC inverter have been performed with SPWM and SVPWM techniques using MATLAB/Simulink software. The results of the comprehensive comparison are presented in two ways. This paper will be divided into six sections. A brief review of the three level NPC inverter is provided in section 2. Sections 3 describes the three level PWM techniques. The proposed three-level space voltage vector algorithm has given in section 4. Section 5 will perform the simulation successively. Finally, at the end of this paper, a general conclusion is given.

2. THREE-LEVEL DIODE-CLAMPED INVERTER TOPOLOGY

Figure 1 shows the three-phase three-level diode-clamped inverter (NPC) topology. From Figure 1, each phase of the inverter shared the DC-link supply. The center of each phase is connected to the common point of the series capacitors. The inverter is feeding an AC a three-phase load. Three-level output consisting of levels -Vdc, 0, + Vdc depending on the DC-bus voltage. Table 1 shows the functioning principle. In order to obtain the desired three-level voltages, the converter must ensure complementarities between the pairs of switches: (S_{i1},S_{i4}) and (S_{i2},S_{i3}) where 'i' is the phase indicator (i = a, b, c), Vio is the phase-to-fictive middle point voltage. Table 1 shows switching of the i-phase in Figure 1 with switching states and corresponding output voltage levels.

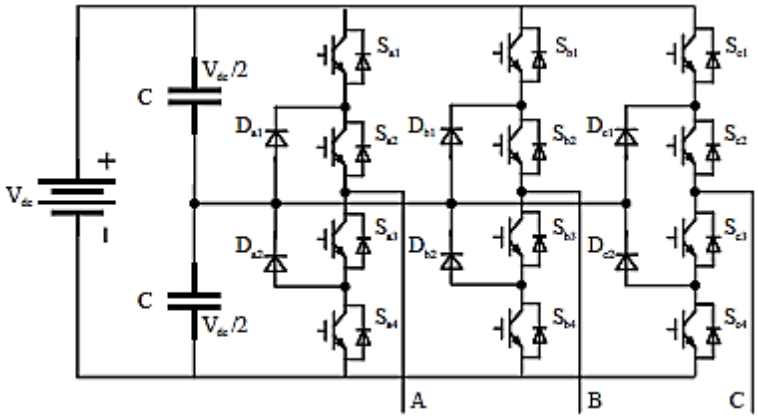


Figure 1. Three-phase three-level NPC inverter circuit

Table 1. Relationship between switching devices and output level

Switching Situations	i-phase of NPC inverter				Terminal Voltage
	Si1	Si2	Si3	Si4	
P	1	1	0	0	+Vdc /2
O	0	1	1	0	0
N	0	0	1	1	-Vdc /2

3. THREE-LEVEL PWM TECHNIQUES

In many applications, the output voltage of the inverter is often required to vary due to the following reasons:

- To compensate the input voltage variations.
- To compensate for the regulation of the inverters.
- For the provision of special loads that will need variation of voltage with frequency.

3.1. Sinusoidal pulse width modulation technique

The principle of the sinusoidal carrier-based pulse width modulation (SPWM) technique; a high-frequency triangular carrier wave V_r is compared with a sinusoidal control signal V_c at the desired frequency. The intersection of V_c and V_r waves determines the switching instants and commutation of the modulated pulse. A transition in PWM waveform is generated at each compare match point. When sinusoidal wave has magnitude higher than the triangular wave the PWM output is positive and when V_c is smaller than V_r, the output is negative. The inverter's switching frequency f_s establishes by the frequency of triangle waveform V_c. The fundamental frequency component in the inverter output voltage can be controlled by amplitude modulation index; we define the modulation index m_i as follows:

$$m_i = V_c / V_r \quad (1)$$

where V_c and V_r are the peak values of the modulating and carrier waves, respectively. The amplitude modulation index m_i is usually adjusted by varying V_c while keeping V_r fixed. The frequency modulation index is defined by:

$$m_f = f_r / f_1 \quad (2)$$

where, f_1 and f_r are the frequencies of the modulating and carrier waves, respectively. The fundamental component V_{out1} of the output voltage has the property as depicted in equation below in a linear modulation region:

$$V_{out1} = m_i * V_d \; m_i \leq 1.0 \quad (3)$$

in (1) shows that the modulation index and amplitude of the fundamental component of the output voltage varies linearly. The m_i value varied from zero to one; it is defined as the linear control range of sinusoidal carrier PWM. Three level pulse width modulated waveforms can be generated by sine carrier PWM. Sine carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves [6, 12].

The three-level sine-PWM inverter is implementation as a two-level inverter using the same principle. Here sine carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves. The corresponding pulses are generated which are to be supplied to the inverter gate devices. The three reference control signals are phase shift by an angle $2\pi/3$ and $4\pi/3$ with same amplitude. Two carrier waves are in phase each other with dc voltage offset. For three-phase SPWM;

$$V_{peack} = m\frac{v_{dc}}{2} \quad (4)$$

where: V_{peak} is the peak value of the fundamental component of the phase-to-neutral voltage, v_{dc} is the DC link voltage. For three-phase space-vector SVPWM, [13].

$$V_{peack} = m\frac{v_{dc}}{\sqrt{3}} \quad (5)$$

For normal steady-state operation, $0 < m \leq 1$.

3.2. Space vector pulse width modulation

The basic principle of SVPWM depends on synthesizing the vector of reference voltage by time averaging of the two vectors produced by the inverter. The reference voltage vector is the required command voltage which that should be given as required to the application. Space vector PWM technique is based on rotating reference voltage space vector approximation. The rotating reference voltage vector represents the spatial vector sum of the three-phase voltage in the α-β space. The amplitude of the vector and the phase angle of the three-phase can be determined by the instantaneous values of the voltages. If the magnitudes are sinusoidal and balanced, the vector it will rotate rapidly in a fixed angular and have a constant amplitude. When considering the three phase of the inverter, there are 27 switching state. Each of these switching states can be represented as a vector using (6):

$$\vec{V} = V_\alpha + jV_\beta = \frac{2}{3}\left(V_a e^{j0} + V_b e^{\frac{j2\pi}{3}} + V_c e^{\frac{j4\pi}{3}}\right) \quad (6)$$

$$\boldsymbol{\theta = tan^{-1}\left(\frac{V_\alpha}{V_\beta}\right)} \quad (7)$$

where V_a, V_b, V_c are the reference three-phase voltages and V_α and V_β are the components of reference vector in α-β coordinate system. Through the use Clark transformation, the a-b-c three-phase coordinate system is transformed to 2-dimentional α-β frame that is helpful in sector identification by following expression:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (8)$$

The 27 output voltage vectors in the three-level VSI as shown in Figure 2. The space-vector diagram shown in Figure 2 consists of 6 major triangular sectors. Each major section represents π/3 of the fundamental cycle. There are 4 minor triangular sectors within each major sector. Therefore, the total is 24 minor sectors in the plane. The voltage vector is represented by the vertices of these sectors. Based on the amplitude the three-level inverter vectors are divided into large, medium, small, and zero vectors, they are listed as shown in Table 2.

As can be seen in Figure 2, the voltage vectors are located at the various points of the two hexagons interleaved according to their switching. The voltage vectors of group large voltage vectors, with amplitudes of $2V_{dc}/3$ and located at the corners of the outer hexagon. The medium voltage vector is the voltage vector of amplitude $V_{dc}/\sqrt{3}$ and is located at the midpoint of the outer hexagon. Small group voltage vectors with amplitudes of $V_{dc}/3$ and are located at the corners of the inner hexagon. When the rotating voltage vector falls into a certain sector in a three-phase three-level inverter, adjacent voltage vectors are selected to synthesize the desired rotating voltage vector based on the principle of vector synthesis, resulting in PWM waveforms in three-phase. The sector in which Vo* resides can be examined by examining the phase angle and the magnitude of a rotating reference voltage vector V*.

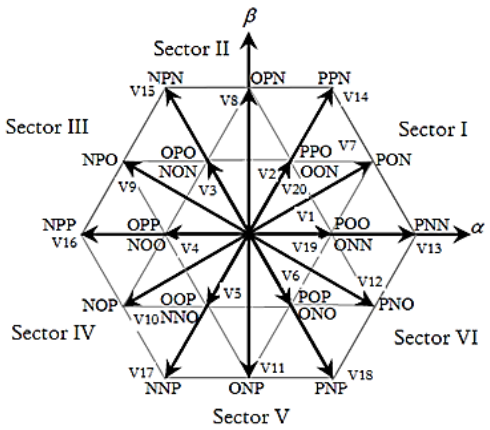


Figure 2. Space voltage vectors in three-level inverter

Table 2. Voltage vectors and switching states

Vector name	vector classification	
Zero vector	[OOO] [PPP] [NNN]	
	P-type	N-type
Small vector	[PPO] [POO]	[ONN] [ONN]
	[OPP] [OPO]	[NOO] [NNO]
	[POP] [OOP]	[ONO] [NON
Medium vector	[NPO] [PON] [OPN]	
	[PNO] [ONP] [NOP]	
Large vector	[PPN] [PNN] [NPN]	
	[PNP] [NNP] [NPP]	

4. THREE-LEVEL INVERTERS SPACE VOLTAGE VECTOR ALGORITHM

As shown in Figure 3, the primary task of SVPWM is to determine, which sector and which of the region, then determine the corresponding output space voltage vectors. The realization of the voltage vector SVPWM is subsumed into the proposed SVPWM technique following steps:

- Transformation of 3-phase to 2-phase.
- Determining the sector containing the tip of the reference vector.
- Determine the region in the corresponding sector.
- Deduction of optimum switching sequence.
- Generation of gating signals to the inverter devices.
- Calculating the duration of switching vectors.

Step 1: Using park's transformation to calculate V_α, V_β, V_{ref} and the angle (θ) (8).

Step 2: After calculating θ, determine the sector according to V_{ref} position of as shown in Table 3

Step 3*:* Determine the region in the corresponding sector. The reference voltage vector can be found in space vector diagram in any region (1-4) of any sector (1-6) as shown in Figure 2.

To estimate the region in sector 1, space vector diagram for m_1 and m_2 is shown in Figure 3, and corresponding switching logic is given in Table 4.

(a) (b)

Figure 3. Space vector diagram for m_1 and m_2 in sector 1

Table 3. Sector calculation based on the location of V_{ref}

Range of α (degree)	$0 \le \theta < 60$	$60 \le \theta < 120$	$120 \le \theta < 180$	$180 \le \theta < 240$	$240 \le \theta < 300$	$300 \le \theta < 360$
Location of V_{ref}	Sector I	Sector II	Sector III	Sector IV	Sector V	Sector VI

$$m_1 = d - c = mcos\theta - \left(\frac{2}{\sqrt{3}} msin\theta\right)\cos\left(\frac{\pi}{3}\right)$$
$$= m\left(cos\theta - \frac{sin\theta}{\sqrt{3}}\right) = m\frac{2}{\sqrt{3}} sin\left(\frac{\pi}{3} - \theta\right) \quad (9)$$

$$m_2 = a = \frac{b}{\sin(\pi/3)} = \frac{2}{\sqrt{3}} msin\theta \quad (10)$$

$$m = \frac{V_{ref}}{2V_{dc}/3} \quad (11)$$

Table 4. Logic used to find the region in which V_{ref} is located

X_1 and X_2	Position of V_{ref}
X_1, X_2 and $(X_1 + X_2) < 0.5$	Region 1
$X_2 > 0.5$	Region 2
$X_1 > 0.5$	Region 3
X_1 and $X_2 < 0.5$ and $(X_1 + X_2) > 0.5$	Region 4

Step 4*: C*alculation of switching time. Determine the switching time of each switch across all the regions.

The SVPWM technique for three-level inverters is called "voltage-time equalization" principle [10]. For example, considering that the reference vector Vref is locating in sector I and in region 2, for this region, the nearest three voltage space vectors are V1, V7 and V2 are shown in Figure 4. Once the nearest three vectors have been identified, by using the volt-second balance method, the on-time calculations of the corresponding vectors can be developed as the following expressions. When the voltage in the second sector is equal to the time synchronization equation; can be written as in (12).

$$v_{ref}T_s = v_1t_a + v_7t_b + v_2t_c \quad (12)$$
$$T_s = t_a + t_b + t_c$$

where T_s is the sampling time, t_a, t_b and t_c are switching on-times for the V_1, V_7 and V_2 vectors respectively.

$$V_1 = \frac{V_{dc}}{3}e^{j0}$$

$$V_2 = \frac{V_{dc}}{3}e^{j\pi/3} = \frac{V_{ref}}{\frac{2}{3}V_{dc}}e^{j\theta}T_s = \frac{1}{2}t_a + \frac{\sqrt{3}}{2}e^{j\frac{\sqrt{3}}{6}}t_b + \frac{1}{2}e^{j\frac{\sqrt{3}}{3}}t_c$$

$$V_7 = \frac{V_{dc}}{\sqrt{3}}e^{j\pi/6}$$

By solving the 3 equations above, the on-time of the concerned vectors can be computed by [14]:

$$t_a = T_s - 2ksin\theta$$

$$t_b = 2ksin(\frac{\pi}{3} + \theta) - T_s$$

$$t_c = T_s - 2ksin\left(\frac{\pi}{3} - \theta\right)$$

$$k = \frac{2}{\sqrt{3}}mT_s$$

where, Ts is the system sampling control cycle, and V_{ref}, θ is the amplitude and angle of the reference voltage vector.

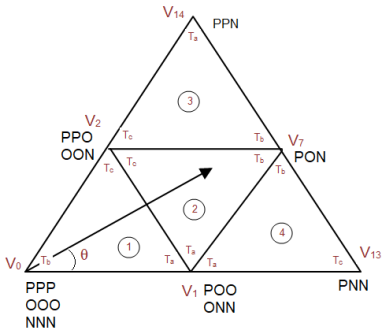


Figure 4. Synthesized reference vector in the first sector

The on-times for other regions in the first sector equilibrium time equations can be computed by using similar procedure as expressed in Table 5. These equations can be made valid for other space vector diagram within the sectors [18].

Table 5. Equations of switching times for sector-1

region	On time		
	t_a	t_b	t_c
1	$2ksin(\frac{\pi}{3} - \theta)$	$T_s - 2ksin(\frac{\pi}{3} + \theta)$	$2ksin\theta$
2	$T_s - 2ksin\theta$	$2ksin\left(\frac{\pi}{3} + \theta\right) - T_s$	$T_s - 2ksin(\frac{\pi}{3} - \theta)$
3	$2ksin\theta - T_s$	$2ksin(\frac{\pi}{3} - \theta)$	$2T_s - 2ksin(\frac{\pi}{3} + \theta)$
4	$2T_s - 2ksin(\frac{\pi}{3} + \theta)$	$2ksin\theta$	$2ksin\left(\frac{\pi}{3} - \theta\right) - T_s$

Step 5*:* Inverter's gating signals generation

The next step in implementation of SVPWM is the selection of the redundant states optimal switching sequence of which is useful in balancing of DC link voltages, fault tolerance and switching

frequency reduction etc. Table 6 shows all possible switching sequence for all sector 1 regions. In the second region of the first sector of the reference vector, the order of switching and phase three-phase spiral of the three-level inverter are shown in Figure 5. After the switching times have elapsed, V_{ref} in which application of voltage space vectors according to sector and region PWM signals should be generated.

Table 6. Possible switching sequence for sector I

Region	Switching sequence
Region 1	PPO-POO-OOO-OON-ONN and symmetry
Region 2	PPO-POO-PON-OON-ONN and symmetry
Region 3	POO-PON-PNN-ONN and symmetry
Region 4	PPO-PPN-PON-OON and symmetry

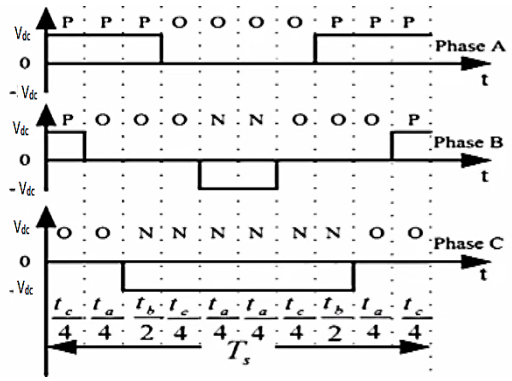


Figure 5. Switching signals for sector-1 second region

5. SIMULATION RESULTS

MATLAB/Simulink software is used to simulate the NPC SVPWM three phase three level inverter scheme shown in Figure 6. In particular, we employed S-functions to enable linear programs to be implemented in Simulink models. In the simulink model, the simulation is performed under the parameters shown in Table 7. Two PWM techniques for controlling the inverter three-phase three-level NPC structure have been simulated in this paper as a comparative study.

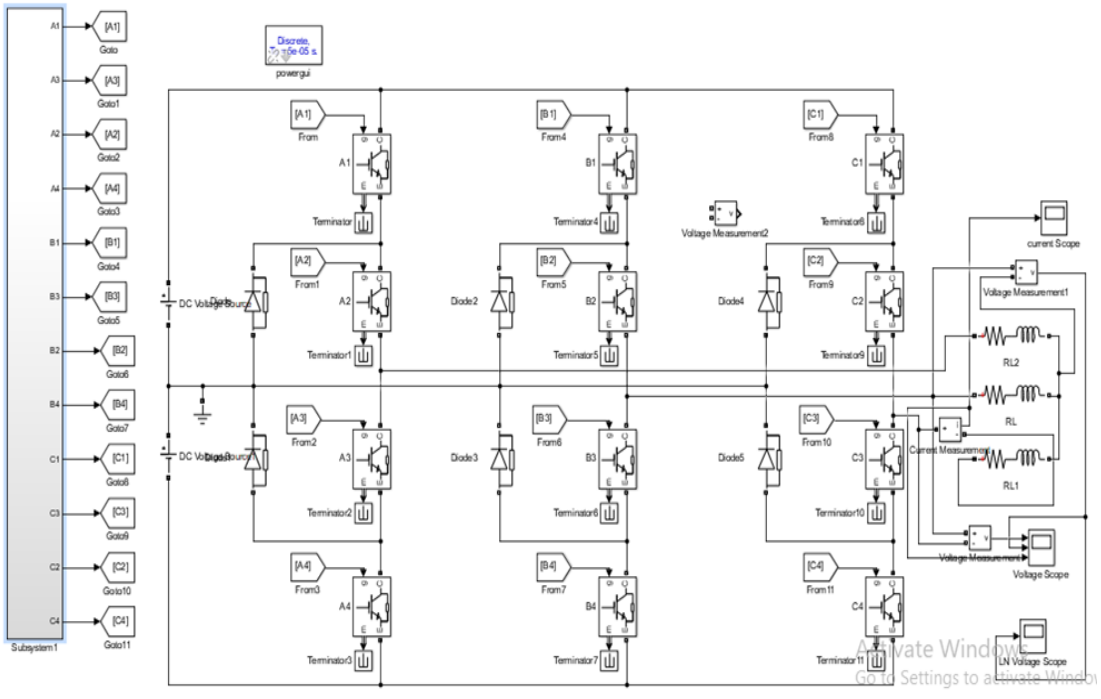


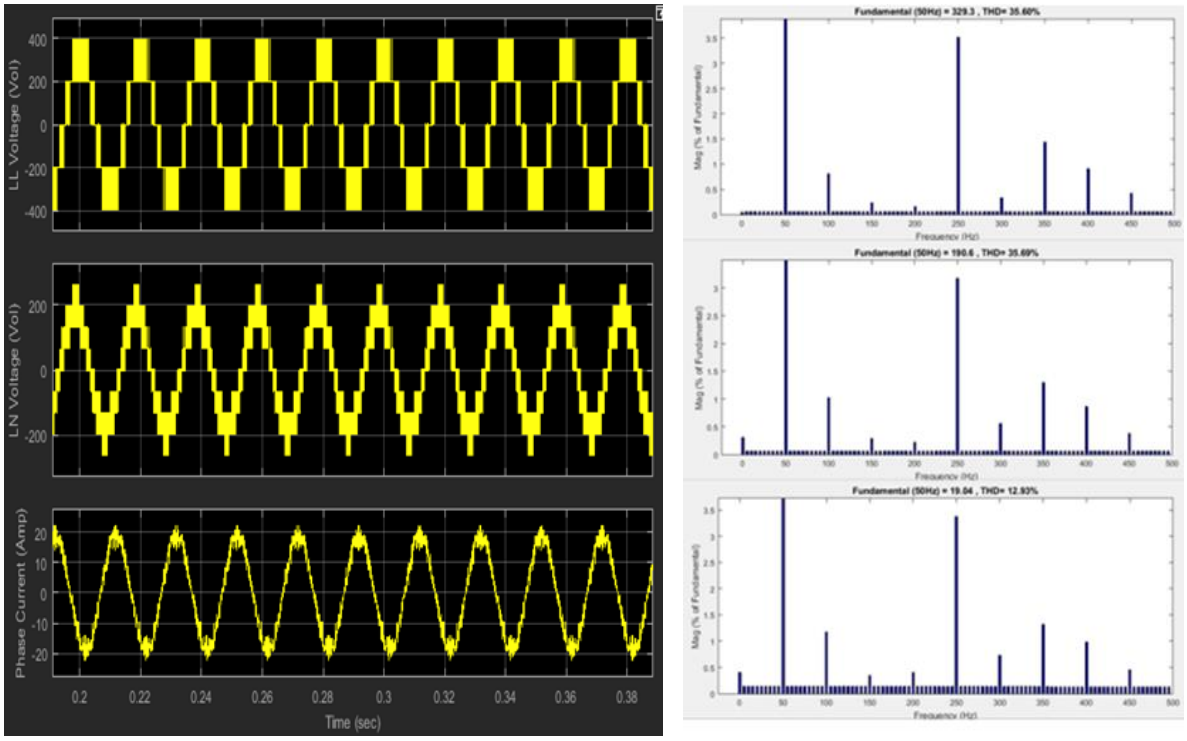
Figure 6. The simulink model of the proposed three-phase three- level diode clamped inverter

Table 7. Three-phase boost inverter parameters (MATLAB/model)

Input DC voltage		400V
AC load per phase	Resistance	10Ω
	Inductance	1 m H
Switching frequency		$5x10^6$ Hz
Carrier Signal Frequency		(2-10)K Hz
Fundamental Frequency		50 Hz

5.1. Simulations results using SPWM technique

From the simulation model in Figure 6, the output voltages and phase current from the proposed inverter are shown in Figure 7. Figure 7 (a) shows the simulated waveforms of the three-phase source voltages inverter output line to line voltage, phase to neutral voltage, and phase current waveforms for RL load. The corresponding harmonic spectrum is shown in Figure 7 (b).



(a) (b)

Figure 7. (a) Output line-to-line voltage, line-neutral voltage and phase current for three phase three level inverter by SPWM algorithm. (b) Line-to-line voltage, line-neutral voltage and phase current FFT

Table 8. %THD output voltages and phase current of Figure 7

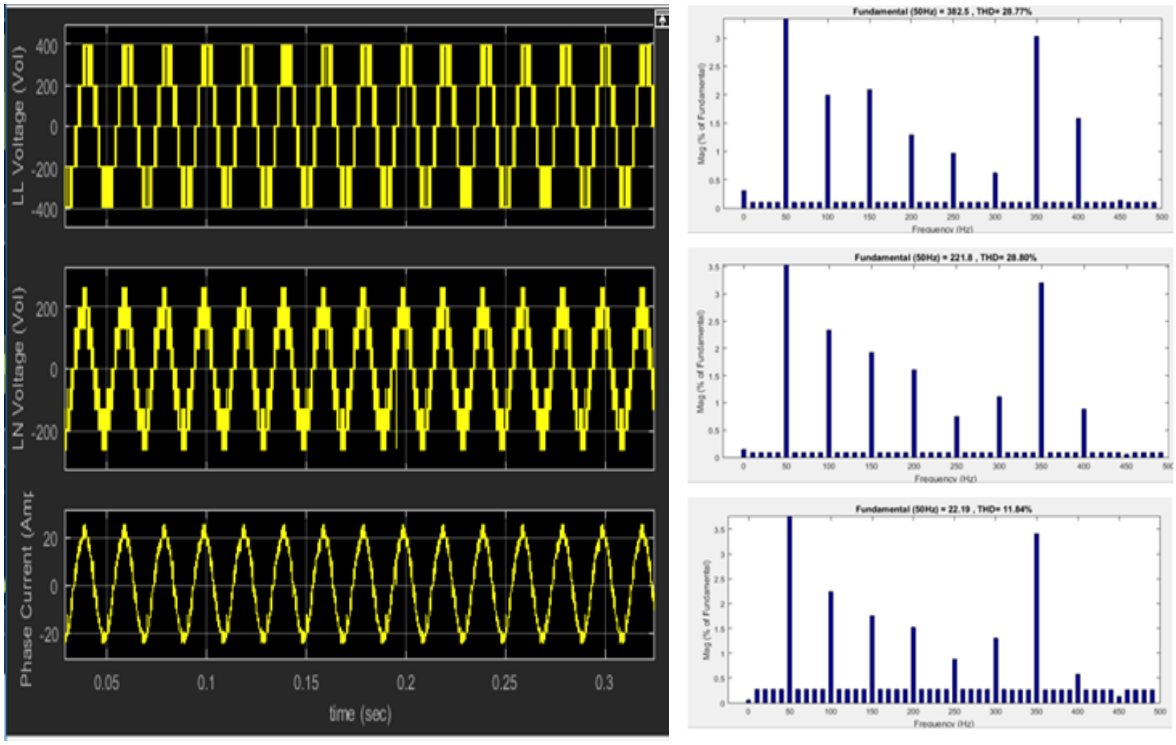
	LL Voltage	NL Voltage	Phase current
Fundamental (50Hz) Value	329.3V	190.6 V	19.4A
THD	35.60%	35.60%	12.93

5.2. Simulations results using SVPWM technique

The SVPWM simulink system model is the same as that of the SPWM system except for the modulating waveform voltages, which are generated by proposed algorithm explained in section 3.2. of the proposed inverter. Figure 8 (a) shows the voltage and current waveforms obtained by controlling the three level SVPWM inverter, the harmonic spectrum of the source current after compensation is shown in Figure 8 (b).

From the simulation result, it can observed that the SPWM technique has total harmonic distortion of line voltage (THD) is 35.60% and the amplitude of the first harmony as 329.3. In addition, the THD of

the phase current is 12.93%, the amplitude of the first harmonic 19.4 A. Where the output line voltage of the inverter switched by SVPWM, the THD is 28.25% and the amplitude of the first harmonic is 567.7 V; the THD of the phase current is 3.66%, and the amplitude of the first harmonic is 178 A.



(a) (b)

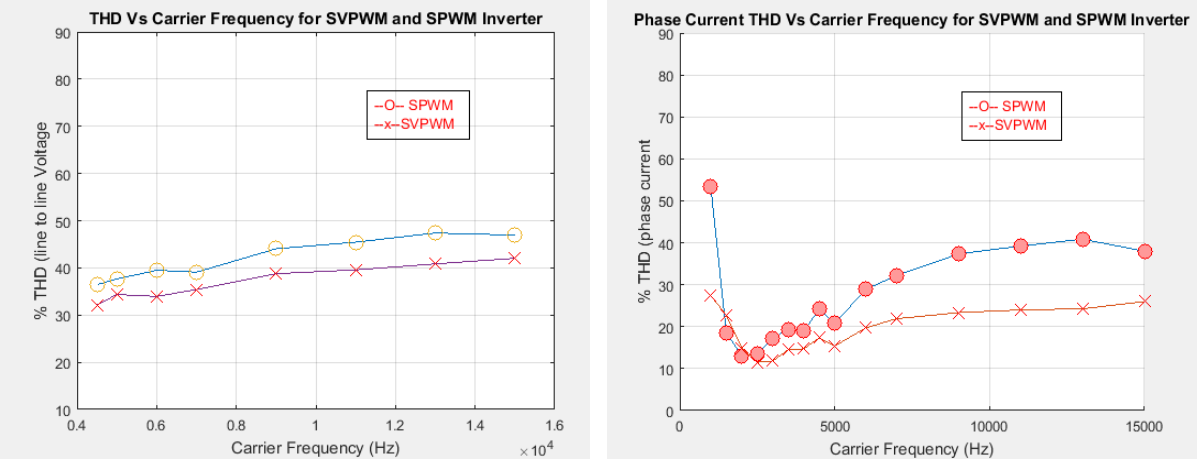
Figure 8. (a) Output line-to-line voltage, line-neutral voltage and phase current for three phase three level inverter by SPWM algorithm. (b) line-to-line voltage, line-neutral voltage and phase current FFT

Table 9. %THD output voltages and phase current of Figure 8

	LL Voltage	NL Voltage	Phase current
Fundamental (50Hz) Value	382.5 V	221.8 V	22.19 A
THD	28.77%	28.80%	11.8

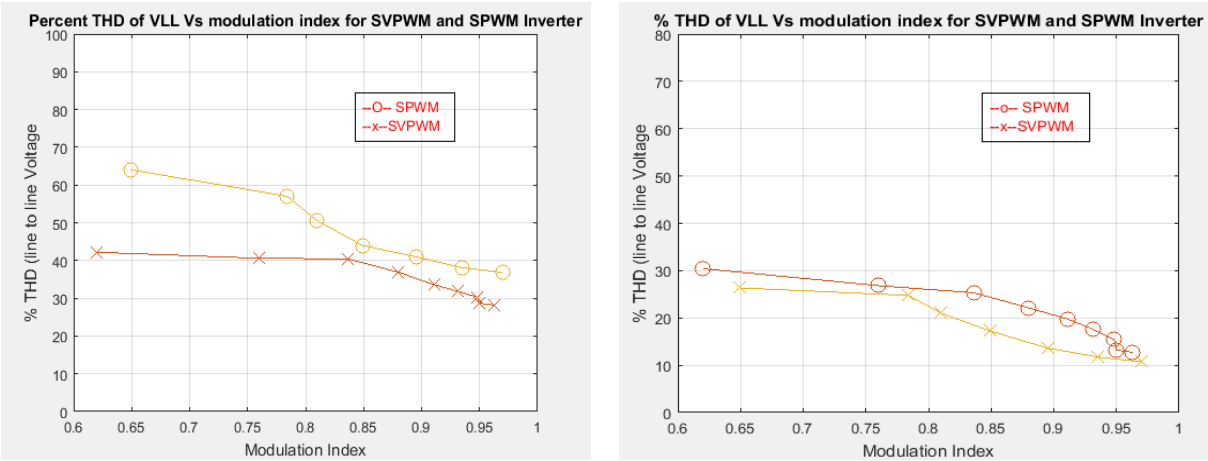
5.3. Comparison of SPWM & SVPWM Inverters

The performance of Space Vector Pulse Width Modulation is compared against Pulse Width Modulation method for three-level inverter. The comparison is done on the basis of simulation results and it is with respect to harmonic content with wide range of carrier frequency and modulation index. The performance of SPWM and SVPWM three-level inverters for simulated results with respect to percentage total harmonic distortion of line to line voltage over a wide range of currier frequency is shown in Figure 9. It is observed the percentage total harmonic distortion of line to line voltage improves for SVPWM inverter as compared to SPWM inverter. The two PWM techniques with three-level inverter are simulated for different modulation indices at a constant switching frequency of 3000Hz. Figure 10 results show the performance curve for modulation index vs Total Harmonic Distortion. According to Figure 10, its note that the increasing of the modulation index for three-level SVPWM can achieve less harmonic distortion compared to SPWM.



(a) (b)

Figure 9. (a) Percent THD of V_{LL} Vs F_{tri} for SVPWM and SPWM inverter,
(b) Percent THD of phase Current Vs F_{tri} for SVPWM and SPWM inverter



(a) (b)

Figure 10. (a) Percent THD of V_{LL} Vs modulation index for SVPWM and SPWM Inverter,
(b) Percent THD of phase Current Vs modulation index for SVPWM and SPWM Inverter

6. CONCLUSION

In this paper, a space vector based SVPWM scheme is compared with sine-triangle SPWM scheme for a NPC three-level inverter. The modeling and simulation of the three phase three level diode-clamped inverter is done using the MATLAB/Simulink program. From the results it is observed that the space vector pulse width modulation technique is better performance than classical conventional method (SPWM). The space vector pulse width modulation technique produces fewer harmonics as compared to the conventional PWM method. The sinusoidal pulse width modulation (SPWM) gives a value of 0.612 *Vdc however the space vector method shows that the maximum output obtained is 0.707 Vdc which is 15% higher than SPWM. The total harmonic distortion (THD) of the output waveform is reduced by 47% than the sinusoidal PWM. From the results it is clear that, SVPWM gave less current ripple, and less THD than the SPWM modulation scheme. Space vector pulse width modulation (SVPWM) technique showed better performance with reduced THD between 0.55 and 0.75 of modulation index.

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