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A 28 GHz 0.18-µm CMOS cascade power amplifier with reverse body bias technique

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Abstract

A 28 GHz power amplifier (PA) using CMOS 0.18 µm Silterra process technology is reported. The cascade configuration has been adopted to obtain high Power Added Efficiency (PAE). To achieve low power consumption, the input stage adopts reverse body bias technique. The simulation results show that the proposed PA consumes 32.03mW and power gain (S_{21}) of 9.51 dB is achieved at 28 GHz. The PA achieves saturated power (P_{sat}) of 11.10 dBm and maximum PAE of 16.55% with output 1-dB compression point (OP_{1dB}) 8.44 dBm. These results demonstrate the proposed power amplifier architecture is suitable for 5G applications.

Keywords*: 5G, CMOS power amplifier, low power consumption, power added efficiency, reverse body bias*

1. Introduction

The race to deploy fifth generation (5G) wireless services by 2020 is ongoing and mm-wave technology will play a key role in meeting mounting demand for broadband data traffic [1]. The mm-wave become next generation carrier source due to exploding data growth in cellular networks and 26-60 GHz bands are of growing interest for potential 5G cellular network [2-4]. The global bandwidth shortage facing wireless carriers has motivated the exploration of the underutilized mm-wave frequency spectrum for future broadband cellular communication networks [5]. However, high efficiency silicon power amplifier (PA) for mm-wave communications is challenging due to ingrained trade-off between break-down and speed in silicon [6]. Power amplifier is one of the important element in Radio Frequency Integrated Circuit (RFIC) design to converts a low power radio frequency signal into a higher power signal in order to make sure that the RF system can deliver high quality, low latency video and multimedia applications for wireless devices [7, 8].

Many researches experience a lot of challenges in implementing mm-wave power amplifiers. First, it is harder to achieve high output power level due to the low supply voltage that accompanies smaller technology nodes. Besides, the technology shrinks causing the gate oxide become thinner and breakdown voltage become lower hence limit to get better output power at receiving end of the system [9, 10]. Second, the power gain output power tradeoff due to transistor sizing that presents itself at mm-wave frequencies poses an upper limit on the maximum transistor size that can be achieved with reasonably high gain and thus on the maximum output power of a single transistor [11]. Moreover, the power gain output power tradeoff due to impedance matching makes it more challenging to achieve high output power levels with reasonable power gain from a single stage amplifier [12, 13].

Research on fifth generation (5G) wireless services by 2020 is in progress, and mm-Wave Ka-Band technology will offer a vital role in meeting high demand for broadband data traffic [14, 15]. Recently, it is reported that Samsung's 5G network also adopts the 28 GHz mm-wave Ka-Band frequency. This is the triggering point for the researcher to research on Ka-Band mm-wave Power Amplifier (PA). These demands have promoted to comprehend a single chip radio transceiver in a low-cost CMOS technology with extra functionality [16]. Since the PA operates at very high frequency, it can have wide bandwidth. However, as the signal

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bandwidth increases, the linearity of the PA is degraded because the asymmetric sideband is generated by the memory effect [6]. Furthermore, the critical part in designing CMOS PA in Ka-Band spectrum is to achieve high gain, low power, input and output matching and power added efficiency over wide band frequency from 26.5-40 GHz.

To date, several excellent CMOS PA's at 20-29 GHz have been reported [11-25]. For example a 22-29 GHz CMOS PA with 2 cascade cascode stage for high power gain in 0.18 µm CMOS process technology is presented [14]. High saturated output power (P_{sat}) of the PA can be enhanced by combining architecture adopted in the output stage. Though P_{sat} of 15.4 dBm is achieved, its PAE of 14.6% and DC power consumption of 163.8 mW are not good enough. In [15], a 22-27 CMOS PA with fully integrated transformer design in 0.18 µm is reported. Though excellent power gain of 14 +/- 2 dB and P_{sat} of 17dBm is achieve, its PAE of 12% is not satisfactory. To demonstrate high PAE and low power consumption can be achieve simultaneously for a 28 GHz CMOS PA, in this work, we report a 28 GHz PA with excellent PAE, P_{sat} and low power consumption using 0.18 µm Siltera process technology. The proposed PA comprises 3 cascade stages with reverse body bias design at input to achieve low dc power consumption and high PAE.

2. Circuit Design

The schematic design of cascade power amplifier is shown in Figure 1. Cascade topology has been chosen to provide sufficient gain. To achieve the desired output power at the power amplifier output, the transistor width of M_1, M_2 and M_3 are optimize to be 48, 50 and 95 µm respectively. The first stage consist of reverse body bias to control the power consumption at first stage (P_{DC1}), to get the high efficiency and low power consumption. The output of the first stage PA is passed to the other stage through an inter-stage matching circuit formed by capacitors C_1 and C_2 which is designed and optimized to achieve maximum PAE and output power. Table 1 shows the component parameters for power amplifier schematic. The design with the three-stage of cascaded amplification is chosen to achieve the required gain. The output stage is designed to provide maximum output power while the first and second stages are designed for maximum gain. Figure 2 show block diagram of cascade system.

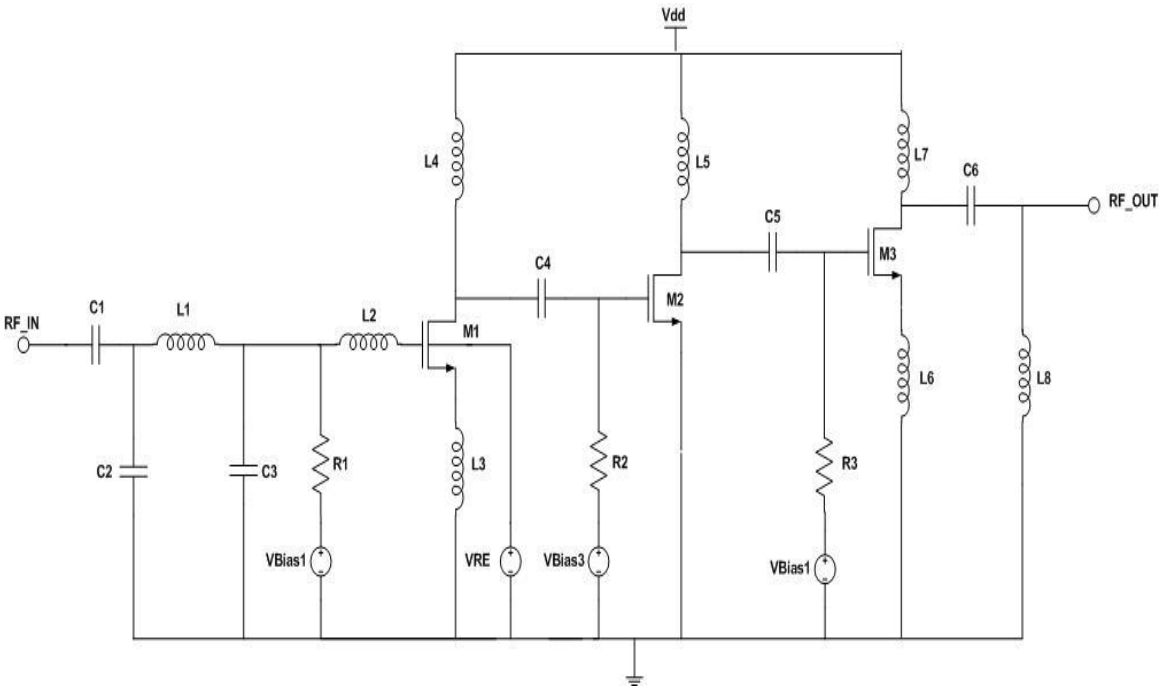


Figure 1. Complete schematic of the proposes three-stage CMOS PA

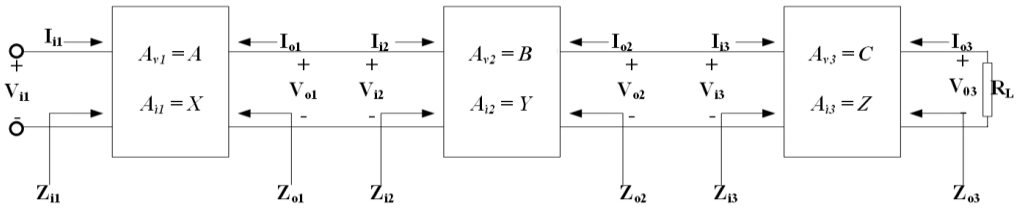


Figure 2. Block diagram of cascade system

Based on Figure 2:

$$\begin{aligned} A_V &= \frac{V_o}{V_i} = \frac{V_{o3}}{V_{i1}} \\ &= \frac{V_{o3}}{V_{o2}} \times \frac{V_{o2}}{V_{o1}} \times \frac{V_{o1}}{V_{i1}} \\ &= \frac{V_{o3}}{V_{i3}} \times \frac{V_{o2}}{V_{i2}} \times \frac{V_{o1}}{V_{i1}} \\ &= A_{v1}A_{v2}A_3 \end{aligned} \quad (1)$$

therefore, if there is n^{th} stage:

$$A_v = \pm A_{v1}A_{v2}A_{v3} \cdots\cdots A_{vn} \quad (2)$$

applying same concept to current gain:

$$A_i = \pm A_{i1}A_{i2}A_{i3} \cdots\cdots A_{in} \quad (3)$$

knowing that, for power:

$$P = IV \quad (4)$$

Hence:

$$A_P = |A_i||A_v| \quad (5)$$

as shown from (5), power gain of the cascade system increases due to current and voltage gain increased by cascading the amplifier stage. Therefore the need for cascading is important to maintain the power gain. The drain current, I_d, in the saturation region, depends on the W/L ratio of transistor, gate bias voltage (V_{gs}) and threshold voltage (V_t):

$$I_d = k'\frac{W}{L}\left[(V_{gs} - V_t)V_{dsat} - \frac{V_{d,sat}^2}{2}\right] \quad (6)$$

where the threshold voltage defines as:

$$V_T = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \quad (7)$$

from (7), the source to bulk voltage (V_{SB}) play an important role to control the V_T. As V_{SB} decreased, V_T will be increased resulting lower I_d. As I_d lower, total power consumption of the device (P_{DC}) will be decreased, eventually it will drive to better efficiency of the circuit as power added efficiency (PAE) is depend on:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{8}$$

noted that for cascade topology as shown in Figure 2, power gain of cascade can be written as:

$$G_1 = \frac{P_1}{P_{in}}, G_2 = \frac{P_{out}}{P_1} \tag{9}$$

from (9), the PAE of the first and second stage can be written as:

$$\eta_1 = \frac{P_1 - P_{in}}{P_{DC1}}, \eta_2 = \frac{P_{out} - P_{in}}{P_{DC2}} \tag{10}$$

hence;

$$\begin{aligned} \eta_{total} &= \frac{P_{out} - P_{in}}{P_{DC1} + P_{DC2}} \\ &= \frac{(P_{out} - P_1) + (P_1 - P_{in})}{P_{DC1} + P_{DC2}} \\ &= \frac{1}{P_{DC1} + P_{DC2}}\left[(P_{out} - P_1) + (P_1 - P_{in})\right] \end{aligned} \tag{11}$$

substituting (9) and (10) in (11) will lead to:

$$\eta_{total} = \frac{\eta_2}{\left[\frac{P_{DC1}}{P_{DC2}} + 1\right]}\left[1 + \left(\frac{G_1 - 1}{G_1}\right)\left(\frac{1}{G_2 - 1}\right)\right] \tag{12}$$

notice that, from (12) if the P_{DC1} is minimum and G_2 is high, the efficiency of the PA will increased. Therefore, to reduce the P_{DC1}, reverse bias technique at the input stage is applied while G_2 is set to be high by cascading the circuit.

Table 1. Component parameters for Power Amplifier schematic

Component	Parameter	Component	Parameter
V_{dd}	1.9 V	C_5	159.24 fF
V_{bias1}, V_{bias3}	800 mV	L_1	478.98 pH
V_{bias2}	864 mV	L_2	181.34 pH
V_{RE}	-510 mV	L_3	211.58 pH
M_1	0.18 µm ×48 µm	L_4	195.16 pH
M_2	0.18 µm ×50 µm	L_5	238.64 pH
M_3	0.18 µm ×95 µm	L_6	195.16 pH
C_1, C_2	53.29 fF	L_7	208.93 pH
C_3	130 fF	L_8	705.34 pH
C_4	207.06 fF	R_1 , R_2 , R_3	2.15 kΩ

3. Simulation Result and Discussion

S-parameter simulation results are shown in Figure 3. The power amplifier provides a simulated peak S_{21} of 9.51 dB at 26 GHz. The S_{21} 3-dB bandwidth is 10 GHz centered around 26.75 GHz. As the input is matched to 50 Ω impedance, it provide a peak simulated S_{11} of -15 dB at 27 GHz. The S_{11} 10-dB bandwidth is 3.48 GHz ranging from 25.52 GHz to 29 GHz.

As the output is matched to 50 Ω impedance, it provides peak simulated S_{22} of -21.31 dB at 27.6 GHz. The S_{22} 10-dB bandwidth is 12.43 GHz ranging from 25.41 GHz to 37.84 GHz. Power simulation results are shown in Figure 4 and 5. The power amplifier delivers a 1 dB compression and saturated output powers of +8.44 dBm and +11.10 dBm respectively as shown in Figure 4. The power gain obtained for the designed PA is 8.07dB and the peak simulated power added efficiency is 16.55% as shown in Figure 5. The amplifier consumes 32.03 mW from 1.9 V power supply.

Simulation results of the proposed PA, with and without reverse bias voltage at 28 GHz for PAE and DC power consumption is shown in Figure 6 (a) and (b). It is clearly notice that the performance of the PA with reverse bias voltage shows significant improvements in term of PAE and total power consumtion. The performance comparison between the proposed PA with and without reverse bias are summarize in Table 2.

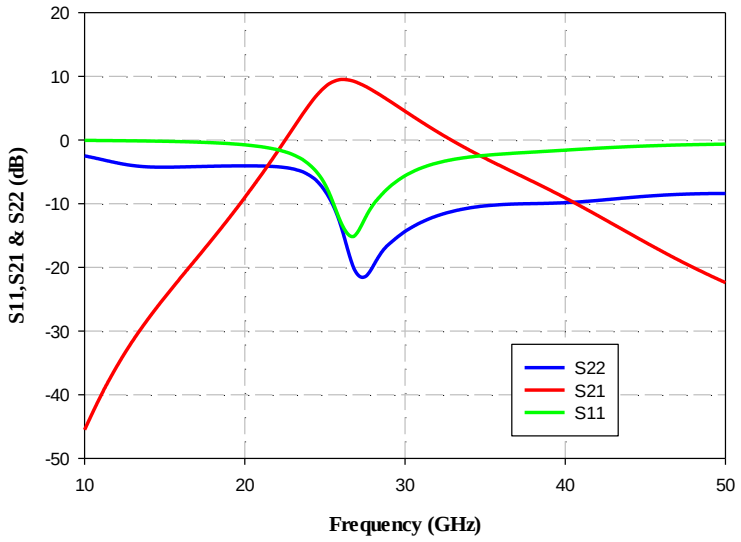


Figure 3. SimulatedS_{21}, S_{11} and S_{22} versus frequency at 28 GHz

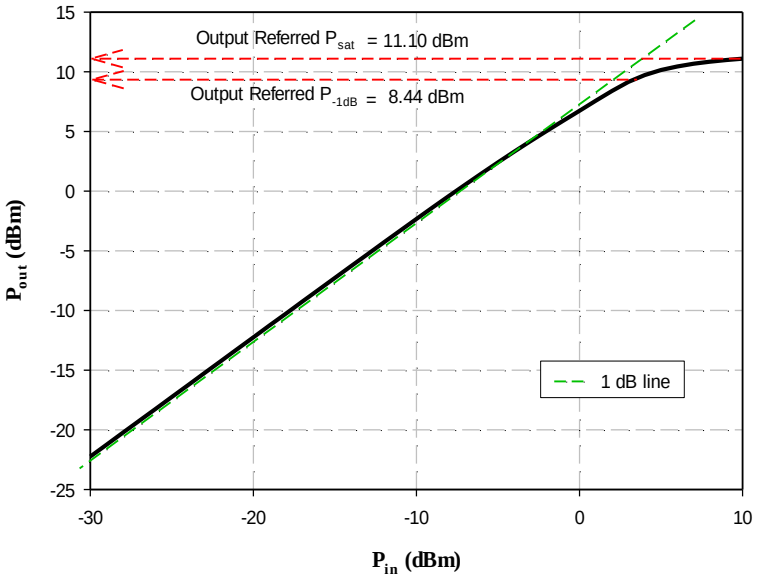


Figure 4. Simulated P_{1dB} of the PA at 28 GHz

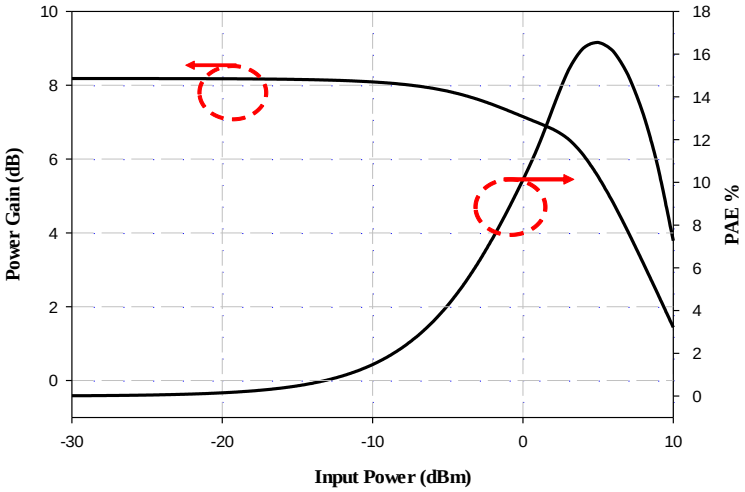
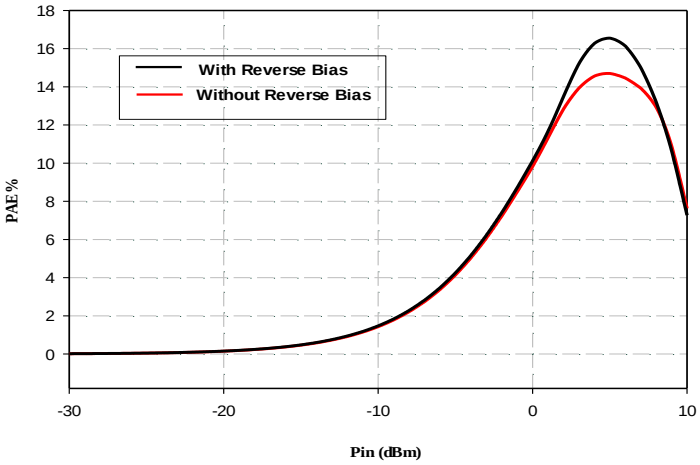
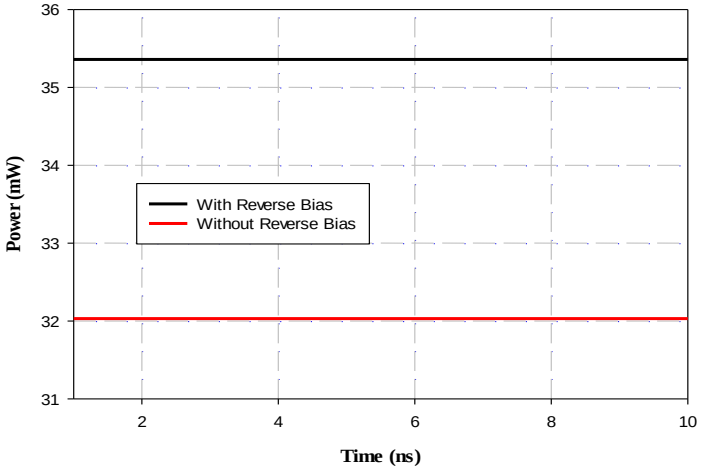


Figure 5. Simulated power gain & PAE of the PA at 28 GHz



(a)



(b)

Figure 6. Performance comparison between (a) PAE and (b) DC power, with and without reverse bias condition

Table 2. Summary of the Proposed PA's Performance at 28 GHz with and without Reverse Bias

Variable	With Reverse Bias	Without Reverse Bias
Output P_1dB	8.44 dBm	8.72 dBm
Output P_{sat}	11.10 dBm	11.17 dBm
Power Gain	8.07 dB	8.32 dB
Maximum PAE	16.55 %	14.68%
Peak S_{21}	9.51 dB	9.30 dB
Peak S_{11}	-15 dB	-15 dB
Peak S_{22}	-21.31 dB	-20 dB
DC power consumption	32.03 mW	35.36 mW

4. Conclusion

This work addresses the requirements, and challenge of realizing an efficient mm-Wave PA in standard CMOS technology for 5G application. A 3 stage cascade with reverse bias topology at 28 GHz CMOS PA is presented. The amplifier is implemented in a standard CMOS 0.18 µm process. The proposed topology employed cascade structure to obtain high PAE with reverse body bias at input stage to achieve low power consumption. The simulation results show that the proposed PA is able to deliver 11.10 dBm of output power to a 50 Ω load with PAE of 16.55% at power consumption of 32.03 mW using a 1.9 V voltage.The proposed PA can be used for future 5G communications.

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