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Buck converter controlled with ZAD and FPIC for DC-DC signal regulation

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ABSTRACT

This paper presents the performance of a fixed-point induction control (FPIC) technique working in conjunction with the non-linear control technique called zero average dynamics (ZAD) to control chaos in a buck converter. The control technique consists of a sliding surface in which the error tends to zero at each sampling period. A switch is controlled by using centered pulse width modulation (CPWM) control signal. The converter controlled with ZAD-FPIC has been simulated in Matlab and implemented using rapid control prototyping (RCP) in a DSP to make comparisons between simulation and experimental tests. To perform this comparison, some variations in the control parameter and the voltage reference are made in order to evaluate the performance of the system. Results are obtained with errors lower than 1 % which demonstrates the good performance of the control techniques.

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1. INTRODUCTION

The variable structure systems switched via centered pulse width modulation (CPWM) present a great number of dynamic behaviors when the control parameters are changed. Some studies of the DC-DC buck converter [1, 2] are obtained with analytical [3, 4] numerical [5] and experimental results [6, 7] all that for certain values of the parameters where instability, strange phenomena, chaos [8] period bands, and subharmonics are presented. Besides, one-period orbits and above were studied in [9], by using numerical simulation algorithms. Due to the discontinuous actions of the controller in conjunction with the global system, "chattering" appears increasing ripple and distortion at the output [10]. With the aim of reducing these problems and obtaining regulated signals at the output, the ZAD control technique (zero average dynamics) was proposed [5, 11-13] whereby using a sliding surface that is forced to have a zero average in each iteration. Herein, it considers the reference signal, the real value at the output, and its derivatives to calculate the duty cycle. This technique combines advantages such as fixed switching frequency, robustness, and low error.

The controller with ZAD technique has shown good performance in numerical results as in [14-16] and in experimental results as in [13, 15, 17-21]. However, most of the implementations contemplate

a centered pulse width modulator (CPWM), mainly due to technical reasons related to current and voltage measurement in areas where they are not so affected by switching transient problems. In studies carried out in [16], where the converter is controlled by the ZAD technique, a new control technique called FPIC (control by induction to the fixed point) is proposed [22-24], which is useful for controlling unstable and/or chaotic systems. In the present work, it is proposed to control the converter studied extensively by [10, 13-15, 25] which will be controlled at the same time by the ZAD and FPIC techniques in order of regulate DC signals at the output with low steady state error.

2. MODEL FOR CPWM WITH ZAD AND FPIC

This section shows the ZAD and FPIC control algorithms with CPWM for an autonomous non-linear SISO system defined by (1), where $x \in R^n$ with f and g vector fields defined ON R^n. Figure 1 shows the electric circuit that corresponds to the power converter, which considers an inductor L, an internal resistance of the inductor r_L , a capacitor C, and a resistance R. With the above equations a non-linear model is obtained in system state variables as shown in (4). The state variables are the voltage in the capacitor (υ_c) and the current in the inductance (i_L). The control variable (u) takes discrete values $+1$ and -1. This system can be represented as $\dot{x} = Ax + Bu$. As the control signal u takes values $+1$ or -1 shown in Figure 2, two different topologies are presented in each sampling period. This system will be controlled by a CPWM in which the system can be modeled as presented in (5).

$$\dot{x} = f(x) + g(x) \cdot u \tag{1}$$

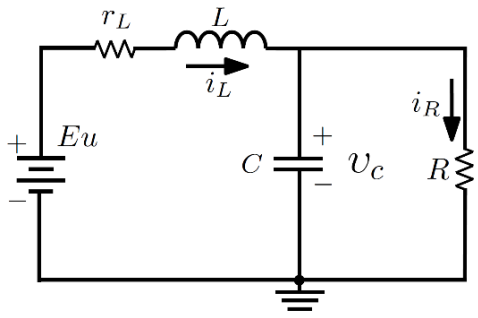


Figure 1. Electric circuit considered in the study

By considering the circuit presented in Figure 1, (2) and (3) are obtained as follows:

$$i_L = C\frac{d\upsilon_c}{dt} + \frac{\upsilon_c}{R} \tag{2}$$

$$Eu = L\frac{di_L}{dt} + \upsilon_c + r_L i_L \tag{3}$$

$$\begin{bmatrix}\dot{\upsilon}_c \\ i_L\end{bmatrix} = \begin{bmatrix}-\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & -\frac{r_L}{L}\end{bmatrix}\begin{bmatrix}\upsilon_c \\ i_L\end{bmatrix} + \begin{bmatrix}0 \\ \frac{E}{L}\end{bmatrix}u \tag{4}$$

$$\dot{x} = \begin{cases} Ax + B, & with\ u = +1, \quad 0 < t < \frac{d}{2} \\ Ax - B, & with\ u = -1, \quad \frac{d}{2} < t < T - \frac{d}{2} \\ Ax + B, & with\ u = +1, \quad T - \frac{d}{2} < t < T \end{cases} \tag{5}$$

Biel, Fossas and Griño [13], proposed the ZAD control technique, which guarantees robustness, fixed switching frequency, and low error. The average function s(x) expressed in (6), called sliding surface,

requires zero at each switching period and that the output voltage (υ_c) follows the reference (υ_{ref}). Numerical results for CPWM, presented in [14, 17, 15], and also experimental results presented in [19-21], have demonstrated the good operation of this technique. In (6), υ_c is the real voltage measured in the load or in the capacitor, υ_{ref} is the reference voltage given by the user, and K_s is the time constant associated to the first order dynamic in the sliding surface. Now, the solution for the non homogeneous case of the state space system defined in (7) is presented in (8). Then the system is solved for the three sections shown in Figure 3; where the control signal u is observed for a single period (T).

$$s(x) = \left(\upsilon_c - \upsilon_{ref}\right) + K_s\left(\dot{\upsilon}_c - \dot{\upsilon}_{ref}\right) \tag{6}$$

$$\dot{x} = Ax + Bu \tag{7}$$

$$x(t) = e^{At}x(0) + \int_0^t e^{A(t-\tau)}Bu(\tau)d\tau \tag{8}$$

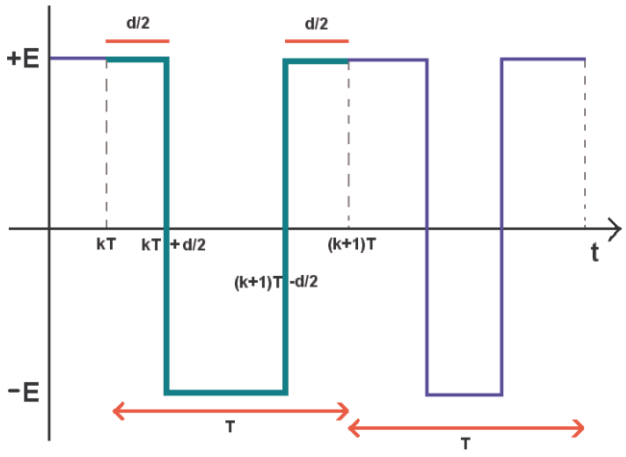


Figure 2. Control signal u obtained with the centered pulse width modulator (CPWM)

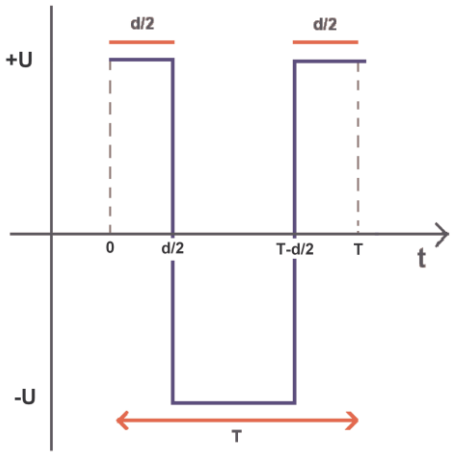


Figure 3. Three control signal conditions per period (T)

For the first interval, $Ax + B$, with $u = +1$, $0 < t < \frac{d}{2}$, the solution in function of time is represented in (9):

$$x(t)_{(u=+1)} = e^{At}x(0) - A^{-1}[I - e^{At}]B \tag{9}$$

next, the initial value $(x(d/2))$ is calculated with (10) and that will be the intial condition for the second interval.

$$x(d/2) = e^{A(d/2)}x(0) - A^{-1}[I - e^{A(d/2)}]B \tag{10}$$

Now, for the second interval, $Ax - B$, with $u = -1$, and $\frac{d}{2} < t < T - \frac{d}{2}$; a new solution in time is obtained as expressed in (11):

$$x(t)_{(u=-1)} = e^{At}x(0) - A^{-1}[I - e^{At}]B \tag{11}$$

and the initial condition for the third interval is defined as expressed in (12):

$$x(T - d/2) = e^{A(T-d)}x(d/2) + A^{-1}[I - e^{A(T-d)}]B \tag{12}$$

finally, for the last interval, $Ax + B$, with $u = +1$, $T - \frac{d}{2} < t < T$, the time solution is defined as in (13):

$$x(t) = e^{At}x(T - d/2) - A^{-1}[\mathrm{I} - e^{At}]B \quad (13)$$

solution for $\mathrm{t} = \mathrm{T}$ is equal to the expressed in (14):

$$x(T) = e^{A(d/2)}x(T - d/2) - A^{-1}[\mathrm{I} - e^{A(d/2)}]B \quad (14)$$

Substituting (10) and (12) in (14), a general solution is obtained as shown in (15):

$$x(T) = e^{A\mathrm{T}}x(0) + \left[-2e^{A(\mathrm{T}-\mathrm{d}/2)} + 2e^{A(d/2)} + e^{AT} - \mathrm{I}\right]\mathrm{A}^{-1}B \quad (15)$$

A discrete time solution, which are multiples for the values of T, is obtained with (16):

$$x((k+1)T) = e^{AT}x(kT) + [-2e^{A(T-d/2)} + 2e^{A(d/2)} + e^{AT} - I]A^{-1}B \quad (16)$$

2.1. ZAD and FPIC control

To control the converter in real time, it is necessary to calculate the duty cycle (d), to determine the time of the switching period (T). This time is related to the intervals that the switch will be ON (d) and OFF ($\mathrm{T} - \mathrm{d}$). Thus, the equation that defines the duty cycle (d) to be applied at each iteration according to the ZAD and FPIC techniques is given by (17). By using x_1, x_2, the parameters of the filter LC, the parameter K_s, the reference signal, and the source voltage (E); the expressions s(x(kT)), $\dot{s}_+$(x(kT)), $\dot{s}_-$(x(kT)), and dss are calculated as shown in (18-22).

$$d(kT) = \frac{d\_zad(kT) + N * dss}{N+1} \quad (17)$$

$$d\_zad(kT) = \frac{2s(x(kT)) + T\dot{s}_-(x(kT))}{\dot{s}_-(x(kT)) - \dot{s}_+(x(kT))} \quad (18)$$

$$dss = \frac{T\left[x_{1ref}(hm - ap) + \dot{x}_{1ref}(a+p) - \ddot{x}_{1ref} - h\frac{E}{L}\right]}{-2h\frac{E}{L}} \quad (19)$$

where:

$$s(x(kT) = (1 + aK_s)x_1(kT) + K_s h x_2(kT) - x_{1ref} - K_s\dot{x}_{1ref} \quad (20)$$

$$\dot{s}_+\big(x(kT)\big) = (a + a^2K_s + hK_sm)x_1(kT) + (h + ahK_s + hK_sp)x_2(kT) + hK_s\frac{E}{L} - \dot{x}_{1ref-K_s\ddot{x}_{1ref}} \quad (21)$$

$$\dot{s}_-(x(kT)) = (a + a^2K_s + hK_sm)x_1(kT) + (h + ahK_s + hK_sp)x_2(kT) - hK_s\frac{E}{L} - \dot{x}_{1ref} - K_s\ddot{x}_{1ref} \quad (22)$$

3. SOFTWARE

The implementation of ZAD and FPIC techniques in order to control the converter requires to configure the algorithm in a platform that provides good characteristics in terms of handling the signals with precision. The plataform has high sampling speed and is computationally effective, thus allowing the control to be executed in real time. Therefore, for the implementation of these control techniques, the DS1104 DSPACE board is used. This device is programmed in Simulink-Matlab platform and there is a visualization interface that can be programmed depending on the need, this platform is called ControlDesk. Below in Figure 4, it is shown one by one the stages carried out in simulink to configure the complete control system.

3.1. Analogue signal sampling (υ_c, i_L, iR and E)

For the implementation of the ZAD and FPIC control techniques, it is necessary to know some values of constant parameters such as: L, C, rL, Fs, Fc, K_s and N. In addition, some system variables must be known in real time such as: capacitor voltage (υ_c), supply voltage (E), inductor current (i_L), and the load (R), which is linear and can be estimated using the Ohm's law, so it is necessary to measure the load current (i_R).

The DS1104MUX_ADC block shown in Figure 5 is used to carry out this first stage. This block has internal access to 4 multiplexed channels (ADCH1, ADCH2, ADCH3, and ADCH4) for data sampling and each one has 16-bit resolution. In this case, channel ADCH1 is used for sampling (υ_c), channel ADCH2 for the current in the inductor (i_L), channel ADCH3 for current in the load (iR) and channel ADCH4 for the source voltage (E). Figure 5 shows amplifications of 10 times the signal for the four inputs (gain1, gain2, gain3, and gain 3) because the block makes an internal division by 10. Then, in order to have the signals with their real values, it is necessary to multiply by the gains av, ai, aR and aE; and the final signals are sensed.

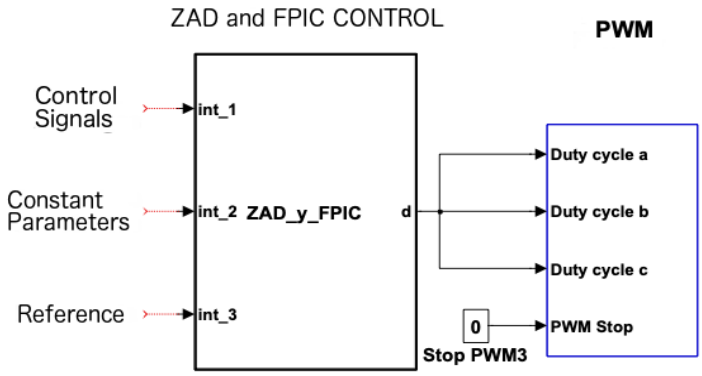


Figure 4. General outline of the control system with ZAD and FPIC

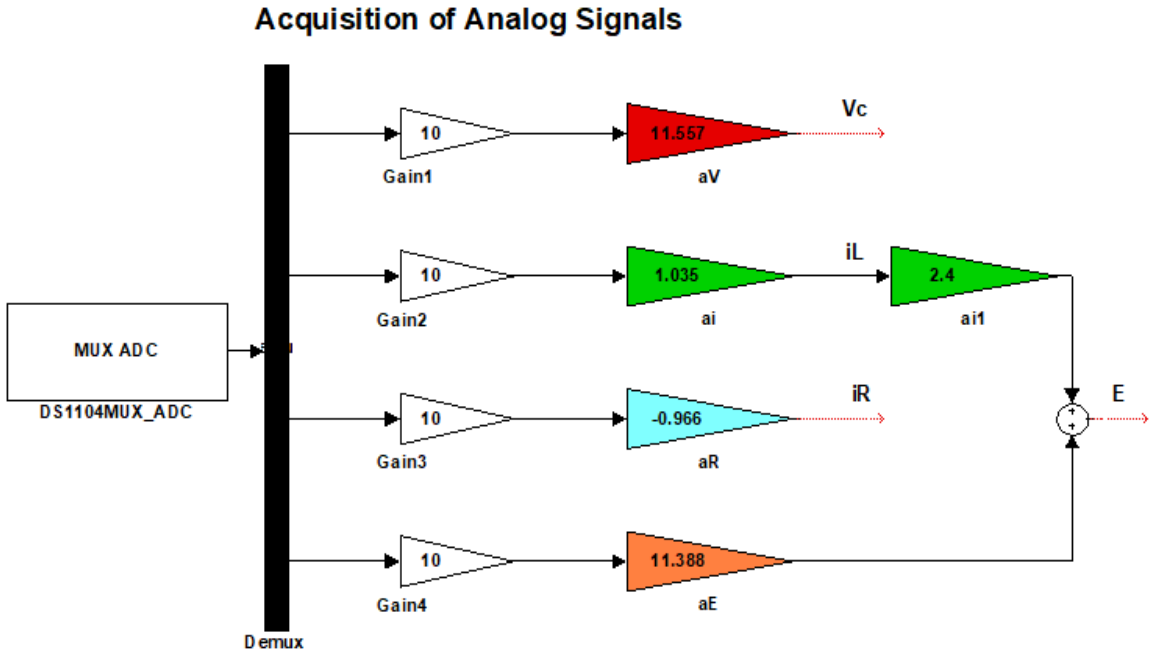


Figure 5. Acquisition of signals at the DSP input

3.2. Reference signal generation

To execute the control techniques, it is necessary to have the reference signal, because the controller needs to have the reference that the user wants at the output. Figure 6 shows the block programmed in simulink that introduces the reference signal and the calculation of its first and second derivative. The block is compiled into the DSP and by using the ControlDesk software [26] the reference signal, amplitude, and frequency values can be changed manually.

3.3. ZAD and FPIC control

These two techniques were implemented using an embedded function block. The control block is shown in Figure 7, in which the values of constant parameters and those acquired from the real system are entered. Thus, the duty cycle is calculated in this block by implementing the (17-20).

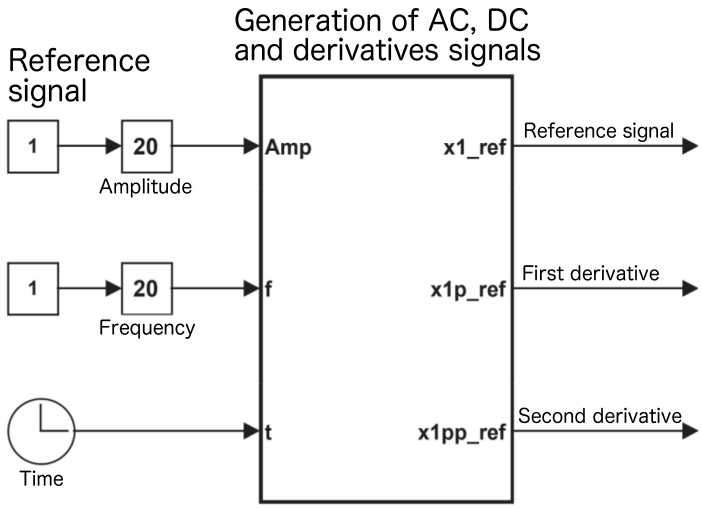


Figure 6. Reference signals

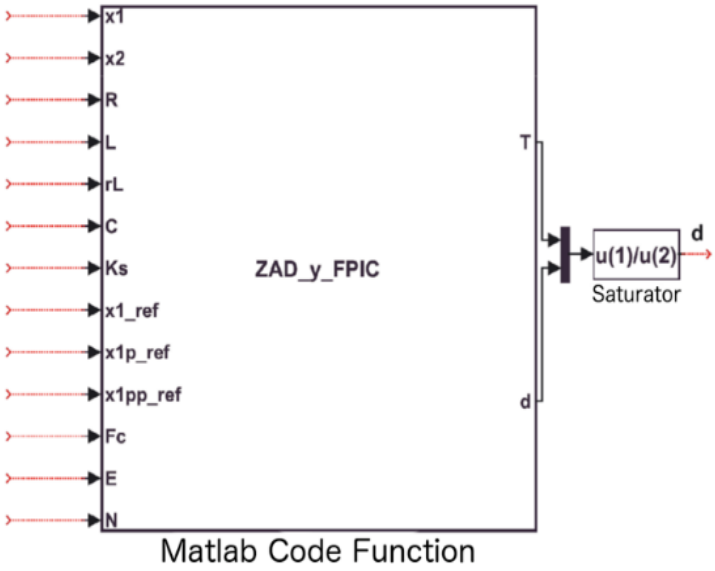


Figure 7. Execution blocks for controllers (ZAD and FPIC)

4. RESULTS AND ANALYSIS

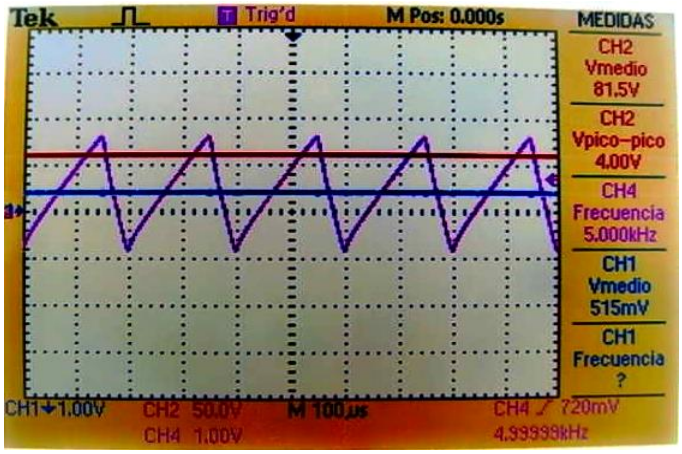
The results presented below are taken from an experimental prototype consisting of a single-phase inverter as described above, powered by a dual source BK PRECISION 1761 configured to provide ±30 Volts. The parameters of the converter and the controllers are shown in Table 1. In case of regulation, it is very important that the value of the capacitor used in the filter be large for smaller ripple. Therefore, in DC-DC signal regulation the value of $C = 229$ µF was used. The performance of the ZAD and FPIC control techniques applied to the drive when sensing the supply voltage (±E) is shown below. The control parameter with ZAD for this case is $K_s = 2$). Figure 8 (a) shows the experimental behavior when the signal has a positive value in the reference voltage ($\upsilon_{ref} = 80$ Volts DC). This Figure shows the current in the inductor (i_L) (purple), which has triangular behavior and similar switching frequency to the CPWM signal.

Additionally, this Figure shows the current in the load, which is proportional to the voltage in the capacitor and without ripple. Figure 8 (b) shows the experimental behavior when the signal has a negative value in the reference voltage ($\upsilon_{ref} = -80$ Volts DC). This Figure shows that the current in the inductor and the current in the load are negative.

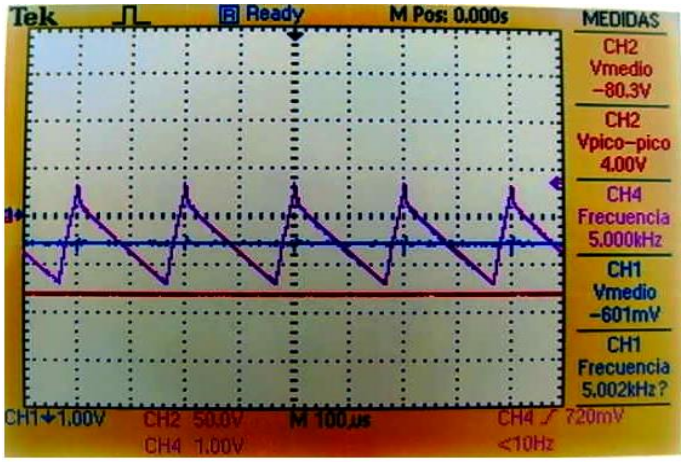
Figure 9 shows four signals measured with the Tektronix TDS2014 oscilloscope. The first signal (CH1) correspond to the current in the load with a value approximately 130 mA, because the load impedance is 151.3Ω. The second signal (CH2) presents the supply voltages with + E and – E values; this channel has a gain of 50 V/div. In channel CH3, the oscilloscope shows the output voltage at the load, regulated to 20 V; note that this channel has a gain of 5V/div. Finally, channel CH4 the current in the inductance is measured; this channel has a gain of 500 mV/div. Figure 10 shows the behavior of the converter when the reference of 20 Volts is given by the user when parameter $K_s = 2$. These signals were obtained by using the acquisition interface designed with the DS1104 board. This zone corresponds to the stable state where the drive regulates with low voltage errors of approximately ±0.5 % and the duty cycle fluctuates between 0.82 and 0.85.

Table 1. Parameters of the converter and controllers

Parameter and Description	Valor
R = Load resistance	151.3 Ω
C= Capacitance	229 µf
L = Inductance	3,945 mH
r_L= Internal resistance	4 Ω
E = Input voltage	±30 V (Dual Source)
Fc= Switching frequency	5 kHz
Fs= Sample rate	25 kHz
N = Control parameter with FPIC	1



(a)



(b)

Figure 8. Voltage measured in the load obtained for the experimental results: (a) with a positive value in the reference voltage ($\upsilon_{ref} = 80$ V), and (b) with a negative value in the reference voltage ($\upsilon_{ref} = -80$ V)

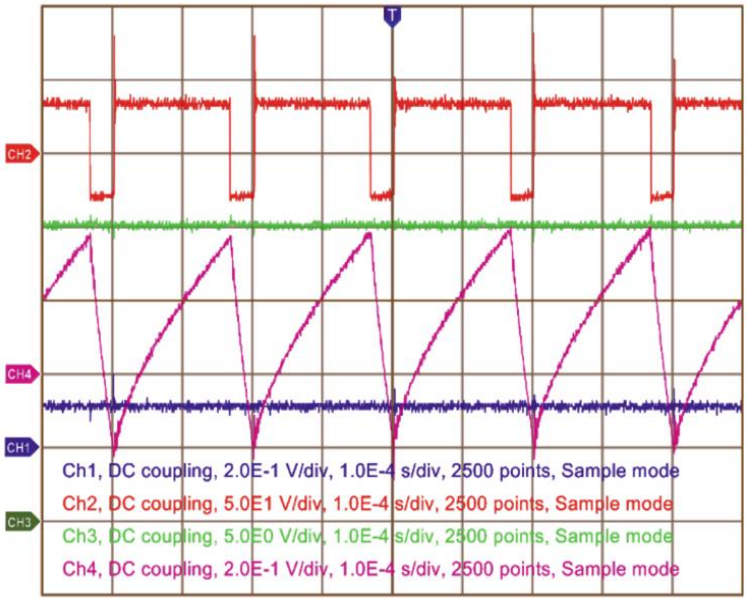


Figure 9. Outputs at the oscilloscope

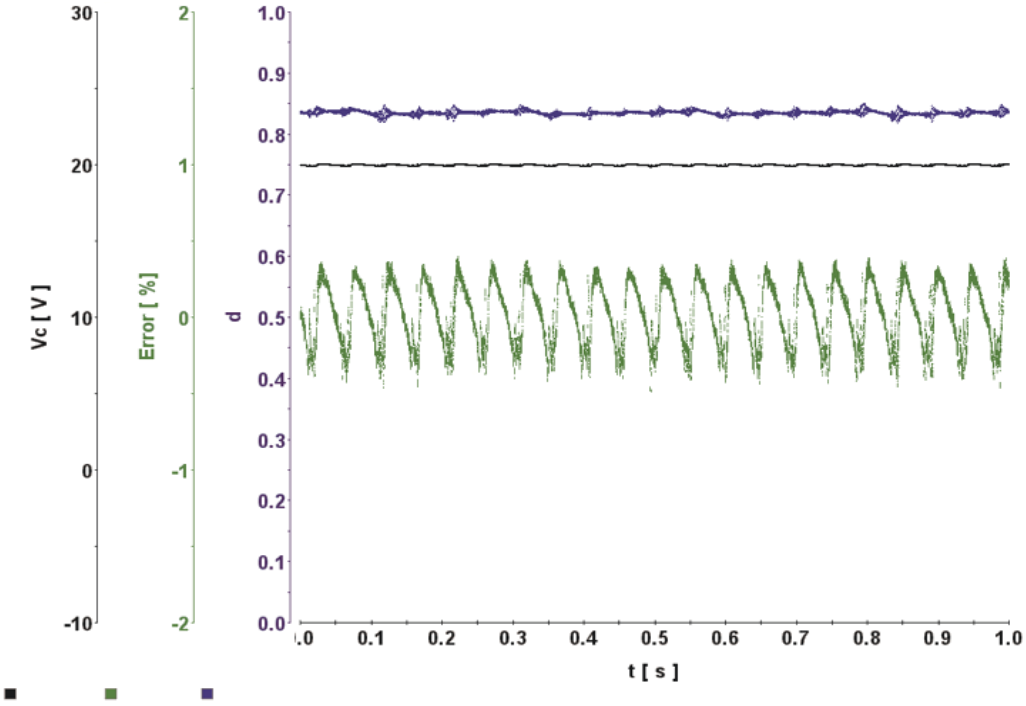
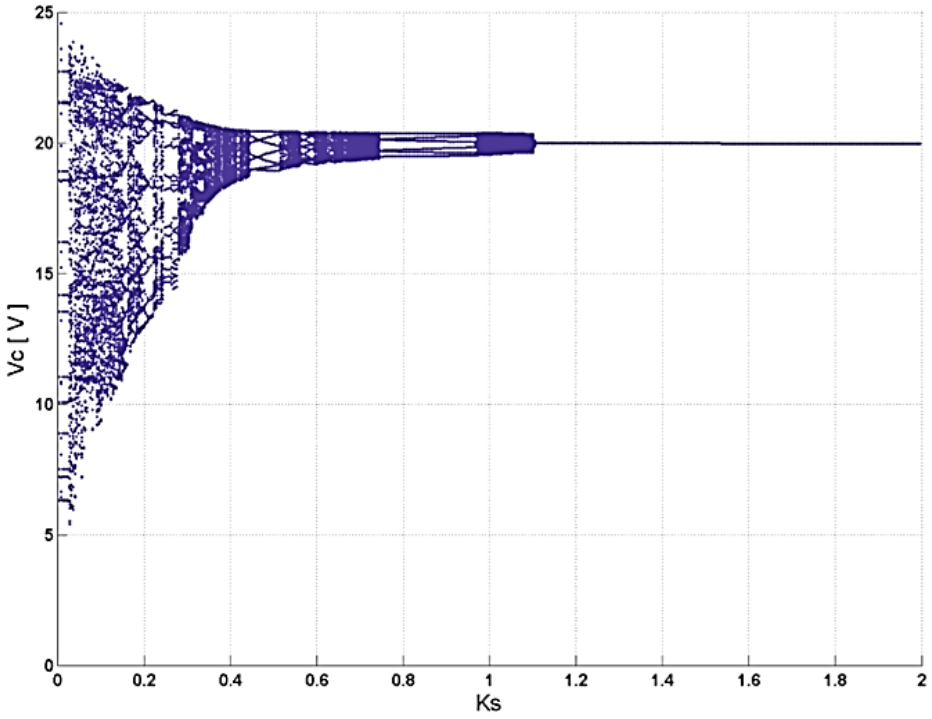


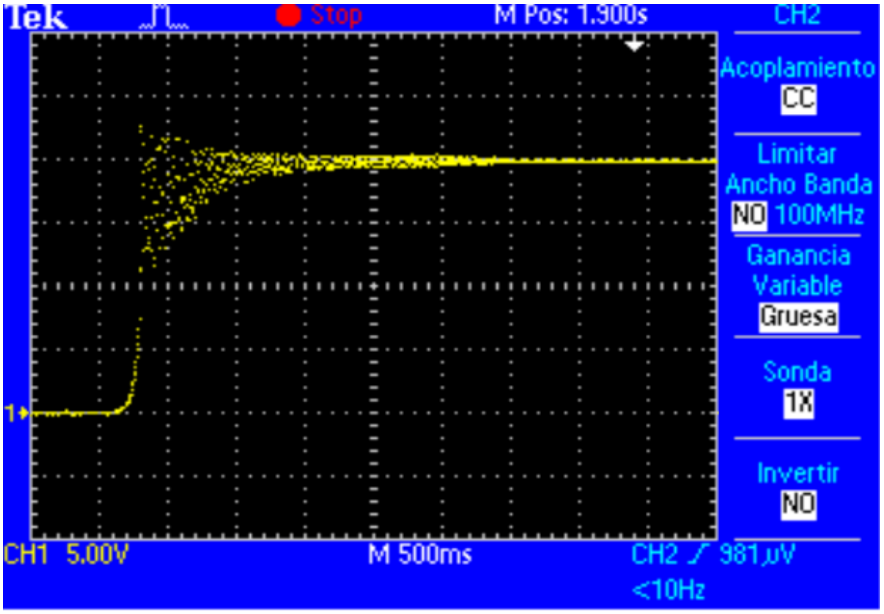
Figure 10. Output voltage, error and duty cicle with $K_s = 2$

Next, a variation of the control parameter K_s from 0 to 2 is carried out, having the control parameter $N = 1$ fixed. This is performed in order to determine the dynamics present in the system variables when the parameter K_s is changed. Figure 11 shows the dynamics present in the controlled variable υ_c for a range of K_s values between 0 and 2. Figure 11 (a) shows the simulated results and Figure 11 (b) shows the results obtained experimentally. In this Figure, from 1.2 to 2 the system is regulated and the error present in this zone is less than ±0.5 %. For values of the parameter K_s less than 1.2, the system does not regulate well, chaos is presented, and the error increases until the system is switched OFF. In the simulated bifurcations diagrams, there are nT periodic orbits when the control parameter K_s is changed, which are not observed in

the experimental results, as the sampling would have to be synchronized in the real model as in the simulation. However, there are noises that are added to the real signals. Figure 11 (b) shows the bifurcation diagram obtained with the experimental test on a Tektronix TDS2014 oscilloscope, channel one (CH1) with a gain of 5 volts per division. Therefore, the signal has low error in the steady state operation for values close to 2. Figure 12 shows the error obtained in the experimental test. This image was obtained by using the acquisition interface with board DS1104. The error obtained is less than 3% for all K_s values greater than 0.7; thus, we can conclude that the controller regulates well the output voltage of the circuit.



(a)



(b)

Figure 11. Bifurcations diagram in υ_c vs. K_s: (a) simulation test, and (b) experimental test

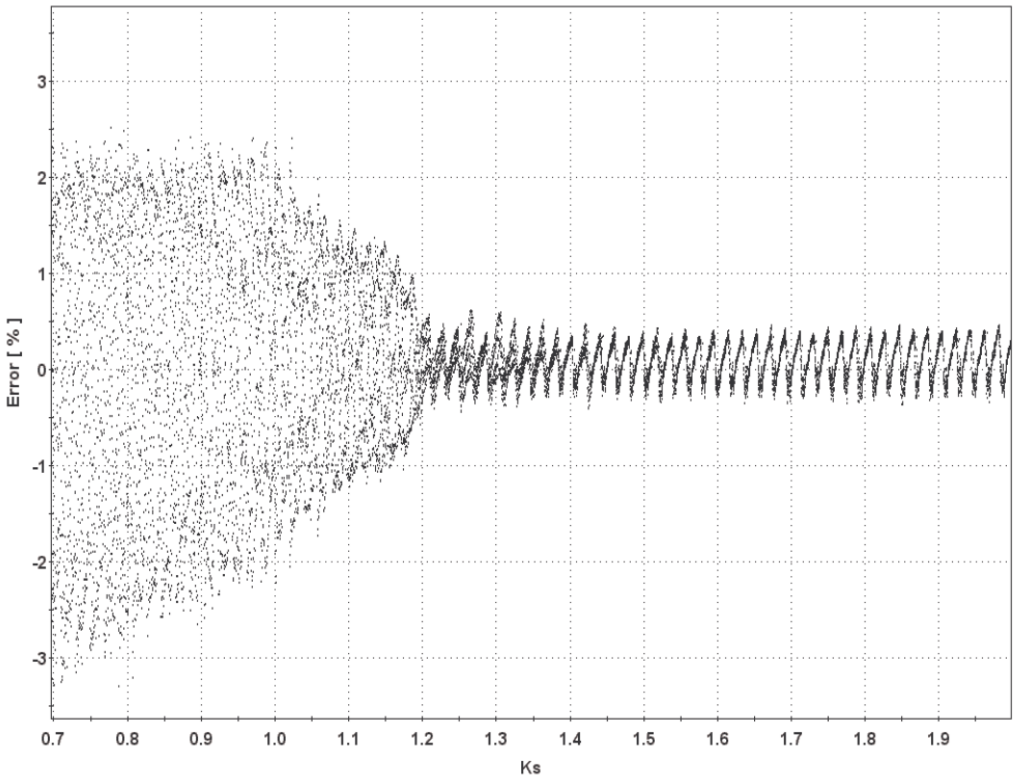


Figure 12. Experimental bifurcations diagram error vs K_s

5. CONCLUSION

The ZAD and FPIC controllers implemented digitally in a DSP meet the requirements of fixed frequency switching, robustness and good performance in DC signal regulation tasks. Bifurcation diagrams of the output voltage υ_c are shown for a range of the control parameter K_s between (0 and 2), it is concluded that the simulated and the experimental results are qualitatively and quantitatively similar. Bifurcation diagrams obtained experimentally for regulation of DC signals with $N = 1$, it is concluded that for large values of K_s the system regulates well with errors in voltage less than 0.5%. If the value of K_s is reduced, an area is reached where the system begins to regulate with greater error, showing nT periodic oscillations. Then, when reducing the parameter K_s further some chaotic dynamics are presented and therefore greater instability. The critical value of stability calculated numerically was verified experimentally, being an important part of the design in the experimental prototype.

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