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Study and Design of 40 nW CMOS Temperature Sensor for Space Applications

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Abstract

In the present study, a novel CMOS temperature sensor based on sub-threshold MOS operation has been presented, which is designed for space and satellite applications. The proposed CMOS temperature sensor is enunciated a good linearity between temperatures range from -60^{O}C to 150^{O}C with inaccuracy of -1.8^{O}C. This circuit is operated at supply 1V and static power consumption 40nW at 150^{O}C is achieved. The circuit utilizes the temperature dependency of threshold voltage of MOSFET, which gives two types of voltage in output, first voltage proportional to absolute temperature (PTAT) and second, negative temperature coefficient (NTC). The sensitivity of both PTAT and NTC is 0.16390mV/^{O}C and 0.17607mV/^{O}C respectively between the specified range -60 ^{O}C to 150 ^{O}C. This circuit is designed & simulated using Cadence analog & digital design tools UMC90nm CMOS technology. The layout area of the circuit is 17.213µm × 6.655µm.

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Keywords: *CMOS; complementary metal oxide semiconductor, temperature sensor, PTAT, proportional to absolute temperature, NTC, negative temperature coefficient, low power*

1. Introduction

Temperature is very important physical quantity in our daily life. It is applied in various fields such as industrial, medical, space and defense etc. In aircraft, the temperature monitoring play important role in fuel consumption, environmental cooling systems, oil in hydraulic, lubricating system, fluid in coolant, heating systems and avionics systems [1]. Today it's heavy demand of the CMOS temperature sensor due to use in thermal management. The advantage of CMOS based efficient temperature sensor is monitoring the steady increase of heat dissipation in different system. It is required to track the process temperature and regulate its cooling fan.

Temperature sensors are commonly divided into two type (a): conventional sensors (b): smart sensors. The conventional temperature sensors are having numerous drawbacks when compared to the smart temperature sensors specially manufactured in CMOS technology consuming more power due to the larger area, less accurate and non-linearity [2]. The smart temperature sensor can directly communicate with a microcontroller / microprocessor in a standard digital format, result reducing the complexity and enhance the response of the system. CMOS Smart temperature sensor circuit consist temperature cell circuit, its signal conditioning circuit and Analog to digital converter [3]. In silicon based MOSFET there is much property which depends on temperature. On the basis of literature report, the smart temperature sensor further designed in to (i) Parasitic BJT based temperature sensor, (ii) delay-Inverter based temperature sensor, (iii) Threshold voltage temperature sensor.

CMOS technology is used to realize parasitic BJTs which based on lateral PNP transistors have been realized achieve challenges related to temperature sensing like less accuracy, consuming more power, and occupying a large area. Now CMOS technology is growing and semiconductor industry adopted this technology frequently due to low fabrication cost and easy fabrication process. The temperature-sensing accuracy of BJTs is limited by the effect of their saturation current (I_S), which can lead to errors of a few degrees. But this error can be reduced ±0.1 by using the calibration [4-7]. Since for reducing the inaccuracy, the calibration technique is needed, but this increases the cost of the system. The bipolar technology is compatible with temperature sensing systems. It was also much more accurate than

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conventional temperature sensor. But there are use at least two PNP transistors, result increases the size of the chip.

Propagation delay-based temperature sensor is designed on the concept of the propagation delay of inverters. Delay line based temperature sensor consumes less power than a parasitic BJTs temperature sensor. The delay is a function of temperature for this type of sensor. For the digitization we need time to digital converter. Subsequently, the output pulse is fed to the input of a cyclic Time-to-Digital Converter (TDC) to generate the corresponding digital [8-10]. The same technique can be also be implemented in another way by measuring the variation in frequency of oscillation caused by variation in temperature. The frequency is inversely proportional to temperature because the decrease in the mobility is the dominant feature [11-12]. Both of these kinds of sensors require a larger chip area and produces difficulty in attaining linearity for the higher range.

To overcome the limitation of CMOS technologies in various temperature sensors (as discussed above), we opted threshold voltage, temperature sensor with for the application in the avionic system, owing to good accuracy with minimum power consumption. The temperature sensors based on the threshold voltage of MOSFETs are known for their lower power consumption and smaller die area [13-16]. The voltage or current across MOSFETs is always varies with the temperature, but the challenge is designing these types of sensors is accuracy. Because linearize this variation is a difficult task. This task is accomplished by proper selection of circuit architecture and adjusting the W/L ratio of the transistors used so that the non-linearity can be reduced.

The rest of this paper has been organized as follows. The characteristic of MOSFET operating in Basic Principle of MOSFET based temperature sensor is given in Section II. Section III describes the methodology and architecture of the proposed temperature sensor circuit. The simulation result and discussion has been summarized in Section IV. Finally, the conclusion of the overall paper is illustrated in Section V.

2. Basic Principle

The small signal analysis the square law of model is not longer holds true. Therefore, we cannot neglect the second order effect. The second order effect will cause temperature nonlinearity.

On chip thermal sensing demonstrates several degree Celsius temperature errors [16] due to nonlinearity. For short channel devices, the effect of velocity saturation and mobility degradation on the drain current in the saturation region [17-20] is defined as:

$$0 \le V_{GSn} - V_{Tn} \le V_{DSn}$$

$$I_D = \frac{\mu_n c_{ox} w}{2l}\left[\frac{\left(V_{GSn} - V_{Tn}\right)}{\left\{1+\left(\frac{\mu}{2lV_{sat}}+\theta\right)\right\}}\right] \quad (1)$$

Where,

V_{GSn} = Gate Source voltage V_{DSn} = Drain Source voltage V_{Tn} =Threshold voltage I_D = drain current of MOS transistor μ_n = mobility of N-type material c_{ox} = oxide capacitance w = channel width of MOS transistor l = channel length of MOS transistor V_{sat} = μ_n E = $10^7 m/s$ constant saturation velocity θ = fitting parameter $\left(10^7 / t_{ox} V^{-1}\right)$

The drain current is temperature dependence of CMOS transistor directly. Since drain current depends upon the threshold voltage and the mobility. The threshold voltage depends upon temperature as shown in equation (2-3):- [21-22].

Where $V_t = V_{to} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$ (2)

And,

$$V_{to} = V_t(V_{SB} = 0) = V_{FB} + 2|\phi_F| + \frac{\sqrt{2q\varepsilon_{si}N_{SUB}\,2|\phi_F|}}{c_{ox}} \quad (3)$$

Where,

$\gamma =$ Bulk Threshold Voltage, $\phi_F =$ Strong Inversion Surface Potential, V_{FB}=Flat Band Voltage, $Q_{SS} =$ Oxide-charge= qN_{SS}, $k =$ Boltzmann's constant, $T =$ Temperature (K), $n_i =$ Intrinsic carrier concentration.

$$V(T) = V(T_0) - k(T - T_0) \quad (4)$$

From Equation (4) it is proved that Threshold voltage decreases with increasing temperature hence the drain current increase. Therefore the drain current increases. This is the reverse dependence.

In MOS device mobility is important parameters that are predominantly sensitive to temperature. Theoretically Mobility of the carrier in the channel can be defined as [23-24].

$$\mu(T) = \left(\mu(T_0).\left[\frac{T}{T_0}\right]^k\right) \quad (5)\backslash$$

Where,

T_0 = Reference temperature T = Absolute temperature

Where k = constant value between -1.2 and 2.42 around room temperature, causing the mobility decrease by about half a percent per degree. The expression for the channel mobility can be further complicated by introducing velocity saturation and mobility degradation. This word means that the mobility at the reference temperature $\mu = \mu(T_0)$ depends upon the bias voltage and the threshold voltage. As temperature increases, the carrier mobility decreases and resulting drain current decreases. This is the normal dependence.
Threshold Voltage variation with the temperature

3. Proposed Circuit

The schematic diagram of temperature sensor circuit is shown in Figure 1. The proposed circuit is made by 4 NMOS and 3 PMOS transistors. Since in NMOS transistor, mobility is higher than the PMOS, therefore it is working as better switch and PMOS work as better load. The load is working as a resistance and the resistance is directly related to temperature. The both output PTAT and NTC voltages have been extracted. In the proposed design the transistors PM1, PM2 and PM3 act as active load, which form the current mirror through transistors PM3, PM2 and PM1. From equation (6) it is clear that the aspect ratio of PM2 and PM3 decided the nature of temperature vs voltage. Since PM2 and PM3 form current mirror therefore the aspect ratio of PM2 and PM3 should be same. This same current mirror helps in obtaining the voltage due to difference in current flow. The W/L ratios of the transistors configured as active resistors are also suitably adjusted for linearization of the output voltages.

The transistors NM1 and NM2 and NM3, NM4 are important in terms of controlling the NTC output voltage range with respect to the temperature range. This output voltage range is given by the W/L ratios of these transistors. From equation (7) it is clear that the NTC voltage depends upon the aspect ratio of transistor NM1 and NM2. For controlling the power consumption of the circuit the transistor NM3 and NM4 are very important. The biasing current should be optimized properly because it not only limits the power consumption of the circuit, but also defines the upper limit of the temperature to be sensed [15].

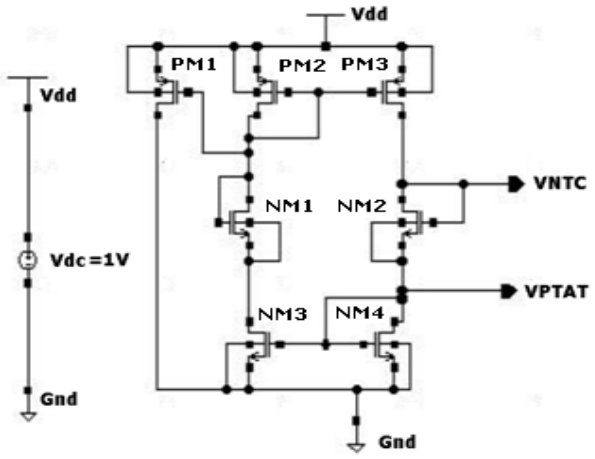

Figure 1. Circuit diagram of CMOS Temperature Sensor Cell

$$V_{PTAT} = V_T\left(1+\frac{3\lambda_{P23}}{\lambda_{P23-}2\lambda_{N12}}\right) = k_1 V_T \quad (6)$$

$$V_{NTC} = V_T\left(1+\frac{2\lambda_{N12}}{\lambda_{P23}-3\lambda_{N12}}\right) = k_2 V_T \quad (7)$$

Where $\lambda_{P23} = \dfrac{W_{P2}/L_{P2}}{W_{P3}/L_{P3}}$

Where $\lambda_{N12} = \dfrac{W_{N1}/L_{N1}}{W_{N2}/L_{N2}}$

4. Simulation Result & Discussion

The proposed temperature sensor circuit has been simulated in Analog Design Environment of Cadence using UMC90nm library. This circuit uses a 1V supply. The PTAT and NTC characteristics have been extracted from the circuit. The proposed circuit has been designed for sensing temperature from -60^{o}C to 150^{o}C and shows a good linearity between these ranges. The PTAT voltage gives an output voltage of 384.51987mV at -60^{o}C and 418.93929 at 150^{o}C. The sensitivity for V_{PTAT} is 0.16390mV/^{o}C. The NTC voltage shows an output voltage of 675.44597mV to 639.35949mV for the temperature range of -60^{o}C to 150^{o}C respectively with a sensitivity of 0.17607mV/^{o}C. Both V_{PTAT} and V_{NTC} curves has been shown in Figure 2(a).

The maximum deviation from actual value at any given temperature in between the specified range of the sensor is known as inaccuracy of any temperature sensor. The inaccuracy of NTC voltage in a specified range of the proposed sensor is -1.8^{o}C respectively. The error of NTC shows better than the PTAT. The error curves for V_{NTC} are given in Figure 2(b).

The circuit has been simulated at different process corners to get the worst operating conditions. In semiconductor product manufacturing, a process corner method is used for IC fabrication of semiconductor wafers. In process corner is naming convention for to use two-

letter, because two types of MOSFET used in CMOS technology: namely NMOS for n-channel and PMOS for p-channel. On behalf of the mobility of MOS transistor there are three type corner rules: (i) typical (t), (ii) fast (f) and (iii) slow(s), which used fast and slow for carrier mobility that is higher and lower than normal, respectively. There are five process corners [25] are involved to simulated my proposed circuit namely: (i) typical-typical (tt), (ii) fast-fast (ff), (iii) slow-slow (ss), (iv) fast-slow (fnsp), and (v) slow-fast (snfp). The (i) to (iii) is called even corners because both types of devices affected same, hence there are no adverse effect of the logical correctness of the circuit. This means the devices can operate at slower or faster clock frequencies. The last two process corners are called as skewed corner and come to concern corners. That is why in the MOSFET, NMOS will switch much faster than the PMOS. This represents imbalanced switching can cause one edge of the output to have a much less slew than the other edge. The Figure 3(a) & Figure 3(b) shows the simulated result at different process corner of PTAT and NTC respectively.

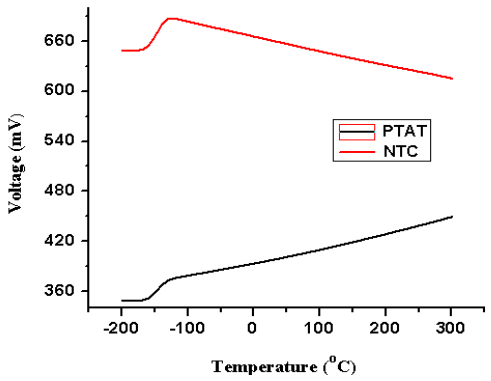

Figure 2(a). Output Voltage of Sensor with variation of Temperature

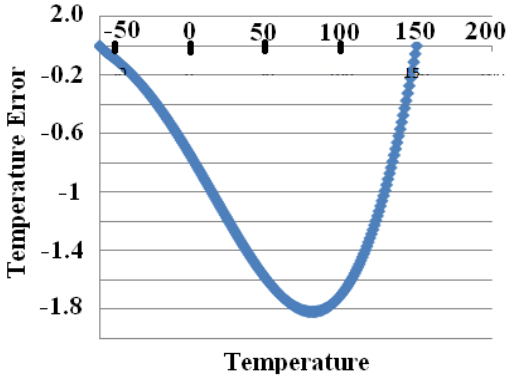

Figure 2(b). V_{NTC} Error of temperature cell

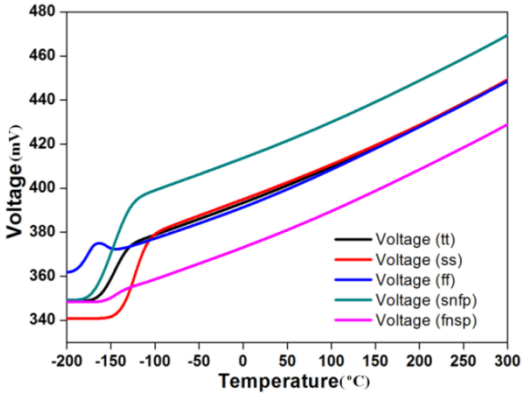

Figure 3(a). Temperature vs Voltage graph at different process corner in UMC 90nm technology of VPTAT CMOS Temperature Sensor

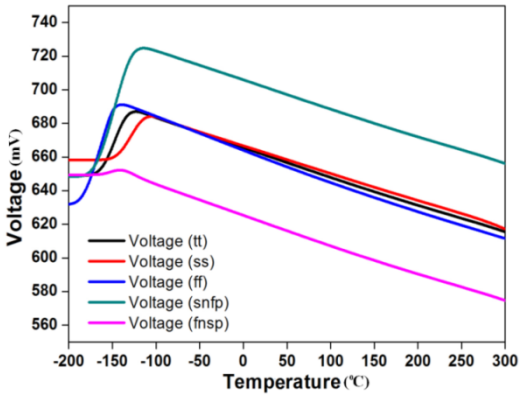

Figure 3(b).Temperature vs Voltage graph at different process corner in UMC 90nm technology of VNTC CMOS Temperature Sensor

Since power consumption of any CMOS circuit increases with increasing temperature. The circuit draws 40nA current from the circuit, which is shown in Figure 4. Therefore the overall resultant power dissipation of the proposed sensor is 40nW at 150°C.

The layout of proposed circuit is shown in Figure 5. The layout area of the cell is 17.213μm ×6.655μm. The designed layout of the cell is finally checked with DRC, it is fully error free and fully matched with LVS.

In Table 1 the proposed temperature sensor has been compared with recent works. The

V_{NTC} from the designed sensor is chosen for comparison as it produces better result than V_{PTAT}. From the table it can be seen that the power dissipation and inaccuracy is better than other result, while the temperature range is quite large. The inaccuracy increases with range. But, the proposed design maintains the inaccuracy in check, well within -1.8°C.

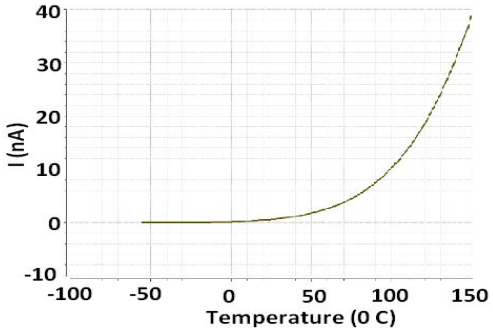

Figure 4. Drawn current from power supply of CMOS Temperature Sensor Cell

Table 1. Performance Summary & Comparison of proposed temperature sensor with recent works

Parameter	[12]	[15]	[26]	This work
Technology	1 µm	90 nm	180 nm	90 nm
Power Supply	1 V	1 V	0.6–2.5 V	1 V
Temperature Range()	+10 to +100 °C	-60 to 150 °C	+10 to120 °C	-60 to150 °C
Inaccuracy with Temperature	+1 °C	±1.3 °C	±2 °C	-1.8 °C
Power Consumption	100 µW	862 nW	7 nW at 0.6V	40 nW
Circuit Area	-	-	0.002 mm^2	114.55 µm^2

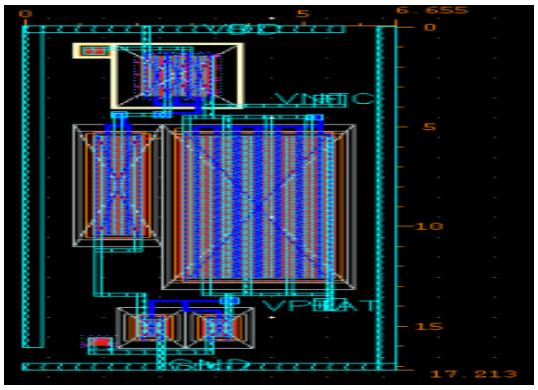

Figure 5. Layout of Proposed Temperature Sensor Cell

5. Conclusion

The circuit designed and simulated using cadence analog and digital system design tool UMC90 nm technology. The temperature sensor circuit presented in this paper utilizes the variation in threshold voltage with temperature to produce PTAT and NTC voltage signal. The NTC voltage produces better result in terms of accuracy for the designed sensor. Moreover the circuit senses for temperature range of -60°C to 150°C, which is spread over 210 degrees. The accuracy of the circuit is also quite good in specified range of temperature range. The layout area of this circuit is 17.213µm ×6.655µm and its power dissipation is 40nW. Since the proposed sensor senses for a widespread range of temperature with satisfactory accuracy the sensor can find its application in military and aerospace applications.

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