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Investigation and design of ion-implanted MOSFET based on (18 nm) channel length

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ABSTRACT

The aim of this study is to invistgate the characteristics of Si-MOSFET with 18 nm length of ion implemented channel. Technology computer aided design (TCAD) tool from Silvaco was used to simulate the MOSFET's designed structure in this research. The results indicate that the MOSFET with 18 nm channel length has cut-off frequency of 548 GHz and transconductance of 967 μS, which are the most important factors in calculating the efficiency and improving the performance of the device. Also, it has threshold voltage of (-0.17 V) in addition obtaining a relatively small DIBL (55.11 mV/V). The subthreshold slope was in high value of 307.5 mV/dec. and this is one of the undesirable factors for the device results by short channel effect, but it does not reduce its performance and efficiency in general.

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1. INTRODUCTION

For high demand of faster and smaller electronic devices, the researchers and semiconductor manufacturers are putting a lot of efforts to face the difficulties and challenges of improving the performance of the semiconductor devices from the conventional one. One of the solutions is to reduce the channel length of the device so that the structure of the MOSFET is not totally changed but the device performances are improved. The nowadays technology, MOSFET is the dominant device used in VLSI and ULSI circuits [1-5] because it can be scaled down to nono dimensions than other types of transistors. As a result of the great development in the techniques required to manufacture devices with dimensions below a micron, there appeared technical limitations related to the basic limits of the dimensions of the device based on physical laws. There are three main determinants [6, 7], the first is the limitations of the device itself, the second is connectivity limitations, finally is the power limitations.

The dramatic development of field-effect transistors manufacturing technology has enabled the growth of modern integrated circuit technology as well as the manufacture of electronic computers, and despite advances in technology for field-effect transistors [8, 9], Bipolar Junction Transistors (BJTs) remained dominant over the technologies of manufacturing transistors during the 1960s and 1970s due to Benefits and better performance compared to field effect transistors [10, 11]. And that the technology of manufacturing field-effect transistors requires less manufacturing steps than those required in the manufacture of bipolar junction transistors (BJT),

then there was a decrease in cost and productivity of more field -effect transistors, in addition to that the technology of bipolar junction transistors could not be reduced without size loss in properties Its performance, while it was possible to reduce the size of field effect transistors and without compromising performance characteristics [12], but to reduce the size (field effect transistors) reduced power consumption, increased speed and allowed a huge number of them to be manufactured in integrated circuits (IC) [10]. All of this led to the increase in the growth and development of the field effect transistors, and at the end of 1970 the field effect transistors became the dominant in the industry of integrated circuits instead of two-segment transistors [12]. Now field-effect transistors and complementary transistors now control over 90% of commercial semiconductor manufacturing technologies [13]. Field-effect transistors industry has become the most sought -after and interested field in research and manufacturing techniques because of its many specifications and practical applications compared to other types of devices. These manufacturing techniques are very precise and sophisticated processes, and these technologies have witnessed large and varied stages of development during the past decades. The doping process has been replaced by diffusion with the ion implantation, the process of thermal oxidation was replaced by the deposition of oxide, and the metal gates were replaced by polycrystalline silicon gates with silicides [14].

The field effect transistor of the enhancement and depletion mode has been designed with improved performance, high speed, and reduced power consumption [15], gate length was 85 nm for both types, with voltage drop on drain has a value of 0.5 V, and the first time used InSb instead of silicon, The results showed: Cutoff frequency 305 GHZ (enhancement) 256 GHZ (depletion) and Subthreshold Slope (SS) 105 mV/dec (enhancement) 140 mV/dec (depletion) and drain-induced barrier lowering current (DIBL) 95 mV/V (enhancement) 180 mV/V (depletion), the research showed that the cutoff frequency increased by 50% and the power consumption was reduced by 10 times for the enhancement type transistor compared to the transistor made of silicon. MOSFET (n-type channel) has been designed with a gate length of 40 nm and using germanium as a base material to improve efficiency and compare the results extracted with MOSFET made of Si as the base material [13], the results of the research showed that the cutoff frequency f_T=252.6 GHz, transconductance gm=1610 μS, threshold Slope SS=97.5 mV/dec and drain-induced barrier lowering DIBL = 231.9 mV/V. In short-channel devices, the voltage of the drain has an effect on the electron barrier height, which shows as a difference in the threshold voltage with the drain bias voltage, and the effect of (DIBL) is worse in the case of reducing the length of the channel, which results in the penetration state (the condition in which the two depletion region clashes and the gate lose its control in the current) [14].

Finally, the effects of the other short channel is what is related to the switching off state of the transistor (turn -off), that is, any change in the gate voltage causes a change in the drain current (ten gradations) known as the subthreshold slope (SS) and measured in mV/dec unit, and the subthreshold region, is the region where the gate voltage is less than the threshold voltage ($V_T > V_{GS}$), and when we reduce the transistor size and reduce the gate length, the subthreshold slope (SS) decreases, and the range of the practical values from 70 mV/dec to 100 mV/dec which is more than the theoretical value range about 60 mV/dec. As long as subthreshold slope SS was least possible, the better switching of the ON and OFF state of the transistor, but the physical properties of the device determine the lowest possible SS value at 60 mV/dec [16-18].

The convenential silicon MOSFETs have problems with intruding circuit elements that are inherent to them, which are the connection capacitors, and one of the ways to overcome these problems is to manufacture silicon MOSFET on insulating substrate, and there are two methods, the first (the primary method) in which a layer of silicon growth on a sapphire blue ground called silicon -on-sapphire or SOS, the second (more modern method) is the growth of silicon above the insulator SOI. It is one of the technologies that contributed to the development of the electronics industry. It includes building (installation) a traditional MOSFET on a very thin film of polycrystalline silicon, and separates this thin film of silicon from the substrate material with an insulating material (relatively thick), and this material (SiO_2) is embedded inside the substrate material. Thus, this technology makes the (MOSFET) electrically isolated from the substrate material, but the device manufacturing processes in (SOI) technology face some challenges, due to the difficulty of producing a very thin film of polycrystalline silicon with high quality, and the difficulty of growth (polycrystalline silicon) on the surface of the insulation material (SiO_2) without occurrence of any effective electrical effects or mechanical pressure [19].

2. RESULTS AND ANALYSIS

Figure 1 represents the (proposed) design of the (n channel) NMOSFET with a gate length of 18 nm using TCAD by Silvaco. The channel length of the transistor is one of the most important factors in the design process, because it represents and determines the technology generation. Although the length of the channel affects relatively the features of the performance of the device, the operation speed of the ICs is very closely related to the length of the MOSFET's channel, and it is inversely proportional to the length of the channel.

In the case of reducing the MOSFET (reducing the channel) the frequency will increase too much, and the electric field inside the device will increase, and this increase in the electric field leads to the appearance of the so - called short channel and hot electron effects [20-22]. Figure 2 shows the relationship of current with the gate voltage at the gate length (20 nm) and (18 nm) and with V_{DS} = 0.1V, the value of the current at the gate length 20 nm was 0.3 mA and the value ofthe current at the gate length 18 nm is equal to 0.8 mA, this mean the current increases as the length of the channel decreases, and this is due to the inverse relationship between the current and the length of the channel according to the following current equation [23]:

$$I_D = k_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] \quad (1)$$

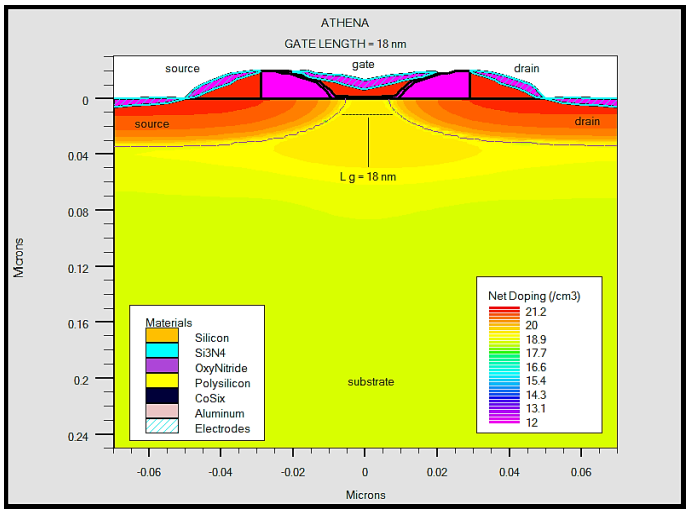

Figure 1. Proposed Ion-Implemented MOSFET structure (n channel) with 18 nm

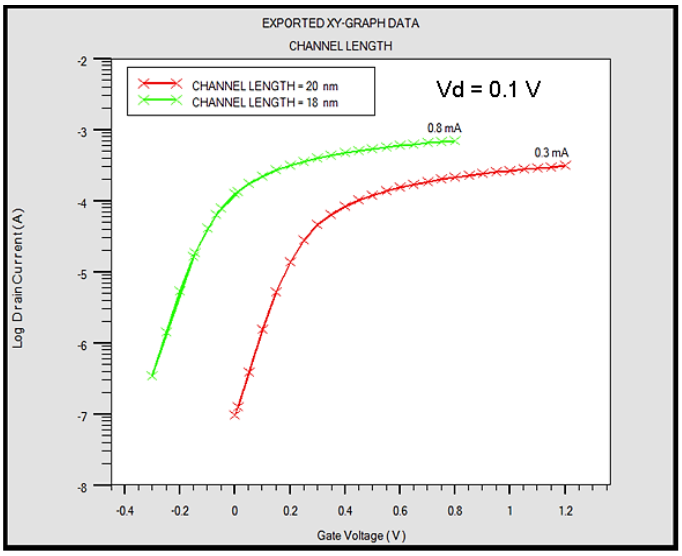

Figure 2. I_D current with the gate voltage at the gate length (20 nm) and (18 nm) and at V_{DS} = 0.1V

As for threshold voltages, the threshold voltage value at the gate length was 20 nm equal to 0.129 V and the threshold voltage value at the length of the gate is 18 nm equal to (- 0.17 V) as shown in Figure 3, we note that the threshold voltage decreases whenever the channel length is shortened due to the short channel effect, what happens as a result of the short channel is the sharing of source and drain charges on the one hand with gate electronic charge on the other hand, this reduces the gate voltage value needed to cause the conversion layer and then reduces the threshold voltage value [20].

Figure 4 shows the relationship of the subthreshold slop (SS) with the gate length at V_{DS} = 0.1V, it is clear that at the gate length 20 nm that the slope (SS) value is 81.86 mV/dec and the slope (SS) value at the gate length 18 nm is 307.5 mV/dec, that is: the value of the slope (SS) is inversely proportional to the length of the channel, and the slope (SS) always increases with a decrease in the length of the channel. The reason for this is due to the short channel effect as well. As known, the lower the slope (SS) value, the better. Therefore, the (relatively large) values of the subthreshold slope (SS) at the short channels are the undesirable factors for the device, but they can be overlooked in return of other benefits such as frequency [18].

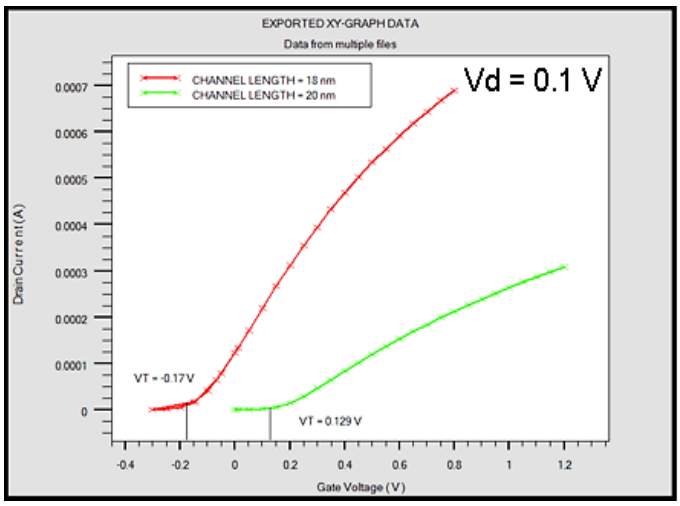

Figure 3. Threshold voltage V_T at the length of the gate is 18 nm and 20 nm

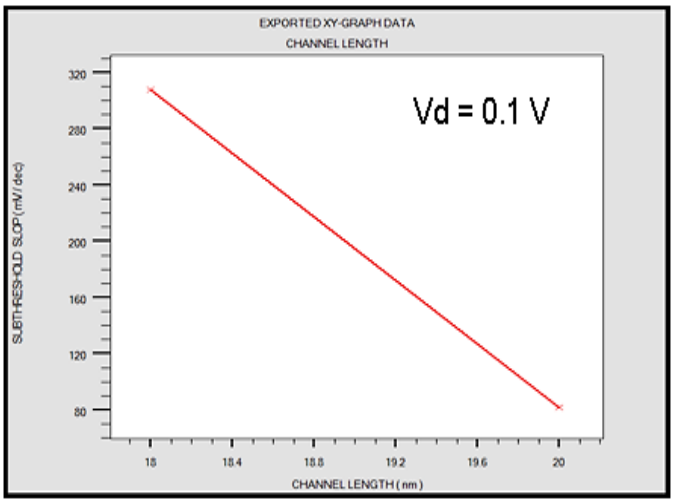

Figure 4. Subthreshold slop (SS) with the gate length at Vd = 0.1V

Figure 5 shows the relationship of the drain-induced barrier lowering current DIBL with the gate length at V_{DS} = 0.1V, and we notice at the gate length (20 nm) that the value of DIBL is 23.6 mV/V and the value of DIBL at the gate length (18 nm) is 55.11 mV/V, i.e., the value of DIBL is inversely proportional to the length of the channel, and the lower the value of the extracted DIBL the better, and the reason for the increase in DIBL with a decrease in the length of the channel is due to two reasons, the first: the electrostatic interaction between the source and the drain, a situation that is not desirable, and the second reason is due to the short channel effects. To overcome this problem, a second gate or so-called double gate is used to completely control the short channel effects [24].

Figure 6 shows the greatest transconductance values (g_m) at gate length (20 nm) and (18 nm) and at V_{DS} = 0.1V, so, the greatest transconductance value at gate length 20 nm was 375.1 µS and the greatest transconductance value at gate length 18 nm Is equal to 967 µS, and we note that the lower of the channel

length, the greater the transconductance, and this is due to the inverse relationship between transconductance and the length of the channel according to (2) [25]. The increase in transconductance is an important factor in measuring the efficiency and performance of the device because it represents the transistor gain.

$$g_m = \frac{\partial I_{D(sat)}}{\partial V_{GS}} = \frac{W \mu_n c_{ox}}{L} (V_{GS} - V_T) \quad (2)$$

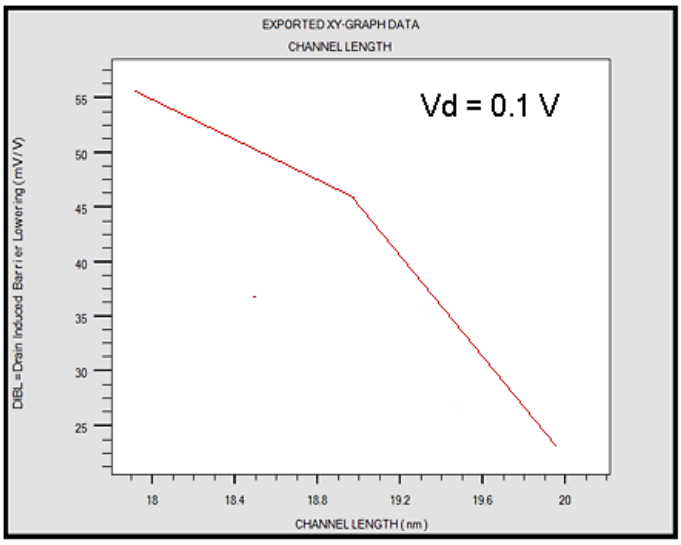

Figure 5. DIBL with gate length at V_{DS} = 0.1V

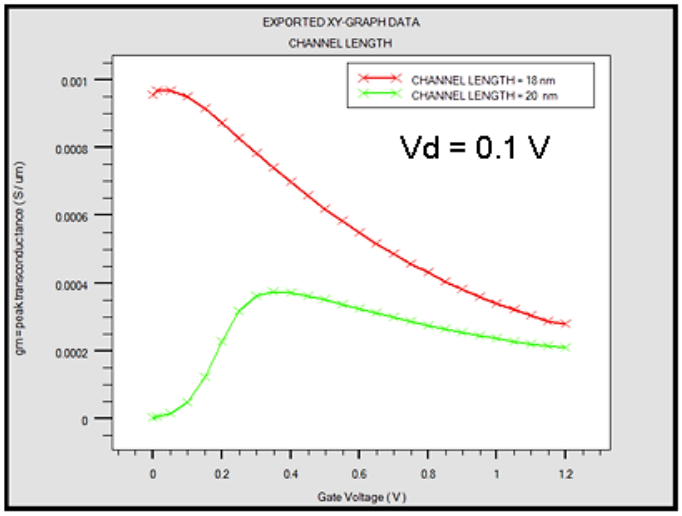

Figure 6. The transconductance (g_m) at gate length (20 nm) and (18 nm) and at V_{DS} = 0.1V

Figure 7 shows the cutoff frequency f_T at the gate length (20 nm) and (18 nm) with V_{DS} = 0.1V, the greatest cutoff value at the gate length 20nm was 368 GHZ and the greatest cutoff frequency value at the gate length 18nm equals 548 GHZ, as the channel length decreases, the cut-off frequency of the transistor increases, and the reason for this is the inverse relationship between the channel's length and the cut-off frequency according to (3) [25]. It is worth noting that the increase in the cut-off frequency is not always the result of the decrease in the length of the channel only, but the increase in transconductance g_m also results in an increase in the cut-off frequency due to the direct relationship between the transconductance and the cut-off frequency.

$$f_T = \frac{V_{sat}}{2\pi L} \quad (3)$$

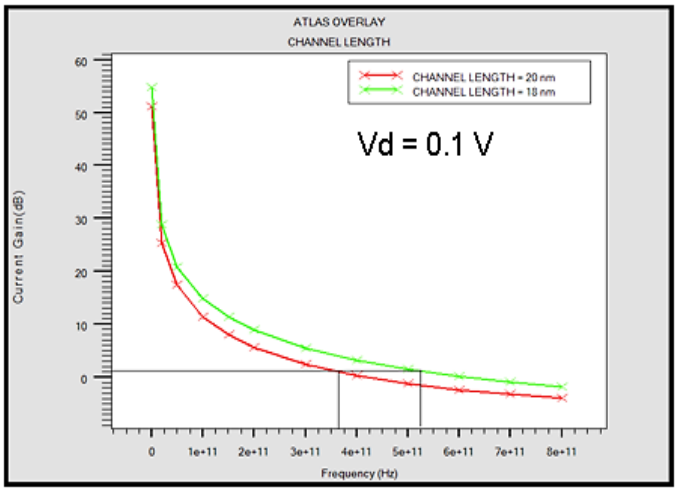

Figure 7. Cutoff frequency f_T at the gate length (20 nm) and (18 nm) with V_{DS} = 0.1V

3. CONCLUSION

The proposed design of ion-implanted N-hannel MOSFET's with (18 nm) channel length has been simulated by TCAD tool by Silvaco, the doping the channel with a concentration of $5*10^{14}$ cm^{-3} and using polycrystalline silicon as the gate material, The results indicates that a good value was obtained for the cut-off frequency which is 548 GHz and also a good value for the transconductance of 967 µS, and the cutoff frequency and transconductance are the most important factors in calculatin g the efficiency and improving the performance of the device, Also, a small value was obtained from the threshold voltage -0.17 V in addition to obtaining a relatively small value from DIBL which is 55.11 mV/V, while the values of subthreshold 307.5 mV/dec were high, and knowing that these relatively large valu es for the subthreshold at the short channels is one of the undesirable factors for the device, but it does not reduce its performance and efficiency in general, the current value was 0.8 mA. With all the results obtained from this design, do not forget the most important result that was the primary purpose of the research, which is to reduce the size of the device (gate length) to the lowest possible physical dimension, which is 18 nm.

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