TELKOMNIKA Telecommunication Computing Electronics and Control
Vol. 20, No. 1, February 2022, pp. 221~234
ISSN: 1693-6930, DOI: 10.12928/TELKOMNIKA.v20i1.21671

Modeling and characterization of optimal nano-scale channel dimensions for fin field effect transistor based on constituent semiconductor materials

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Article Info

Article history:

Received Mar 17, 2021
Revised Oct 09, 2021
Accepted Oct 20, 2021

Keywords:

Channel dimensions
FinFET
I_{ON}/I_{OFF} ratio
MuGFET simulator
Subthreshold swing

ABSTRACT

This study aims to design an optimal nano-dimensional channel of fin field effect transistor (FinFET) on the basis of electrical characteristics and constituent semiconductor materials (Si, GaAs, Ge, and InAs) to overcome issues regarding the shrinking of dimensions and ensure the best performance of FinFETs. This objective has been achieved by proposing a new scaling factor, K, to simultaneously shrink the physical scaling limits of channel dimensions for various FinFETs without degrading their performance. A simulation-based comprehensive comparative study depending on four variable parameters (length, width, oxide thickness of the channel, and scaling factor) was carried out. The influence of changing channel dimensions on the performance of each type of FinFET was evaluated according to four electrical characteristics: i) ON-state/OFF-state current (I_{ON}/I_{OFF}) ratio, ii) subthreshold swing (SS), iii) threshold voltage, and iv) drain-induced barrier lowering. The well-known multi-gate field-effect transistor (MuGFET) simulation tool for nanoscale MuGFET structure was utilized to conduct experimental simulations under the considered conditions. The obtained simulation results showed that the optimal channel dimensions for the best performance of all considered FinFET types were achieved at a minimal scaling factor K=0.125 with 5 nm length, 2.5 nm width, and 0.625 nm oxide thickness of the channel.

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1. INTRODUCTION

Nano-electronic applications have benefited enormously from substantial advancements in the emerging nanotechnology industry. The tremendous downscaling of transistor dimensions has enabled the placement of over 100 million transistors on a single chip, thereby resulting in reduced cost, increased functionality, and enhanced performance of integrated circuits (ICs) [1]-[3]. However, reducing the size of conventional planar transistors would be exceptionally challenging due to electrostatic leakages and other fabrication issues [4], [5]. The application of nano-science and its inherent technology has been extensively used in interdisciplinary research, particularly in the past two decades [6], [7].

Nanotechnology involves the use of low-dimension materials with different structural configurations; such materials include nanowires (NWs), nano-rods, nano-tubes, or nano-crystalline films. This technology has therefore attracted interest in various science and engineering fields. The materials within the range of "1 nm -100 nm" exhibit

the nano-particle characteristics of bulk samples from the same material [8]. Describing the system of units and how small nanomaterials are bears importance. Examples of nanomaterials include human DNA strands (approximately 2.5 nm) and human hair (8-10×10^4 nm). These materials exhibit characteristics, including a large surface area, low thermal properties, high electrical resistivity, high specific heat capacities, excellent magnetic properties, and thermal expansivities. These properties are responsible for various applications of these materials in medicine, biotechnology, bioremediation, solar cell catalysis, and separation processes, and their recent uses in cancer therapy [9].

Fin field effect transistor (FinFET) shows great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies. The structure of FinFET provides superior electrical control over the channel conduction, thus it has attracted widespread interest from researchers in both academia and industry. However, aggressively scaling down of channel dimensions, mainly the channel length will degrade the overall performance due to detrimental short channel effects (SCEs). A number of researchers and engineers have exerted considerable efforts in discovering different varieties of nanoscale materials such as a field-effect transistor (FET)-based device. Such application is largely due to the improved properties, which include remarkable strength, lightweight, and high resistance to chemical reactions of these materials. In recent years, FETs have become widely prevalent in many ICs, especially with the evolution of the field of communication technology and the internet of things [10]. The wide use of FETs has, therefore, notably influenced the production of various electronic devices. The application of FET is largely based on the concept of the attraction of charges within a semiconductor channel. The FET comprises a semiconductor channel coupled with electrodes at either end of the drain and source. The gate is a control electrode lying in close proximity to the semiconductor channel. The configuration for electric charge effects enables the FET gate to effectively control the flow of electrons or holes (i.e., carriers) from the source to the drain. The flow of these carriers is achieved by controlling the size and shape of the semiconductor channel.

Scaling down the transistor from large to small dimensions has led to the emergence of IC production. This outcome could be traced to the need for minimizing transistors into basic units with smaller IC chips. As a result of size minimization (which at present has reached 0.1 microns), in the past 40 years, the metal–oxide–semiconductor FET (MOSFET) transistor has become the basis of micro-electronic manufacture of many computing devices. The reduction of transistors into a miniature entity with dimensions far below 100 nm has helped in the re-coupling and integration of numerous transistors on a single chip.

New FET structures are being explored on a large scale; these structures include the fin FET (FinFET), which is described as a MOSFET built on a material where the gate is supported by "2-4" channels or configured to form a dual gate structure. Figure 1 illustrates the structures of FinFET and its different channel dimensions. The gate structure form of FinFET looks like a group of fins. This technology entails a double-gate non-polar transistor built upon silicon on insulator (SOI) substrate. This form provides improved electrical control on channel delivery, reduces current leakage levels, and overcomes other short-channel effects (SCEs). FinFET devices feature significantly faster switching times and higher current density than the mainstream complementary metal-oxide-semiconductor (CMOS) technology. This transistor structure has attracted widespread interest from researchers in the industry and in academic investigations of semiconductors. Mack [11] reported that an achievable similarity in the quadrupling of devices in a chip and improved transistor performances occur every three years, according to Moore's law. Moreover, Dennard's scaling law states that such transistors achieve high speed, consume a low amount of power, and are cheap to manufacture by assuming a miniature form [12].

This paper involves simulation-based research that aims at the modeling and simulation of different types of FinFET transistors with various channel dimensions for distinct semiconductor materials. We used multi-gate FET (MuGFET) simulation tool to produce the output characteristics of FinFETs. This work was limited to the considered parameters and FinFET types. This research also focused on investigating the effect of shrinking channel dimensions (L, W, and T_{OX}) on the electrical characteristics of four types of FinFET transistor types (Si, Ge, GaAs, and InAs). The performance evaluation of FinFETs in this study was based on four electrical characteristics: ON-state/OFF-state current (I_{ON}/I_{OFF}) ratio, subthreshold swing (SS), threshold voltage (V_T), and drain-induced barrier lowering (DIBL). Depending on the highest I_{ON}/I_{OFF} and SS nearest to the ideal value, the best nano-dimensions of channel and semiconductor FinFET types were selected. This study adopted the following objectives and contributions:

- Simulation-based model for electrical characterization of FinFET transistors to simulate and analyze the electrical characteristics (i.e., I_{ON}/I_{OFF}, SS, V_T, and DIBL) of FinFET transistors according to channel dimensions (length, width, and oxide thickness) and semiconductor materials (Si, Ge, GaAs, and InAs);
- Propose a new scaling factor (K) for scaling down channel dimensions simultaneously to new nanoscale limits while maintaining acceptable performance of FinFETs with various constituent semiconductors;

– Design and modeling of a FinFET structure with optimal channel dimensions and semiconductor material according to the best performance characteristics. The obtained simulation results of this study will play a role in investigating the field of nano-electronic devices and can accelerate the development of FinFET applications in nanotechnology by introducing new nanoscale limits for different semiconductor FinFETs.

The remainder of this paper is organized as follows. Section 2 emphasizes the motivations of this work and summarizes previous related studies. Section 3 describes the adopted methods for this research along with the simulation environment. Section 4 investigates and compares the performance of FinFETs using simulations. Finally, section 5 presents the concluding remarks with directions for future work.

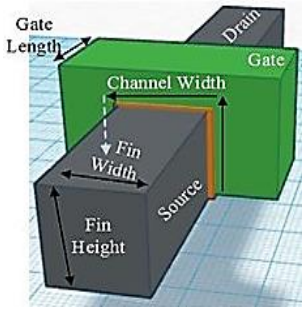

Figure 1. FinFET structure

2. BACKGROUND AND RELATED WORKS

2.1. Motivations and problem statement

Performance, speed, and density have been substantially improved through scaling-down of transistors from large to miniature dimensions. As planner MOSFETs continually shrink in size toward higher circuit density, the adverse consequences arising from SCEs became progressively important. Thus, following Moore's law and further scaling down of planar MOSFET devices became difficult. Numerous techniques have been introduced to sustain this trend and allow for more advanced nodes. In addition, the power dissipation of nanoscale devices is becoming a major concern with the current market scenarios and has increased drastically with the scaling down of transistors [13].

Several constraints that led to energy dissipations and other problems could be traced to an increase in current gate leakage due to the quantum mechanical tunnel of tankers through the thin gate. Oxide I_{OFF} increases due to the quantum mechanical tunnel of tankers from the source to the MOSFET drain. A lower I_{ON}/I_{OFF} ratio results from reduced density control and dopant atoms located in the channel and source/drain region. Another advantage is SS, which is defined as the change in gate voltage (V_G) required to change the order of the current amount from state to state [14]. SS is controlled in MOSFET by diffusing the thermal emission carrier across a thermal barrier and features an ideal value equal to or higher than 60 mv/dec at room temperature. Thus, further reduction of MOSFET without a significant increase in I_{OFF} and SS presents extreme difficulty [15].

Integrations of several circuits have considerably improved the function of semiconductors and reduced the cost for semiconductor industries. The reduction of production cost has aided in the speed of data transfer, lowered overall processing time, and improved computing power. These developments have invariably enabled the simultaneous performance of multiple tasks, which is the merit of transistor scaling. However, researchers are investigating several alternatives to the transistor for ultra-dense circuitry to tens of nanometers. This science is called nanotechnology, such as the latest FinFET technology demonstrated at the 10 nm channel length by the Intel company in 2017.

To overcome these issues, researchers have generated numerous plots depicting scaling trends over the years by showing the limit of critical dimensions. Additional new FETs are explored on a large scale. Substantial attention is being dedicated toward the fabrication of MOSFET with a vertical channel (such as an SOI wafer), which is often characterized as a FinFET. FinFETs possess the potential to be fabricated with a channel length of less than 25 nm as they can provide a high drive current and immunity to SCEs. The FinFET structure has attracted wide interest from both industry and academia. Such structures provide good control, reduce current leakage levels, and overcome other SCEs [16]. FinFET behavior must be simulated and characterized to help in decision-making on reducing channel dimensions and improving the performance of FinFET design. Hence, the lack of qualitative and quantitative characterization studies on FinFET as a successor to conventional planar devices is one of the major issues for understanding the electrical characteristics of FinFETs according to their channel dimensions and semiconductor materials.

As mentioned, numerous challenges, including electrostatic leakages and other fabrication issues, occur in the scaling trend of conventional planar transistors. Such problems arise because downscaling of channel dimensions results in the degradation of transistors. This degradation culminates in the reduction of I_{ON}/I_{OFF} ratio due to increased leakage current, which leads to substantial energy dissipation. Such a condition also causes an increased SS value, thereby slowing down the devices. Therefore, FinFETs present a high potential in scalability and manufacturability as a promising candidate in nanoscale CMOS technologies. However, downscaling of FinFET channel dimensions cannot be performed arbitrarily or in an ad hoc manner. Furthermore, the constituent semiconductor materials (such as Si, Ge, GaAs, and InAs) significantly influence FinFET performance due to SCEs. Therefore, the individual influence of each channel dimension on the performance of different FinFETs must be investigated according to the type of semiconductor materials and the effect of simultaneous downscaling of three-channel dimensions (L, W, and T_{OX}) according to the scaling factor should be further analyzed.

2.2. Related works

This section highlights the most recent related studies on nanoscale dimension effects on the electrical characteristics of FinFETs. Over the last decade, different types of research have focused on the manufacture of FinFETs in various nanoscale devices, such as semiconductor materials and insulation materials, and on different manufacturing techniques developed to predict the FinFET performance. Nevertheless, such investigations failed to focus on the full comprehension of the subject. For example, several studies concentrated on one channel dimension (that is, on either length, width, or oxide thickness) depending on one metric (such as I_{ON}/I_{OFF} or SS) and one semiconductor material (such as Si-FinFET or Ge-FinFET). A summarized literature review has also been introduced.

A study [13] focused on the physical insights into the scaling of Gaussian channel design of junctionless FinFET. In this study, junctionless FinFET with a Gaussian channel design was explored for its scaling capability in a nano regime. The device performance metrics, viz, the OFF-state current (I_{OFF}), I_{ON}/I_{OFF} ratio, DIBL, and SS, were also assessed as functions of gate dimensions. The researchers also compared and contrasted the proposed graded structure with the conventional uniformly doped junctionless FinFET structure. The Gaussian channel junctionless FinFET structure demonstrated superior performance according to the I_{ON}/I_{OFF} and SS with a channel length of 7 nm. However, a significant decline in DIBL performance was observed, resulting in a channel length below 14 nm. The researchers noted the low SS at 85 mv/dec, and DIBL of up to 100 mv/v can be obtained with Gaussian channel structure at 10 nm. Despite the evidence that the structure reached the length of the 10 nm gate, the SS value = 85 mv/dec and the DIBL value = 100 mv/v remain large.

Mobarakeh *et al.* [17] aimed to examine the SiGe-NW-FinFET performance. The authors proposed and conducted an analysis of different NW-FinFETs, including Si, Ge, and SiGe NW. They aimed to determine the extent to which doping concentration influences the channel length and dielectric thickness, thereby determining the SCE on I_{ON}/I_{OFF} ratio and DIBL. The researchers reported results illustrating the significant advancement of the considered parameters with Si structure in comparison with the other two structures used in the study. Specifically, their work revealed that the transistor's I_{ON}/I_{OFF} ratio might be improved by increasing the doping concentration, a change that was also found to affect DIBL. The results obtained from this comparison proved the superiority of the SiGe structure of FinFET and the former's suitability for analogous applications. However, this study failed to test the channel width and therefore showed no SS value that directly affects transistor velocity.

A previous study focused on the influence of cross-sectional shape on InGaAs FinFET performance at the 10 nm gate length [18]. The involved researchers examined the effect of shape on current-voltage (I–V) characteristics and induced variability. The authors claimed that the investigated performance metrics (OFF-current, DIBL, and SS) decreased with the triangular shape of the cross-section, and the I_{ON}/I_{OFF} ratio was three times higher compared with the rectangular-shaped counterpart. However, the obtained results were unsatisfactory relative to our findings at a lower dimension. Notably, although the SS was acceptable and approximated the ideal value, the obtained I_{ON}/I_{OFF} was low, an outcome that may result in increased energy dissipation. Das and Baishya [19] investigated the application of various structures of Ge-FinFET and compared their performance with conventional FinFETs. The new structures achieved low leakage current, which caused an increment in the I_{ON}/I_{OFF} ratio to 10^{13} and a decrement in SS value to 71 mv/dec at a channel length of 40 nm. In addition, the effect of fin thickness (T_{fin}) on V_T and SS were considered. Nevertheless, this study only focused on Ge-FinFET and ignored other constituent semiconductor materials. Moreover, only one channel dimension was examined.

A previous study focused on the influence of variation on geometry parameters on the performance of FinFET at 50 nm channel length [20]. Several performance indicators were evaluated: I_{ON}/I_{OFF}, SS, and DIBL, different gate lengths, and fixed-width and oxide thickness (L=20 nm, W=5 nm, and T_{OX}=0.9 nm). The

authors claimed that the considered metrics significantly improved with decreasing gate lengths. Hence, constraints of current leakage could lead to an increase beyond 10 nm. Therefore, the characteristics of FinFET revealed a significant improvement when gate length was maintained at 20 nm. However, when the value approximated the gate length of 12 nm, the leakage current became more serious. At this point, the threshold could no longer be ignored. Devices below sub-10 nm must be designed with optimal doping concentrations and mesh spacing to obtain good performance. The best results were $I_{ON}/I_{OFF} = 3.6\times10^8$, DIBL = 69.96 mv/v, and SS = 69.11 mv/dec. The data and results were modest enough, except for oxide thickness, which can be considered as a novelty.

A. Nejati *et al*. [21] examined FinFET as a temperature nano-sensor according to the type of semiconductor. FinFET temperature sensitivity was simulated for different constituent semiconductor materials (Si, Ge, GaAs, and InAs). The FinFET transfer properties with $V_d = 1$ V were investigated at different operating temperature values (-25 °C, 0 °C, 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C) for all semiconductor channel types. The outcomes indicated that GaAs-FinFET is best used as a nano-sensor as it features a larger ΔI (10.9 %) than the other types, thus showing a type II FinFET at 25 °C. The best stability of FinFET with the increment in operating temperature was obtained with Si-FinFET. This outcome is due to the minimum ΔI (6%) and classification of the transistor as type II at 25 °C. However, the leakage current (I_{OFF}) and SS values must be considered, particularly when studying modern complex sensor systems containing millions of sensors [22]. Table 1 presents a summary of related literature.

Table 1. Summary of the main findings of previous studies

References	I_{ON}/I_{OFF}	SS mV/dec	DIBL mv/v	V_T V	L nm	Material
[13]	_	85	10 0	_	10	Si
[17]	10^9	_	28		7	SiGe
[18]	4.7×10^4		67	_	10.4	InGaAs
[19]	10^{13}	71	_	0.46	40	Ge
[20]	3.6×10^8	69	69	_	20	Si
[23]	15.3×10^4	68	_	0.26	10	Si
[24]	10^5	71	_	0.6	200	Ge

3. METHODS AND MATERIALS

After reviewing the relevant literature and highlighting the limitations in the field of nanotechnology applications in relation to FinFETs, the problem statement of this research was identified, and four main phases were adopted for the general descriptive research methodology. These phases include different stages and research activities in conjunction with the detailed simulation environment as follows:

- Phase I: The FinFET transistor was considered the main focus of this study as it is the successor of FET-based nanoscale devices. Then, MuGFET was selected as the simulation tool to conduct the study due to its superiority and reliability in evaluating the performance of MuGFET transistors, particularly FinFETs and NW transistors.
- Phase II: Simulation and characterization of FinFETs were performed according to various channel dimensions (L, W, and T_{OX}), and the best performance per dimension was identified for different semiconductor materials of FinFETs.
- Phase III: According to the obtained results of Phase III, a new scaling factor, K, was proposed for scaling down all channel dimensions simultaneously to achieve new physical limits of channel dimensions.
- Phase IV: FinFETs with optimal nanoscale channel dimensions were designed for the best transistor performance. Finally, different FinFET performances were evaluated and compared on the basis of electrical characteristics for identifying the best constituent semiconductor materials.

This section explains in detail the procedure for the analysis of electrical characteristics of FinFET. Initially, we selected simulations from MuGFET. Next, the semiconductor type of FinFET was selected from the material option that enters the required semiconductor data. Channel dimensions (length, width, and oxide thickness) were subsequently included. After their extraction, electrical properties were plotted for the analysis and study of each type of semiconductor. These steps were repeated with variations of the proposed scaling factor, K, which was used to scale down channel dimensions simultaneously. The final evaluation and comparative analysis of FinFET performances were conducted, and optimal dimensions were designed using the proposed scaling factor to achieve new nanoscale limits for each semiconductor material (Figure 2).

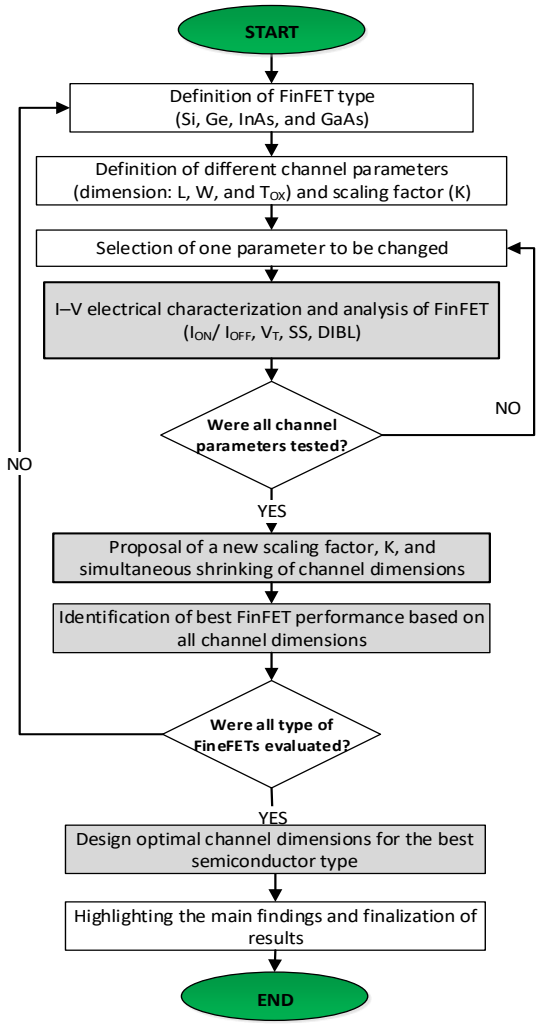

Figure 2. Flow chart of research methodology

3.1. Simulation tools

The use of simulations is an important tool that helps in the proper understanding of device behavior and performance evaluation. The application of simulation tools accelerates the development of FinFET and helps in providing support for experimental works carried out by industry researchers. Simulation tools present the benefits of reducing costs and identifying the strengths and weaknesses of various models and approaches. Such tools also benefit the demonstration of the viability of materials up to the nanometer range. Computer-assisted designs for nano-meter-scale semiconductor devices require an appropriate measure of mechanical quantum models in capturing the atomic accuracy of the simulation field. Most researchers in the field of nanodevices used to simulate proposed new structures and investigate their characteristics using available simulation tools. MuGFET is one of the simulation tools that are used to simulate the characteristics of FinFET. MuGFET is a simulation tool that solves the Schrodinger equation with open orbital conditions. The burden of calculation depends directly on the complexity of this basis. The size of Hamiltonian matrices depends on the orbits to describe the atom.

MuGFET utilizes either PADRE or PROPHET simulators, both of which are advanced by Bell Laboratories. PADRE is a device-oriented simulator for 2D and 3D devices with arbitrary geometry. PROPHET is a partial differential equation solver for equations with one, two, or three dimensions. MuGFET supplies useful plots for engineers but requires a deep understanding of physics. Therefore, MuGFET provides self-consistent solutions to Poisson and drift-diffusion equations [23]. MuGFET includes a provision for selecting either FinFET or Nanowire for simulation. Moreover, MuGFET simulates quantum transport at the nano-level, which approximates the atomistic dimension [25]. However, quantum transport exhibits a disadvantage that renders the drift-diffusion simulation type a superior tool. PROPHET and PADRE are drift-

diffusion-based simulators in this case. Either of the simulators can be used for FinFET, but only PADRE can be employed for Nanowire. Six different sections are involved, with each section featuring different parameters that can be varied according to requirements. The gate length, width, oxide thickness, and doping concentration can be altered. Other options are available after graph simulation; the options include I–V characteristics, train conductance, DIBL, and V_T as shown in Figure 3.

3.2. Simulation design

3.2.1. Selection of semiconductor material

The procedure followed for investigating the electrical characteristics of FinFET will be explained in detail in this section. Herein, four scenarios were considered to study the effect of channel dimensions (length, width, oxide thickness, and scaling factor) on FinFET performances (Table 2). The parameters of semiconductor materials were initially selected. As shown in Figure 4, Silicon (Si) was selected as a semiconductor, followed by GaAs, Ge, and then InAs. These materials were selected owing to their low cost and availability in nature. At the same time, they are typically used in the manufacture of ICs. For Si-FinFET, the parameters in the simulator are illustrated in Figure 5. For the environment, a 300 K temperature (room temperature) was selected, and channel voltage was varied from 0.5 V to 5 V with a choice of 21 points between the length and voltage gate as shown in Figure 6.

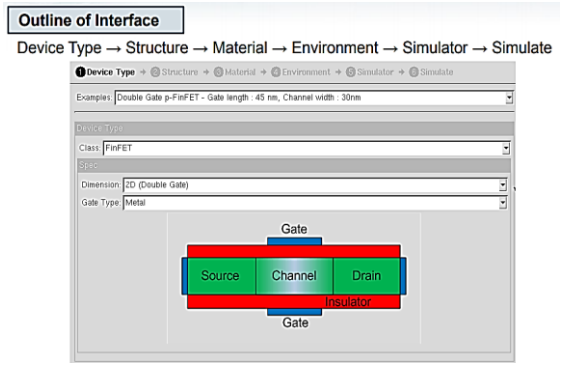

Figure 3. "MuGFET" simulation tool homepage

Figure 4. Parameter selection

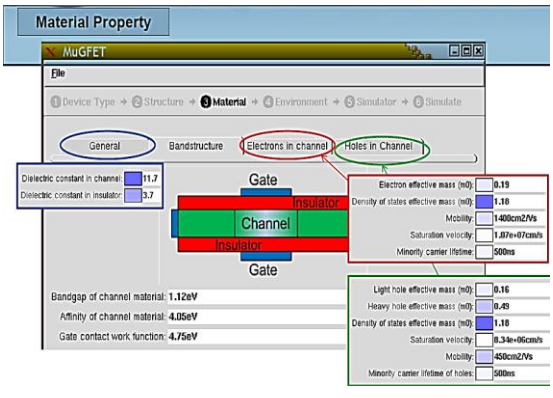

Figure 5 Selection of silicon parameters

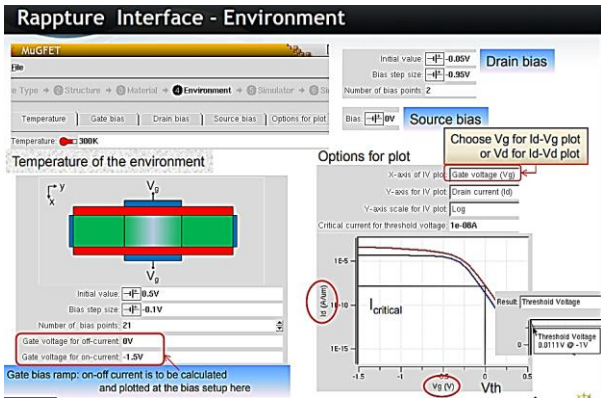

Figure 6. Voltage gate and temperature options

3.2.2. Selection of channel dimensions

This section explains the selection of channel dimensions and the effect of each dimension (length, width, and oxide thickness) on transistor performance. The calculation of the effect of dimensions on the combined channel characteristics through scaling factor *K* is also explained. The first simulation scenario was conducted based on channel length (i.e., 5, 10, 20, and 40 nm) as shown in Figure 7. The width and oxide thickness of the channel were kept constant (i.e., W=5 nm; T_{OX}=2.5 nm). At the end of the simulation, electrical

properties were extracted for each length, and the properties were drawn with variable lengths at certain points. The I_{ON}/ I_{OFF} ratio was calculated at V_{DD}=5, 0.5 V, the SS at V_{DD}=0.25 V, V_T at V_{DD}=0.5 V, and DIBL at V_{DD}=0.75 V. For the second simulation scenario, channel width was changed through 5, 10, 15 to 20 nm as shown in Figure 8. The length and oxide thickness were kept constant at L=40 nm and T_{OX}=2.5 nm. The electrical properties were drawn in relation to width change. In the third scenario, oxide thickness was changed to 1.5, 2.5, 5 and 7 nm at fixed length and width. Then, the data on properties were drawn with the change in oxide thickness.

Table 2. Simulation parameters

Parameters	Value
Channel length (L)	(5, 10, 20, 40) nm
Channel width (W)	(5, 10, 15, 20) nm
Channel oxide thickness (T_{OX})	(1.5, 2.5, 5, 7) nm
Scaling factor (K)	(1.0, 0.5, 0.25, 0.125)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}
Gate voltage	0.5–5 V
Temperature	300 K

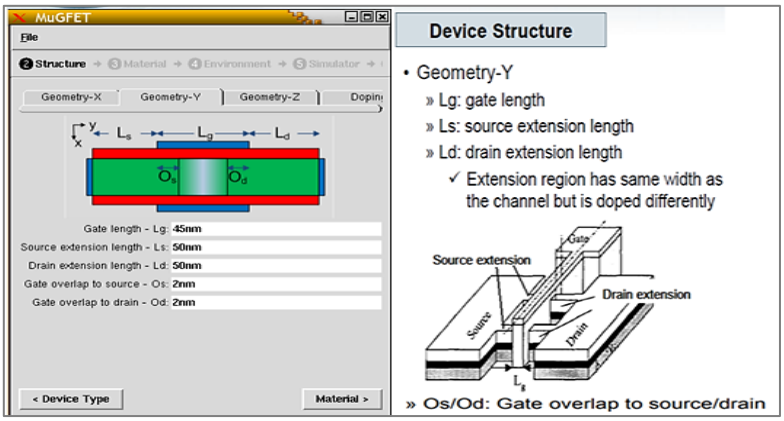

Figure 7. Channel length selection

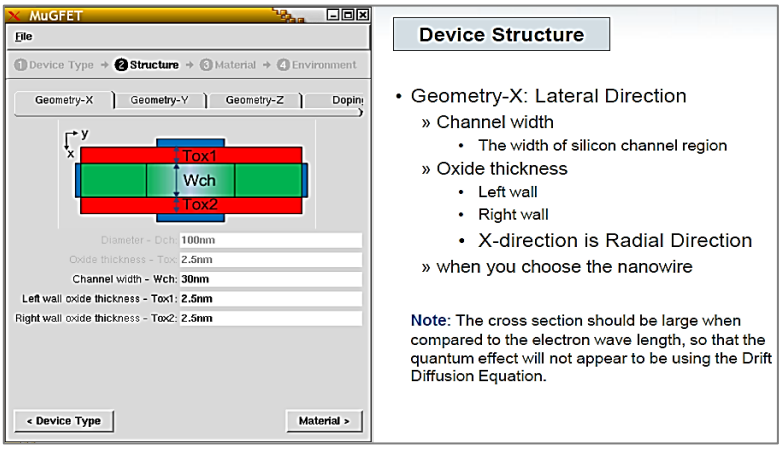

Figure 8. Channel width and oxide thickness selection

3.2.3. Scaling factor

To scale down all channel dimensions at once, the scaling factor K was proposed. Scaling down of channel dimensions and its effect on the characteristics of all FinFETs were simulated at the same voltage

range in all simulation scenarios. The length, width, and thickness will be scaled down by a factor (K). K=0.125 represents the minimal value of the dimension, whereas K=1 represents the original dimensions as summarized according to Table 3. Electrical characteristics were then extracted, and the extent of the scaling ratio was determined. This process was repeated in the selection of other semiconductors (i.e., Ge, GaAs, and InAs).

Table 3. Parameters used with the condition scaling factor K

K	L (nm)	W (nm)	T_{OX} (nm)
1.00	40	20	6
0.50	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.625

3.2.4. I–V characteristics

The electrical characteristics were extracted from the "simulate" option. The impact of changing channel dimensions on the performance of each type of FinFETs was evaluated based on FOUR (4) electrical characteristics namely, i) I_{ON}/I_{OFF} ratio ii) subthreshold swing (SS), iii) threshold voltage (V_T), and iv) drain-induced barrier lowering (DIBL). The desired properties were drawn, and the values were extrapolated as illustrated in Figure 9 and Figure 10.

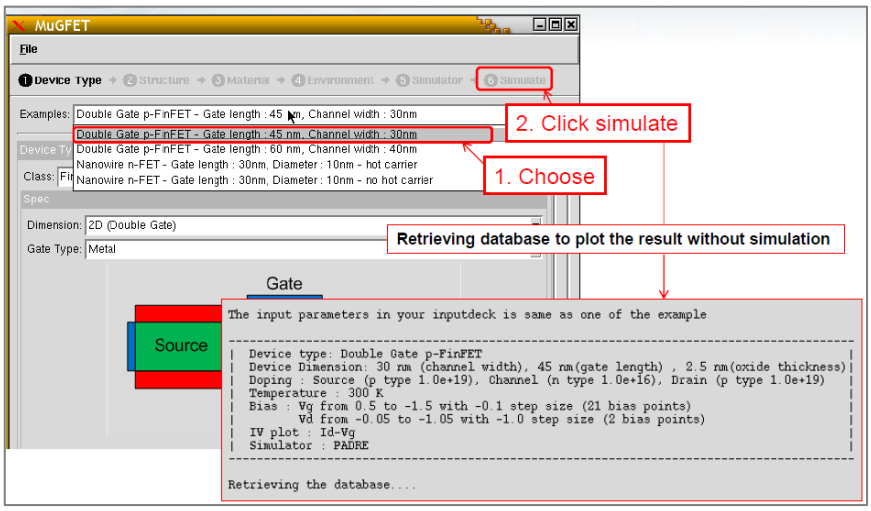

Figure 9. Electrical characteristics

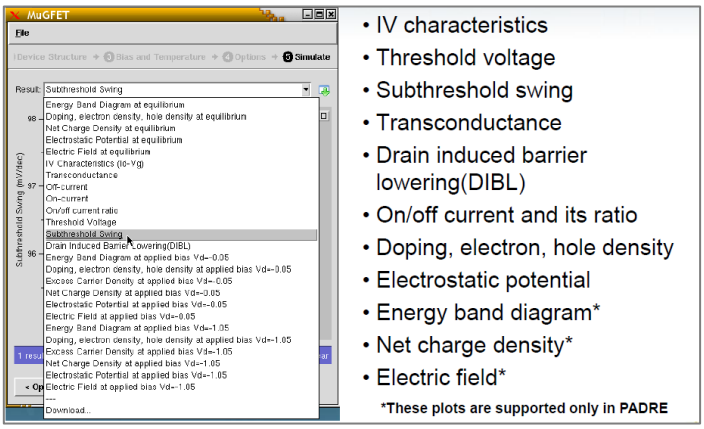

Figure 10. Electrical characteristic type selection

4. SIMULATION RESULTS

This section introduces the simulation results and electrical characteristics of Si, Ge, GaAs, and InAs FinFETs according to various channel dimensions. The output characteristic curves of the transistors under different conditions and parameters were considered. The effects of variable channel dimensions, such as channel length, width, and oxide thickness, in addition to the scaling factor of Si, Ge, GaAs, and InAs FinFETs, were determined on the basis of I–V characteristics derived from the conducted simulations. In this study, the Id–Vg characteristics of Si, Ge, GaAs, and InAs FinFETs at 300 K were simulated and evaluated with the simulation parameters. SS-ideal represents the minimum SS that can be found with a yield of 59.5 mV/dec at room temperature.

Fin field effect transistor (FinFET) shows great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies. The structure of FinFET provides superior electrical control over the channel conduction; thus it has attracted widespread interest from researchers in both academia and industry. However, aggressively scaling down of channel dimensions, mainly the channel length will degrade the overall performance due to detrimental short channel effects (SCEs). In this study, four simulation experiments were designed to evaluate the performance of each transistor in terms of the considered metrics. In the first scenario, channel length was changed, whereas other dimensions (W and T_{OX}) were kept constant. In the second scenario, the effect of changing the channel width was investigated, whereas both the length and thickness of the channel were kept constant. In the third scenario, oxide thickness was changed, whereas length and width were fixed. In the last scenario (which is reported in this paper), the influence of changing the scaling factor was studied by changing the three dimensions all at once and on the basis of a new changeable scaling factor K. For brevity, the obtained results from the first three scenarios (length, width, and oxide thickness) for each semiconductor material are summarized and compared in Table 4, which also highlights the highest value of I_{ON}/I_{OFF} and the SS nearest to the ideal value. Results of the last scenario (which were acquired according to the scaling factor, K) were emphasized through a distinctive color in Table 4. The best dimensions for all semiconductor FinFET channel types (Si-FinFET, Ge-FinFET, InAs-FinFET, and GaAs-FinFET) were obtained at the highest length (L=40 nm) in the first scenario, the lowest width (W=5 nm) in the second scenario, and the smallest T_{OX} (T_{OX}=1.5 nm) in the third scenario.

According to the conducted simulations, the best performance in terms of the considered electrical characteristics was achieved at channel length L=40 nm, channel width, W=5 nm, and channel oxide thickness, T_{OX}=1.5 nm. Thus, Si-FinFET could not achieve a proper performance with a shrinking channel length where it attains better performance at the longest channel case. Similarly, The scaling down of channel dimensions and its effect on the characteristics of GaAs-FinFET was simulated for the same voltage range in all simulations. The best performance in terms of the considered electrical characteristics was achieved at channel length L=30-40 nm, channel width, W=5 nm, and channel oxide thickness, T_{OX}=1.5-2.5 nm. For Ge-FinFET, the best performance in terms of the considered electrical characteristics was achieved at channel length L=40 nm, channel width, W=5 nm, and channel oxide thickness, T_{OX}=1.5 nm. Thus, Ge-FinFET has not achieved a proper performance with a shrinking channel length where it attains better performance at the longest channel case. In order to scale down all channel dimensions at once, we have applied a scaling factor, K, on all dimensions including, length, width, and thickness. Based on the obtained results from the comprehensive characterization of InAs-FinFET depending on various channel dimensions, the best performance can be achieved with a channel length L=25 nm, channel width, W=5 nm, and channel oxide thickness, T_{OX}=1.5-2.5 nm. In order to scale down all channel dimensions at once, a scaling factor K was applied to all dimensions including, length, width, and thickness. Thereafter the electrical characteristics were investigated based on the scaling factor. The reference value of 'K' is defined as "1" with its highest channel dimensions. Then, all dimensions are scaled down to new physical limits for the channel of Si-FinFET, GaAs-FinFET, Ge-FinFET, and InAs-FinFET.

This paper presents an overall comparison of the different FinFETs based on the type of semiconductor materials and according to obtained results from the fourth scenario of each type. All the considered FinFETs performed poorly with the shrinking channel length; that is, each only attained better performance at the longest channel. To simultaneously scale down all channel dimensions, scaling factor K was applied to all dimensions, including length, width, and thickness. In particular, this scenario was designed for simultaneous consideration of all dimensions (L, W, and T_{OX}) by changing the scaling factor K to decrease all dimensions and was used to evaluate transistor performance for each value of K. Thereafter, the electrical characteristics were investigated according to the scaling factor. The reference value of K was defined as "1" with its highest channel dimensions. Then, all dimensions were scaled down to the new physical limits for the Si-FinFET channel. Table 3 lists all dimensions corresponding to the defined scaling factors. The electrical characteristics (I_{ON}/I_{OFF}, SS, V_T, and DIBL) of FinFET transistors (Si, Ge, GaAs, and InAs) were compared.

Given their importance as key metrics of transistor performance, I_{ON}/I_{OFF} and SS were emphasized in our evaluation for identifying the best performance based on semiconductor materials.

Table 4. Comparison of semiconductors channel types of FinFET

Semiconductor	**Si**	**GaAs**	**Ge**	**InAs**
I_{ON}/I_{OFF}	2.12×10^{8}	1.08×10^{8}	2.29×10^{5}	6.97×10^{6}
SS(mv/dec)	60	59.65	65	101
Best L(nm)	**40**	**30-40**	**40**	**25**
I_{ON}/I_{OFF}	2.12×10^{8}	1.08×10^{8}	2.29×10^{5}	5.58×10^{7}
SS(mv/dec)	60	60	62	124
Best W(nm)	**5**	**5**	**5**	**5**
I_{ON}/I_{OFF}	2.15×10^{7}	2.11×10^{8}	3.53×10^{4}	2.54×10^{6}
SS(mv/dec)	62	59.7	67	155
Best T_{ox} (nm)	**1.5**	**1.5-2.5**	**1.5**	**1.5-2.5**
I_{ON}/I_{OFF}	2.15×10^{7}	3.65×10^{6}	3.56×10^{4}	7.94×10^{4}
SS(mv/dec)	62.2	65.7	68.9	94
Best K	**0.125**	**0.125**	**0.125**	**0.125**

Si-FinFET achieved the highest I_{ON}/I_{OFF} ratio in all cases compared with other materials regardless of the scaling factor value (Figures 11 and 12). Although Si-FinFET obtained the highest I_{ON}/I_{OFF} at K=0.5, its SS at K=0.5 is far from the ideal value. With the increment in K-value, the SS increased significantly and led to decreased transistor speed. Therefore, the best performance of Si-FinFET, by considering both SS and I_{ON}/I_{OFF}, was achieved at K=0.125, similar to the other types. The Si-FinFET maintained more than 10^8 I_{ON}/I_{OFF} ratio and 62.2 mv/dec SS relative to the nearest competitor, which is GaAs-FinFET, which attained more than 10^6 I_{ON}/I_{OFF} ratio and 65.7 mv/dec SS at the same scaling factor of 0.125. GaAs-FinFET performed poorly in terms of the considered metrics at other scaling factor values. A notable improvement occurred in I_{ON}/I_{OFF} ratio with the simultaneous downscaling of all channel dimensions. Consistent results were obtained for both Ge- and InAs-FinFETs, where the best values of I_{ON}/I_{OFF} ratios were higher than 10^4 and achieved at a scaling factor of K=0.125; the poorest I_{ON}/I_{OFF} ratios were less than 10^2, which occurred at the reference scaling factor for both V_{DD} voltages. In terms of SS, which respectively reached 195 and 189 mv/dec at K=1, both InAs- and GaAs-FinFETs recorded the poorest results in all scenarios regardless of channel dimensions due to their high permittivity values relative to other semiconductors. Overall, SS proportionally increased with K regardless of the semiconductor material.

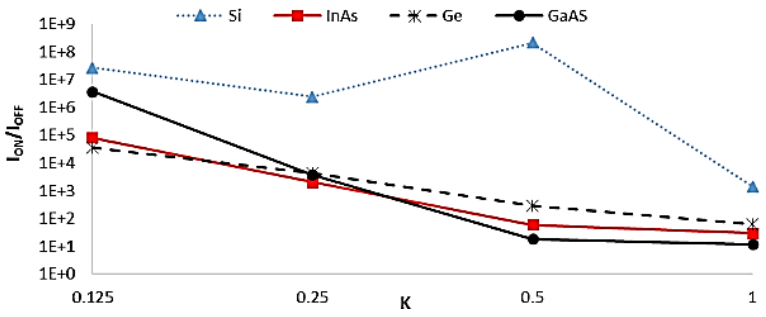

Figure 11. I_{ON}/I_{OFF} ratio vs. the scaling factor for various FinFET semiconductors

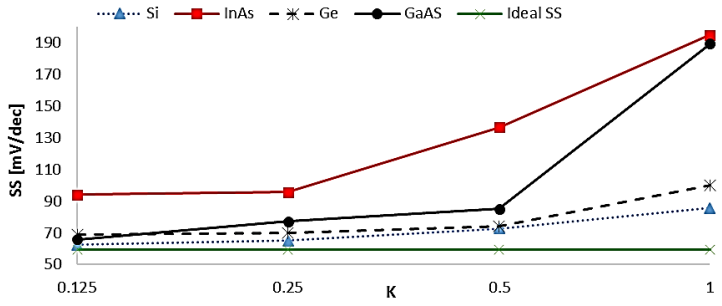

Figure 12. SS vs. the scaling factor for various FinFET semiconductors

Figures 13 and 14 illustrate the influence of the changing scaling factor (K) on V_T and DIBL, respectively. Oxide thickness is a key player in changing the value of V_T, whereas other dimensions presented marginal effects on this metric. Therefore, the variation of V_T with changing scaling factor is limited for all transistors except for InAs-FinFET, which attained the highest V_T in all cases. InAs-FinFET achieved the highest value of V_T=1.28 V at K=1 compared with the lowest value of V_T=0.7 V at K=0.25. Si-FinFET followed and outperformed others in all cases except at K=0.125 where V_T=0.49 V was the lowest among all semiconductors. Similarly, InAs-FinFET achieved the highest DIBL results in all cases compared with other semiconductor materials. For Si-FinFET, the DIBL value ranged from 45 to 50 mV/V until it reached 49.99 mV/V at K=0.125. This outcome indicated that charge exchange was almost stable at the different dimensions of the Si channel. For GaAs-FinFET, DIBL decreased from 298 mV/V at K=1 to 48 mV/V at K 0.125, at which a similar performance of Si-FinFET was observed. The obtained results in terms of V_T and DIBL cannot provide a good indication for comparing the considered semiconductor materials as they are based on multiple parameters related to the nature of Fin-FETs rather than channel dimensions. Therefore, our conclusion for these simulation results was drawn mainly on the basis of the first two electrical metrics, I_{ON}/I_{OFF} and SS value.

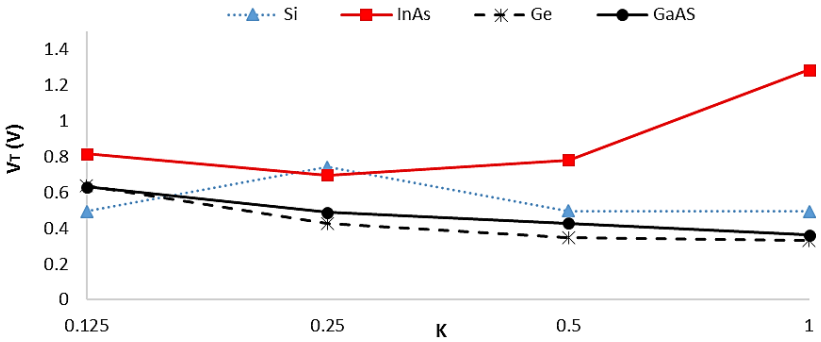

Figure 13. VT vs. K for various FinFET semiconductors

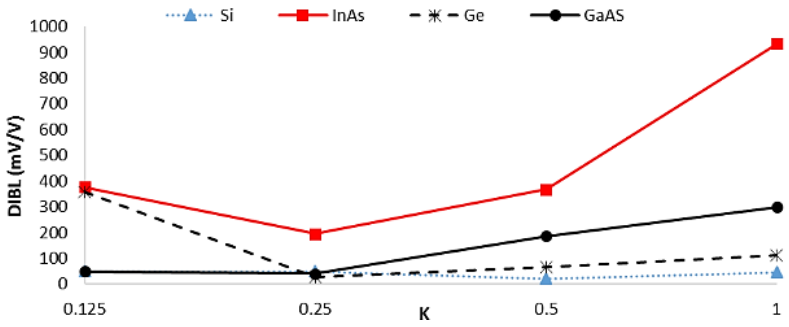

Figure 14. DIBL vs. K for various FinFET semiconductors

5. CONCLUSIONS AND FUTURE WORK

This paper investigated and evaluated the influence of changing each channel dimension on the electrical characteristics of each semiconductor material. Optimal dimensions were selected depending on the highest I_{ON}/I_{OFF} ratio and the SS nearest to the ideal value. The performance of FinFETs improved with the increasing channel length, decreasing width, and decreasing oxide thickness. These outcomes were due to the SCEs on I_{ON}/I_{OFF} and SS. Si-Fin-FET outperformed other semiconductors in the considered single-dimension-based scenarios. To achieve new downscaling limits, a scaling factor, K, was proposed to shrink down all channel dimensions at the same time. Three steps were considered to decrease the channel length along with width and oxide thickness to 25% of their default values. The obtained results introduced new limits with good performance in terms of the investigated characteristics. The default values at K=1 were set to L=40 nm, W=20 nm, and T_{OX}=6 nm. These dimensions were downscaled to L=5 nm, W=2.5 nm, and T_{OX}=0.625 nm when the proposed K was set to 0.125. According to the new scaling factor, the new nano-dimensional channel was designed for four types of semiconductor material-based FinFETs (Si, Ge, GaAs, and InAs). The performances of different FinFETs were evaluated and compared. The highest I_{ON}/I_{OFF} ratio (more than 10^8) and the SS

nearest to the ideal value (62.2 mv/dec) were obtained with Si-FinFET with the new limits of channel dimensions. GaAs-FinFET came second with I_{ON}/I_{OFF} of more than 10^6 and SS=65.7 mv/dec. InAs-FinFET presented the poorest performance in terms of SS (94 mv/dec), and Ge-FinFET attained the lowest I_{ON} /I_{OFF} compared with the other types. The outcomes of this research contribute toward new channel nano-scaling limits of FinFETs as potential successors to planar transistors in nanoscale devices and nanotechnology applications and for further analysis of the electrical characteristics of FinFETs by reducing leakage current and overcoming SCEs. This paper has focused on the effects of scaling down the channel dimensions of FinFET transistors relative to their electrical characteristics. Four semiconductor material-based FinFETs were considered. However, issues regarding the aspect of FinFETs as successors to nanoscale and planner devices require further investigation. The following recommendations show how this work can be expanded in various research directions: i) A comparative study between FinFET and silicon nanowire transistor (SiNWT) as suggested successors to MOSFET at the achieved nano-dimension limits; ii) Investigation of the temperature characteristics of various semiconductor material-based FinFETs with different insulating materials; iii) Application of the suggested model with optimal channel dimensions of FinFET inverters; and iv) Conducting experimental research to investigate the capability to achieve such nanoscale channel dimensions in real transistors and compare the performance criteria of different FinFETs in both simulation and experimental studies.

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