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Performance improvement of fractional N-PLL synthesizers for digital communication applications

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ABSTRACT

Loop filter with two order was designed to improve the performance of the fractional N-phase locked loop (PLL) circuit (reference spurs noise and switching time), decreasing these two factors give good characteristic to fractional N-PLL circuit, the second order and third order loop filters are widely used in frequency synthesizer because they give good stability tolerance and for their simple architecture. They are designed at bandwidth B=125 KHz and its multipoles, at two values of the phase margin (pm)= 35°, 57°. MATLAB program was used to find the lock time, the component values for each element in the loop filter, also the filter impedance T(s), the bode plot of frequency response for close loop (CL) and open loop gain (OL). It is found by comparing the result of the frequency response for the 2nd order loop filter and 3rd order loop filter, that increasing the order of the filter will reduce the spurs noise that destroy the received signal at receiving side.

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1. INTRODUCTION

The frequency synthesizer circuit is used in the field of communications such as mobile phones, satellites and radio devices, the purpose of its use is to generate a specific range of frequencies for any application for the purpose of switching between the frequencies of different channels. Fractional-N synthesizer is a kind of indirect analogue synthesizer that mixes high accuracy and quickness. At very high reference frequency, the frequency space between channels can be reduced [1], [2]. These synthesizers can synthesize rational multiples of the reference frequency, allowing for a high reference frequency for a given frequency resolution, ensuring that the loop bandwidth can be extended without endangering the loop. due to the spectral purity that the frequency synthesizer gives, it gets a significant improvement in reducing spurs noise as well as phase noise and reducing the lock-time. The main reason of using frequency synthesizer is to produce accurate and coordinated frequencies with fast switching between channels at a minimum of phase noise. To satisfy device requirements the conflict between high resolution and rapid switching necessitates can be solved by using two separate integer synthesizers [3]-[9]. Figure 1 shows the main component of the fractional-N phase locked loop (PLL) frequency synthesizer.

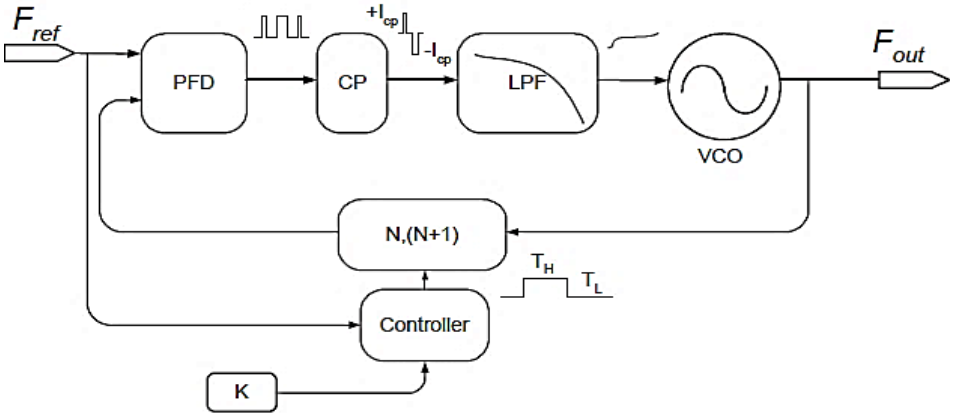

Figure 1. Fractional-N PLL frequency synthesizer component [10]

2. RESEARCH METHOD

There are several characteristics that distinguish the performance of frequency synthesizer from each other, as there are several standards and conditions set by modern wireless communication systems when designing, and one of the most important characteristics that distinguish the performance of frequency synthesizer is the frequency spacing between channels where the application used in the synthesizer determines the value of the frequency distance between channels, for Bluetooth application system, the frequency spacing between the channels is equal to 1 MHz, and distinguishes the efficiency of the frequency synthesizer is the lock-time, phase noise and spurs noise. In this paper, the lock-time and spurs noise of the frequency synthesizer used in the implementation of the Bluetooth system have been improved, as the permissible values of the lock-time are less than 220 µsec and the permissible value for the spurs noise is less than or equal to -49 dB [11]-[15].

Settling time: is defined as the time it takes for the oscillator output signal to achieve a steady state during the transition from one channel to the next. The settling time is proportional to the loop filter's bandwidth, which should be ten times less than the reference frequency to keep the loop stable. The faster the settling process, the wider the loop bandwidth [16]-[19]. Therefor to achieve a faster transient settling time, a PLL-based frequency synthesizer needs a high reference frequency. The settling time for a frequency synthesizer is calculated using the following equation [20]:

$$\text{settling time} = \frac{-\ln\frac{tol*\sqrt{1-\delta^2}}{f2-f1}}{\delta*wn} \quad (1)$$

where:

$f2 - f1$: Representing the channel spacing and equal to 1MHz for bluetooth application

tol: Representing the tolerance and it is equel to 1kHz.

$$\text{wn: Is the ringing frequency of the output signal to reach steady state} = \sqrt{\frac{K_{\emptyset}*K_{vco}}{N*A_o}} \quad (2)$$

$$\delta\text{: Denoted to the damping factor} = \frac{T2*wn}{2} \quad (3)$$

Spurs noise: is an undesirable and non-harmonically based signal that appears at the voltage control oscillator's output spectrum. Figure 2 shows the effecting of the spurs noise on the received signal, spurs noise is classified into two categories: fractional spurs noise and reference spurs noise. In a fractional phase locked loop that uses a fractional divider with a fractional value, fractional spurs noise occurs. Although reference spurs noise persists when offsets have the same frequency as the input signal, the discrepancy between two charge pump currents is the primary cause of reference spurs noise [21]-[24].

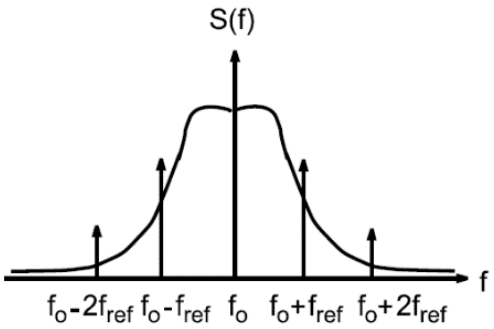

Figure 2. Effecting of the spurs noise on the received signal [25]

3. LOOP FILTER DESIGN

The passive loop filter works in compatible with the charge pump, where the current outgoing of the charge pump is a pulse width modulated current and this current is the input signal of the loop filter, so the filter is called a current divider loop filter. The passive loop filter converts current pulses from a PFD into stable voltage by using a simple combination of resistors and capacitors that consist the filter circuit. Passive loop filters are commonly used in integrated PLLs and frequency synthesizers due to their basic topology, small area profession, and low power dissipation. So, for their high stability tolerance and simplified design second and third order loop filters are widely used in frequency synthesizers. Beyond the loop's cut-off frequency, higher order designs will provide improved noise suppression. It is possible to effectively suppress phase noise at high offset frequencies, which is particularly important in a large bandwidth application. The third order topology is used in this work in the real frequency synthesizer design. In order to reap the benefits of adequate noise reduction without risking stability. The design of second order loop filter is shown in Figure 3 (a). Its consist of one resistance (R1) and two capacitances (C1, C2). When phase margin and width of the filter passband are specified and by applying the equation in Table 1, the filter parameter (R1, C1 and C2) can be calculated. A third pole can be added to the filter response by adding resistor R2 and capacitor C3, as shown in Figure 3 (b). This method can be used to optimize the output of a second order loop filter or to build a third order loop filter by designing an additional component. The benefit of a third order loop filter over a second order loop with auxiliary filtering is that the response rolls-off more quickly beyond the loop natural frequency, allowing for loop noise portion rejection. This indicates that the reference noise side bands are narrower for a given loop natural frequency. The basic equations that will be utilized to determine the essential design variables for the 2nd and 3rd order filters at the fractional N-PLL synthesize will be utilized in Table 1.

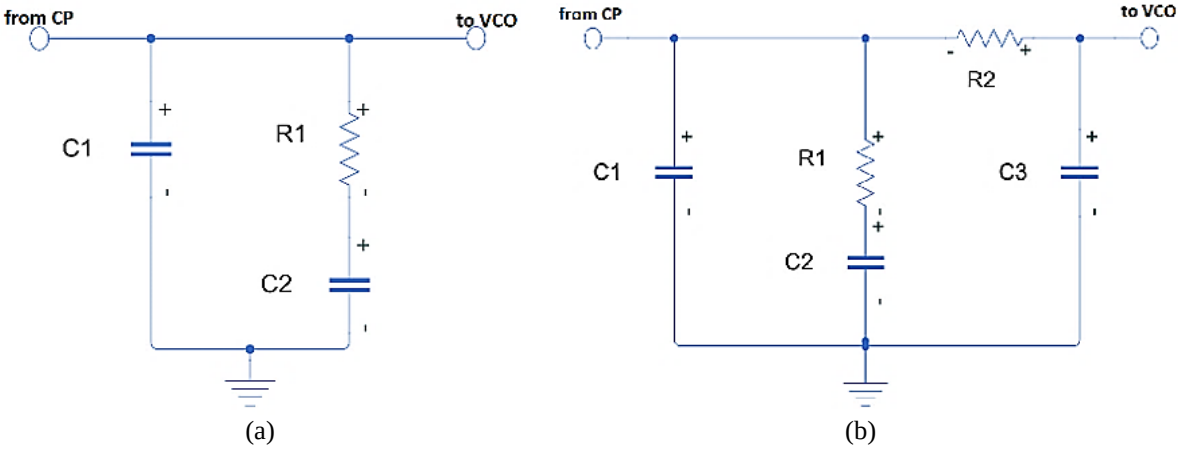

Figure 3. Loop filter design for 2nd and 3rd order: (a) second order loop filter and (b) third order loop filter

Table 1. The 2nd and 3rd order loop filter basic equations [25]

Abbreviations	Definition	Equation of 2nd order loop filter	Equation of 3rd order loop filter
T(s)	The loop filter's transfer function	$\frac{1+S\,T2}{S\,A0(1+S\,T1)}$	$\frac{1+S\,T2}{S(S^2A2+S\,A1+A0)}$
N	Division ratio	F_{out}/F_{ref}	F_{out}/F_{ref}
T1	The first pole in the loop filter transfer function	$\frac{\sqrt{(1+\gamma)^2\tan^2\emptyset+4\gamma}-(1+\gamma)\tan\emptyset}{2\,fc}$	$\frac{\sec(\emptyset)-\tan(\emptyset)}{fc(1+T31)}$
T2	The zero in the loop filter transfer function	$\frac{\gamma}{T1\,fc^2}$	$\frac{\gamma}{fc^2(T1+T3)}$
A0	The loop filter coefficient	$\frac{K_\emptyset K_{vco}}{N\,wc^2}*\sqrt{\frac{(1+T2^2fc^2)}{(1+T1^2\,fc^2)}}$	$\frac{K_\emptyset K_{vco}}{N\,wc^2}*\sqrt{\frac{(1+T2^2\,fc^2)}{(1+T1^2\,fc^2)(1+T3^2fc^2)}}$
C1	The first capacitor in the loop filter	$A0\frac{T1}{T2}$	$\frac{A2}{T2^2}(1+\sqrt{1+(T2\,A0-A1)\frac{T2}{A2}})$
C2	The second capacitor in the loop filter	A0-C1	A0-C1-C3
R1	The first resistor in the loop filter	$\frac{T2}{C2}$	$\frac{T2}{C2}$
O(s)	The open loop gain of the loop filter	$\frac{T(s)K_\emptyset K_{vco}}{S\,N}$	$\frac{T(s)K_\emptyset K_{vco}}{S\,N}$
G(s)	The close loop gain of the loop filter	$\frac{O(s)}{1+O(s)}$	$\frac{O(s)}{1+O(s)}$
R2	Resistor 2 of the 3rd order loop filter	NON	$\frac{A2}{T2C1C3}$
C3	Capacitor 3 of the 3rd order loop filter	NON	$\frac{-T2^2\,C1^2+T2\,A1\,C1-A2\,A0}{T2^2C1-A2}$
T3	The second pole in the 3rd order loop filter transfer function	NON	T1 T31
A1	The loop filter coefficient	NON	A0(T1+T3)
A2	The loop filter coefficient	NON	A0 T1T3

The symbols in the equations are defined as the following:

γ: The Improvement Factor.
T31: The Ratio of the second pole to the first pole
Ø: The Phase Margin (pm), in degree unity.
$k_ø$: The charges pump current, in μA unity.
F_{ref}: The Input signal frequency.
F_{out}: The Output Frequency.
fc: The carrier frequency.
k_{vco} : The voltage-controlled oscillator's gain.
Where $k_ø . F_{ref}. F_{out}. fc. k_{vco}$ is in Hertz unit.

4. SIMULATIONS RESULTS

The simulation results of the fractional N-PLL circuit frequency response at the two-order state loop filter (2nd, 3rd) are shows in the following steps:

- The second-order loop filter is designed, and with utilizing Table 1 the loop filter components will find as C1=70 pF, C2=0.19 nF, and R1=12.8KΩ, these values was calculated accoding the following variables pm=35°, K_ϕ=50 μA, K_vco=210 MHz, f_ref = 19.2 MHz, and B=125 kHz.When the bandwidth (B) is multiples by the facter x=1,2,4 the close loop transfer function for a fractional N-PLL frequency synthesizers will shows as in the Figure 4.

It will be noted from the Table 2 that multipules the bandwidth of the filter dosen't improving the amplitude frequency response gain, also it noted that the values of the response gain will becomes unwanted values at high frequencies, and it's one of the characteristics of low-pass filters, furthermore when the slope gain is greater than the bandwidth frequency the frequency response is faster to go down. Therefore, it should choosing low bandwidth values to improve the filter's noise performance, especially at higher frequencies.

Table 2. The close loop transfer function magnitude response comparition for the 2nd order loop filter at pm=35° and B=(125, 250, 500-kHz)

Frequency (MHz)	CL Transfer function magnitude (dB)		
	B =125kHz	B =250kHz	B =500kHz
1	-30.4	-18.3	-5.95
10	-70.5	-58.4	-46.4
100	-110	-98.4	-86.4

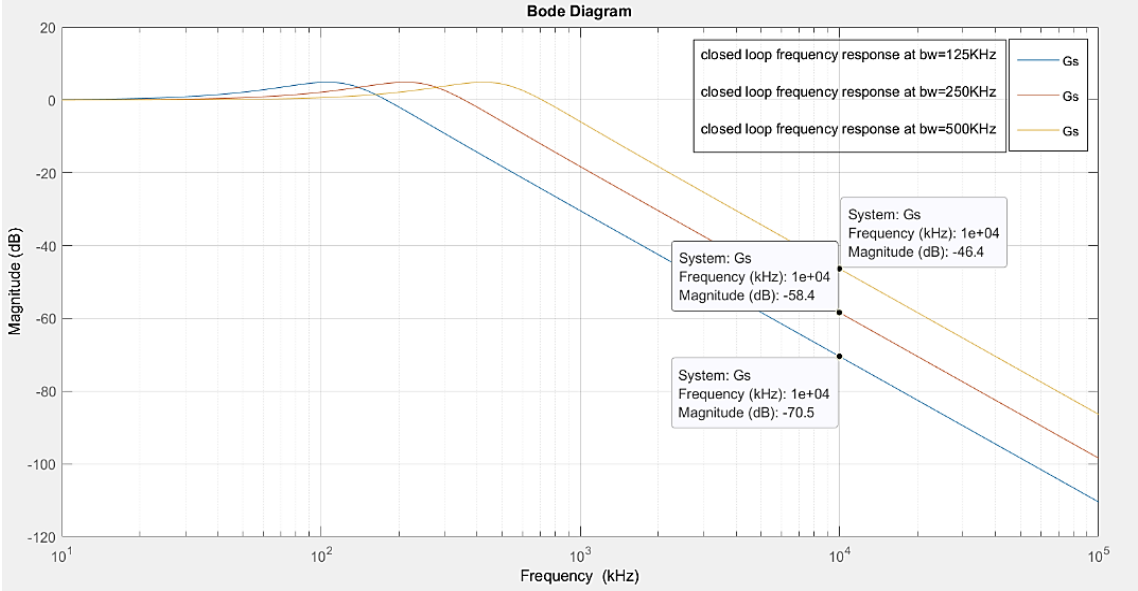

Figure 4. The close loop transfer function response (CL) for the 2nd order loop filter at pm=35° and B=(125, 250, 500-kHz)

– The second-order loop filter is designed, and with utilizing Table 1 the loop filter components will find as C1=40 pF, C2=0.14 nF, and R1=10.25 KΩ, these values was calculated accoding the following variables pm=57°, K_ϕ=50 µA, K_vco=210 MHz, f_ref=19.2 MHz, and B=125 kHz. When the bandwidth (B) is multiples by the facter x=1,2,4 the close loop transfer function for a fractional N-PLL frequency synthesizers will shows as in the Figure 5.

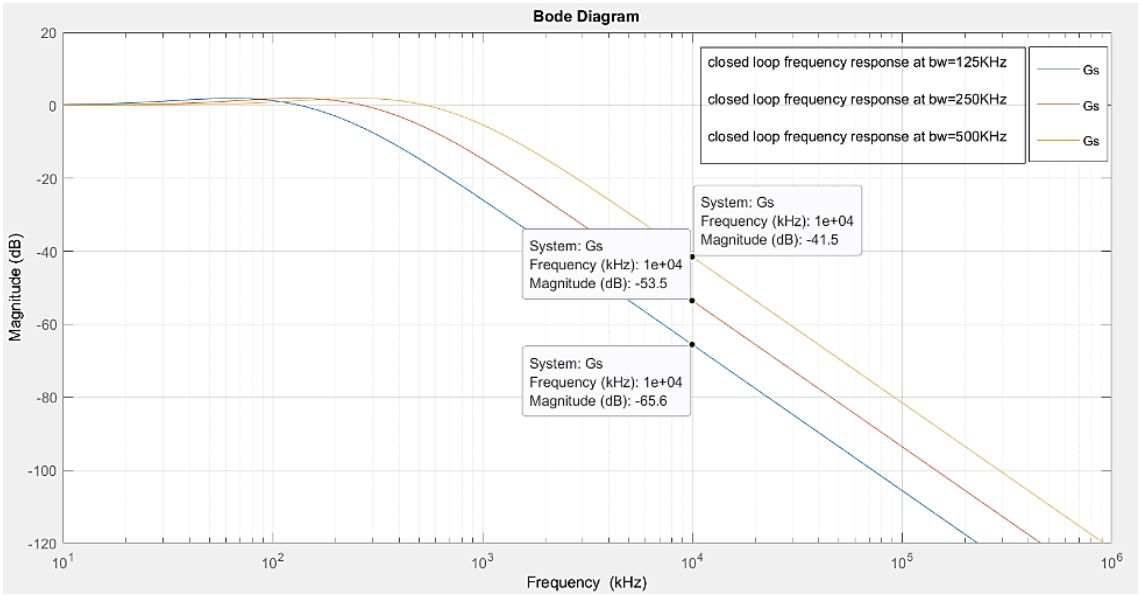

Figure 5. The close loop transfer function response (CL) for the 2nd order loop filter at pm=57° and B=(125, 250, 500-kHz)

As seen in Table 3 at small values of the Banwidth the spurs noise is eliminated more effectively, because the slope gain is faster to go downand the frequency response is quickly reduced due to the 2nd order

filter. Furthermore, raising the phase margin values will not enhance the frequency response gain at high frequencies.

Table 3. The close loop transfer function magnitude response comparition for the 2nd order loop filter at pm=57° and B=(125, 250, 500-kHz)

Frequency (MHz)	CL Transfer function magnitude (dB)		
	B=125Hz	B=250kHz	B=500kHz
1	-25.9	-14.7	-5.32
10	-65.6	-53.5	-41.5
100	-106	-93.5	-81.5

– The third-order loop filter is designed, and with utilizing Table 1 the loop filter components will find as C1=34.7 pF, C2=0.23 nF, C3=4.88 pF, R1=10.4 K, and R2=64.6 K, these values was calculated accoding the following variables pm=35°, K_ϕ=50 µA, K_vco=210 MHz, f_ref=19.2 MHz, and B=125 kHz.When the bandwidth (B) is multiples by the facter x=1,2,4 the close loop transfer function for a fractional N-PLL frequency synthesizers will shows as in the Figure 6.

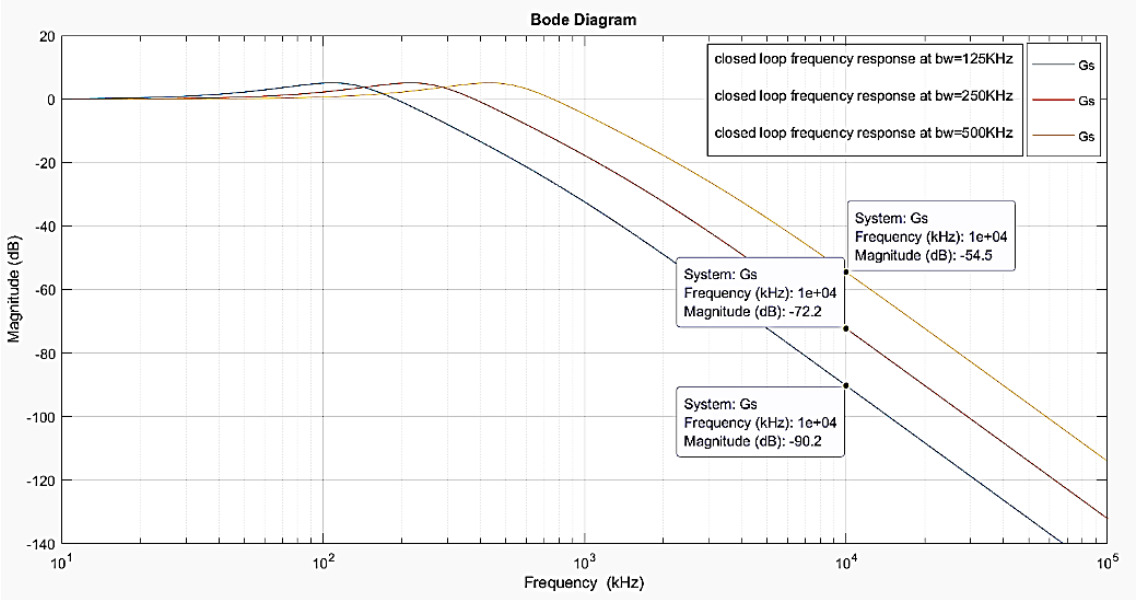

Figure 6. The close loop transfer function response (CL) for the 3nd order loop filter at pm=35° and B=(125, 250, 500-kHz)

Table 4 shows that as the order of the filter is increased, the response gain increases. It must be observed that the slope of the gain frequency response in the third order filter is faster to go down than in the second order filter. At higher frequencies, the amplitude of the frequency response is better, resulting in less spurs noise.

Table 4. The close loop transfer function magnitude response comparition for the 3nd order loop filter at pm=35° and B=(125, 250, 500-kHz)

Frequency (MHz)	CL Transfer function magnitude (dB)		
	B=125kHz	B=250kHz	B=500kHz
1	-32.4	-17.7	-4.74
10	-90.2	-72.2	-54.5
100	-150	-132	-114

– For a fractional N-PLL the settling time calculated using (1) in the (second order and third order) designed loop filter, and the results were shown in the tables.

It is noted from the Tables 5 and 6 that the value of the lock time of the second order loop filter is close to the value of the lock time of the third order loop filter (that is, the increase in the filter order does not affect on the value of the lock time), where the lock time is affected by changing the phase margin and the bandwidth, so by increasing the phase margin the locking time will increase, but the increasing of bandwidth will decrease the lock time.

Table 5. Lock time for 2nd loop filter in µsec.

B.W (kHz)	pm (degree)					
	30	35	47	57	61	62
125	18.3	18.4	18.8	19.95	21.9	N.D
250	9.15	9.21	9.43	9.97	10.9	N.D
500	4.57	4.6	4.71	4.98	5.48	N.D

Table 6. Lock time for 3rd loop filter in µsec.

B.W (kHz)	pm (degree)						
	30	35	47	57	61	62	63
125	19.32	19.35	19.38	20.2	21.7	23.7	N.D
250	9.6	9.63	9.69	10.1	10.8	11.8	N.D
500	4.8	4.82	4.84	5.05	5.44	5.92	N.D

5. CONCLUSION

In the proposed fractional-N types PLL, it is found that reducing the bandwidth will reduce the level of the spurs noise, but the settling time will increase and the values of the capacitors of the filter will be unrealistically large, thus causing additional noise in the output of the synthesizer circuit due to parasitic capacitors, therefore large values of the frequency bandwidth are taken and thus the values of the capacitors will be acceptable and will not affect the circuit. The settling time will also improve, but the level of spurs noise will increase with the increase in the bandwidth. Therefore, a higher-order filter is used as it works to reduce the spurs noise. The precision in selecting the values of (bandwidth, phase margin and filter order) is taken into consideration when designing the filter, depending on the application in which the synthesizer circuit to be used.

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