TELKOMNIKA Telecommunication Computing Electronics and Control
Vol. 21, No. 4, August 2023, pp. 872~880
ISSN: 1693-6930, DOI: 10.12928/TELKOMNIKA.v21i4.22341

Design and performance analysis of low phase noise LC-voltage controlled oscillator

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Article Info

Article history:

Received Nov 30, 2021
Revised Aug 08, 2022
Accepted Oct 26, 2022

Keywords:

Figure of merit
Low phase noise
MOS varactor
Tuning range
Voltage controlled oscillator

ABSTRACT

Voltage controlled oscillator (VCO) offers the radio frequency (RF) system designer a freedom to select the required frequency. Today's wireless communication system imposes a very stringent requirement in terms of phase noise generated in VCO. This study presents an inductive source degeneration technique to improve the phase noise performance of the inductance-capacitance (LC)-VCO. Double cross-coupled topology has been chosen for the proposed VCO. The post layout simulations with the parasitic resistance, inductance, capacitance (RLC) extracted view is carried out with united microelectronics corporations (UMC) 0.18 µm process by spectre simulator of cadence tools. The proposed VCO provides a phase noise of -124.3 dBc/Hz @ 1 MHz. The tuning range obtained is 19.87% with a centre frequency of 2.46 GHz which makes it suitable for industrial, scientific, and medical (ISM) band applications. It consumes a power of 2.10 mW. Also, a good figure of merit of -189 is achieved. The total layout area occupied is 477×545 μm^2.

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1. INTRODUCTION

The global voltage controlled oscillator (VCO) market is predicted to increase substantially due to rapid technological advancements in the very large scale integration (VLSI) sector and the wide application of voltage-controlled oscillation in numerous end-user industries. There is a need for wide tunable reference frequency in almost all wireless or wireline tasks, which supports multi-standard applications. Despite a large amount of research and development, radio frequency (RF) designers still find the VCO to be a difficult component. As the need for wireless communications grows, and new applications enter the market at higher frequencies, VCOs are subjected to more demanding standards. VCO may be realized with many configurations according to the applications and performance requirements. The available fundamental approaches are ring oscillator [1]-[3], inductance-capacitance (LC) oscillator [4], [5] tunable active inductor (TAI) based oscillator [6], [7], and relaxation oscillator [8]. Apart from the phase noise (PN); tuning range, power consumption, and output waveform are also necessary VCO specifications. Unfortunately, there are direct tradeoffs between these specifications like ring oscillator, or TAI-based VCOs have larger tuning range but lower phase noise while resonator-based oscillators have lower phase noise but suffer in terms of tuning range. The performance of VCO has a very significant impact on the overall performance of RF front end they are being used in [9]. In high-performance applications where low PN is required, VCO using LC tank is preferred. The minimum phase noise requirement in the VCO is set by the specific communication standard. Various low PN techniques like noise filtering [10]-[12], tail current shaping [13], [14], self-switched bias [15], [16] have been

reported in the literatures. In this paper, we present an inductive source degeneration (ISD) based low PN technique to improve the PN performance of the LC-VCO. The organization of the paper is as: section 2 discuss the methodology for implementing LC-VCO. Circuit architecture and detailed analysis of the proposed design are presented in section 3. Section 4 elaborate the layout, post layout simulation and performance comparison followed by conclusion.

2. METHODOLOGY FOR IMPLEMENTATION OF LC-VCO

VCO designers generally need a methodology to evaluate the performance parameters. It helps to optimize the various components of the circuit. Double cross-coupled (CC) topology is very much popular among the LC-VCO designers. It has been widely used by the many researchers [17]-[24]. The CC topology offers large amplitude, symmetrical waveform and higher transconductance. All these advantages make the double CC differential topology an optimal choice, and hence the same has been adopted in this work. The design of an optimized LC tank is of prime importance.

2.1. VCO core design

In order to get the low power consumption, large tuning range, and low PN performances. The LC resonator and active circuitry of VCO must be optimized. The design of inductor and varactor is challenging to achieve a low PN VCO. In this design, the size of N-channel metal-oxide semiconductor (NMOS) and P-channel metal-oxide semiconductor (PMOS) transistors, inductors, varactor value, and parasitics are critical physical parameters.

– Metal oxide semiconductor (MOS) transistor sizes

The size of transistors is one of the essential design parameters which impacts the various performance parameters; hence it may be considered for the optimization procedure. The large size of the transistor gives a better transconductance which helps to overcome parasitic losses offered by the LC tank and thus helps in start-up oscillations at the cost of tuning range. Hence the aspect ratio of the transistor is chosen to generate sufficient negative resistance. Also, as the symmetry has to be maintained for better PN, the sizing of NMOS and PMOS has been chosen keeping in mind the following relations.

$$I_{dsat} = \frac{\mu_n C_{OX}}{2} . \frac{W}{L} . (V_{GS} - V_{th})^2 \quad (1)$$

$$G_{mn} = \frac{dI_{dsat}}{dV_{GS}} = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{th}) \quad (2)$$

Similarly for PMOS:

$$G_{mp} = \mu_p C_{OX} \frac{W}{L} (V_{GS} - V_{th}) \quad (3)$$

The minimum length of 180 µm for the transistors has been used.

– Circular spiral inductor

Lesson's phase noise model [25] suggests large Q of the tank to achieve the lower PN. The selection of an inductor in the design of VCO is an important aspect. A three terminal circular spiral inductor model L_SLCR20K_RF from UMC 0.18 µm RF compemetary metal oxide semiconductor (CMOS) process library in spectre RF has been employed to design the proposed VCO. The various parameters of the spiral inductor having 7.14 nH inductance is given in Table 1. The inductance value can be adjusted by the number of turns, width and diameter. The inductance value affects the tank amplitude and start-up constraints.

Table 1. Spiral inductor's parameter (UMC process technology)

Parameter	Size/value
Diameter (µm)	126
Width (µm)	6
Number of turns	5.5
Inductance (nH)	7.14

– MOS varactors

The tuning of a spiral inductor is not possible by some control voltage, so we need some varactor to implement the VCO. Because of its wider capacitance range compared to junction varactor, the inversion metal oxide semiconductor (IMOS) varactor has been employed as a tuning element of LC VCO.

$$f_0 \cong \frac{1}{2\pi\sqrt{L(C_v+C_{avg}+C_{par})}} \quad (4)$$

Where C_{avg} is the instantaneous average capacitance due to sinusoidal voltage at the gate terminal of varactor, C_v is the varactor capacitance and C_{par} is capacitance due to presence of parasitic. Other than these capacitances, load capacitance (C_L) or external capacitance, whose value depends upon the application (buffer), is also added. These external capacitances also affect the power dissipation. Therefore the value of tuning elements i.e., L or C has to be recalculated. This means the VCO requires redesign for different load [1]. This makes the oscillator design a challenging task. So as this (4) suggests that only inductance or capacitance are tuning elements. The large tuning indicates better design in terms of controllability.

The PMOS transistors instead of NMOS transistors have been used in the varactor design because of its low flicker noise. To reduce the flicker (1/f) noise contributed by MOS switches, the device area can be increased as shown in (5). A larger area means a lower tuning range, so we need to adjust the area properly. The value of K for PMOS is 50 times lower than NMOS, so it gives less drain current thermal noise than NMOS.

$$\overline{i^2_{n,\frac{1}{f}}} = \frac{K}{WLC_{ox}} \cdot \frac{1}{f} \cdot g_m^2 \quad (5)$$

2.2. Design flow

Various design flow for the LC-VCO have been proposed in the literatures [22], [26]. Design specifications originate from the application where VCO is being used. Technology file or foundry to be used is also an important criterion. Next, there is a need to identify the design variable available for the design. The important design variables are MOS transistor size, the geometrical parameter of the inductor, and a number of transistor arrays in the varactor. The design flow is shown in Figure 1.

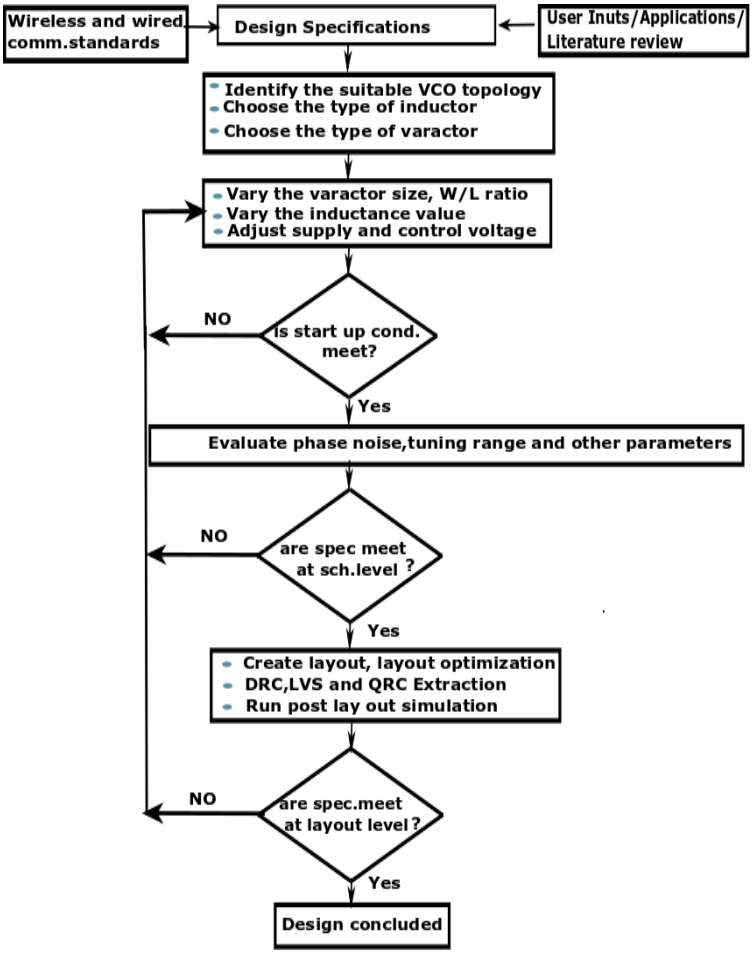


Figure 1. Design flow for the proposed LC-VCO

3. INDUCTIVE SOURCE DEGENERATION BASED LC-VCO

The noise associated with tank and active circuits are the intrinsic noise sources that cannot be permanently removed. Active devices contribute major noise as compared to other components of the VCO. The designers have minimal options like device selections, and setting bias operating points. To minimize the phase noise. The PN models discussed in [25], [27] gives some insights into low PN VCO design. As per the lesson's equation [25], tank Q, active circuitry, signal power, and other frequency parameters are the important consideration for low phase noise. The flicker noise reduction mechanism was discussed in [28], [29]. Various techniques exist to reduce the phase noise performances in VCO [29], [12], [30], [31], [16]. The VCO design techniques need to be investigated in several aspects to obtain a better PN performance. The tail current transistor used in conventional LC-VCO as shown in the Figure 2(a) contributes to phase noise. As reported in [12], [15], [10] noise from tail transistor can be effectively suppressed by filtering techniques. Here, we present the inductive source degeneration technique for low phase noise VCO design.

3.1. Circuit architecture and analysis

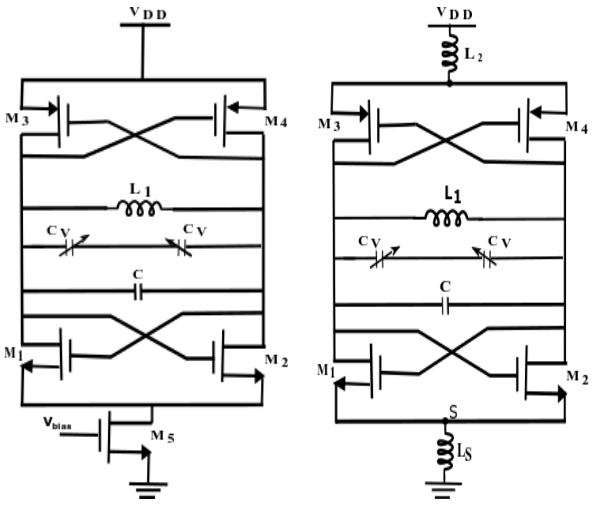
Figure 2(a) shows the conventional design of LC-VCO while Figure 2(b) shows the proposed double CC VCO with inductive source degeneration. The advantages of these differential topologies are that they can directly drive circuits that require a differential input. The complementary cross-coupled configuration has been used to compensate losses produced by tank circuits and active sources. This complementary structure gives double transconductance compared to conventional all NMOS structure at the cost of tuning range and thus relaxes the start-up criteria. The negative resistance which is required for start-up oscillation may be expressed as:

$$R_{neg} = \frac{-2}{g_{mn}+g_{mp}} \leq R_{eq} \quad (6)$$

Where R_{neg} is the equivalent negative resistance offered by double cross-coupled transistor, R_{eq} is the parallel resistance provided by LC tank, g_{mn} and g_{mp} are the transconductance of NMOS and PMOS transistor respectively.

In differential CC LC oscillator, tail current generator at source is considered the major source of flicker noise. The close-in PN is dominated by the up-converted flicker noise of the tail current [30], [32], [33]. Most of the complementary structures either use NMOS or PMOS tail current sources. In any balanced circuit, even harmonics flow in a common mode path; therefore, there is a need for high impedance to even harmonics of the oscillation frequency. The high impedance offered by the tail current source also helps to avoid the degradation of the resonator's quality factor [12].

Source degeneration scheme is an excellent technique to suppress flicker noise up-conversion into phase noise [34]. Several circuit structures using source degeneration techniques such as inductive degenerated, resistive degenerated, capacitive degenerated, and LC filtering technique [12], [31] are presented in various research papers. By removing the tail current generator in the proposed design, the close in phase noise could be improved, but this will impair the quality factor of resonator and due to the absence of high impedance, oscillator will be more sensitive to ground noise. So, instead of tail current generator, an inductor is inserted.



(a) (b)

Figure 2. VCO: (a) traditional implementation of double CC VCO and (b) topology with added ISD

In perfectly balanced LC-VCO, odd and even harmonics are present. The odd harmonics exist in a differential path with no current flowing through the tail transistor. Opposite to that, even harmonics flow from supply to ground path, including the tail transistor. The nonlinearities in the oscillator are responsible for converting low-frequency noise of the tail transistor into high-frequency noise around the even harmonics and the down-converting to the PN around the carrier. The effect of higher-order harmonics on the phase noise is neglected oweing to their low level.

The inductor provides a high impedance common node for differential pairs at the cost of the area. A spiral inductor (L_s) is used to resonate in parallel with parasitic capacitance C_p at source node (S). If the value of inductor (L_s) is chosen in such a way that ω_s (resonant frequency at source node) is equal to the second harmonic frequency ($2\omega_o$) of the oscillator, then impedance (Z_s) at source node seen from differential transistor is approximately infinite [35]. The Resonant frequency at output node is depicted in Figure 3(a). The Resonant frequency at source node (S) as shown in Figure 3(b) and Figure 3(c) is:

$$\omega_s = \frac{1}{\sqrt{C_p L_s}} = 2\omega_o \tag{7}$$

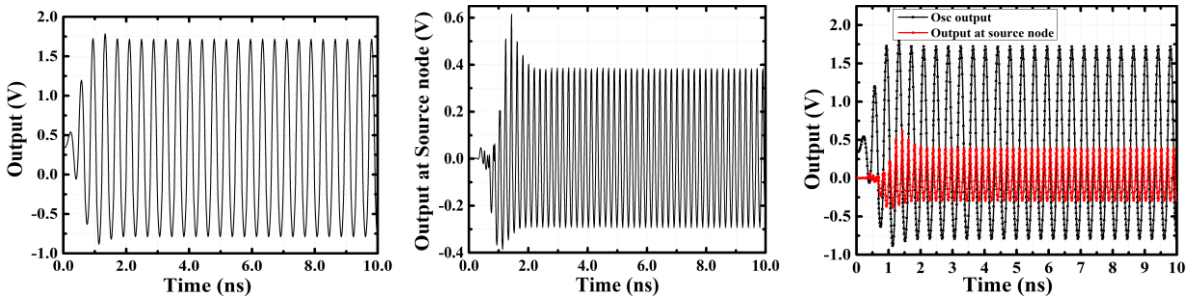
Where ω_s is the resonant frequency at source node, L_s is the series inductor and C_p is the total capacitance at the source terminal (S) of the oscillator including parasitic capacitance and source capacitance of NMOS transistors. This can be shown:

$$Z_s = \frac{j2\omega_o L_s}{1-(2\omega_o)^2 L_s C_p} = \frac{j2\omega_o L_s}{1-\frac{(2\omega_o)^2}{(\omega_s)^2}} \tag{8}$$

It can been seen from (8), as ω_s (Figure 3(b)) is approximately equal to second harmonic of oscillator frequency (ω_o) (Figure 3(a)), the impedance Z_s at source node approaches infinity, and the Q of the inductance-capacitance tank is maintained. A symmetrical waveform is also helpful to get the lower PN [36]. So in the proposed design, W/L ratio of tramsostors of CC is chosen to have equal rise and fall time in the waveform. To obtain symmetrical waveform, the transconductance of PMOS and NMOS transistors should be equal. This leads to (9):

$$\sqrt{2\mu_n I_{ds} \frac{W_n}{L_n} C_{ox}} = \sqrt{2\mu_p I_{ds} \frac{W_p}{L_p} C_{ox}} \tag{9}$$

Where μ_n and μ_p are the surface mobilities of NMOS and PMOS channel respectively, C_{ox} is the capacitance per unit area of the gate oxide, $\frac{W_p}{L_p}$ and $\frac{W_n}{L_n}$ are the effective channel width-length ratio of PMOS and NMOS device respectively.



(a) (b) (c)

Figure 3. Simulated waveform: (a) single-ended output signal (ω_o), (b) second harmonic of oscillating frequency ($2\omega_o$) at source node (S), and (c) at the source and output node

The higher sensitivity of the oscillating frequency to voltage supply (frequency pushing) can be lowered by inserting an inductor (L_2) having 3.5 nH inductance between a supply voltage and resonator. In addition to that, it also provides a high impedance path between resonant tank and power supply (V_{DD}). Variation in the oscillation frequency has been obtained by varying the control voltage of IMOS varactor consisting of 5 parallel units of two series connected back to back PMOS transistor.

4. RESULTS AND DISCUSSION

The performance of the design is greatly affected by the parasitic resistance and capacitance present in the layout. The good layout design considerably reduces the degrading of the system performance. The complete layout of the proposed inductive source degeneration-based LC-VCO is drawn using Cadence Virtuoso layout suite XL with UMC process parameter as shown in Figure 4. It consists of three spiral inductor, a varactor bank, and CC pairs of the transistor. The spiral inductors occupy the 99% area in the layout. The total area is 477 µm × 545 µm. After design rule check (DRC) and layout versus schemetic (LVS), quantus parasitic extraction was performed to extract the parasitics offered by the design. The dimensions and values of the transistor are given in Table 2.

Post layout simulation from the extracted cell view is required to evaluate the effect of parasitic on the system's performance. This also helps a designer to get the results closer to reality. Here in this work, post layout simulations were carried out with UMC 0.18 µm process by spectre simulator of cadence tools. The periodic steady state (PSS) simulation is performed to evaluate the tuning range of the proposed VCO. IMOS varactor consisting of PMOS transistors has been used to regulate the tuning range. The VCO exhibits a turning range from 2.22 GHz to 2.71 GHz when the control voltage varies from 0.8 V to 1.8 V, as shown in Figure 5. Phase noise performance represents the spectral purity of the output signal. The plot shown in Figure 6 shows the single sideband PN with respect to relative frequency from the carrier for the proposed and conventional design.

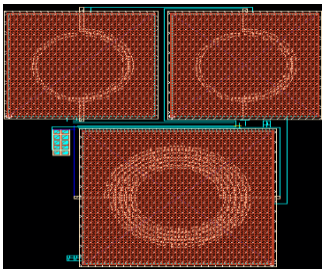


Figure 4. Layout of the proposed ISD based LC-VCO

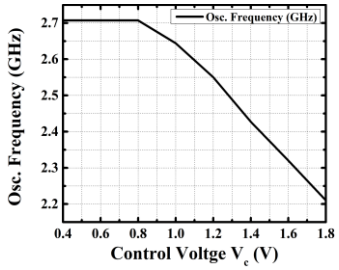


Figure 5. Tuning range of the proposed VCO

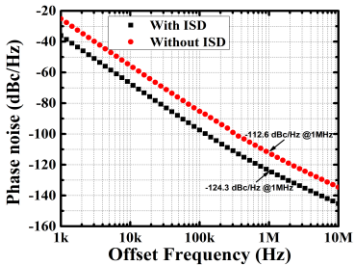


Figure 6. PN performance with and without ISD technique

Table 2. Transistor aspect ratio of the proposed VCO

Components	Device size / values	Fingers
M_1, M_2	2.4 µm / 0.18 µm	1
M_3, M_4	6.0 µm / 0.18 µm	1
PMOS transistor of varactor	9 µm / 0.18 µm	10

At offset frequency of 1 MHz, the PN achieved for this technique is -124.3 dBc/Hz, which can meet the specification of ISM band applications. Using the proposed technique, PN improvement of -11.7 dBc/Hz at a frequency offset of 1 MHz is achieved compared to the conventional design. A buffer amplifier is not considered in the design but output power must have a reasonable value. The output spectrum is shown in Figure 7. The VCO gain (K_{VCO}) with respected to tuning voltage is ploted in Figure 8. The Monte Carlo (MC) simulation for 1000 sample has been performed to examine the effect of process variation on the phase noise. The MC simulation based histogram is ploted in Figure 9. The VCO draws a current of 1.166 mA from the supply voltage of 1.8 V. The performance of VCO may be evaluated in terms of various specifications like PN, power dissipation, output amplitude, and tuning range. There are several figure of merits (FOMs) to evaluate the performance metrics of a VCO. The following equation is widely used to evaluate the performance of VCO [37].

$$FOM = L(f_{off}) - 20\,log\left(\frac{f_o}{f_{off}}\right) + 10\,log\left(\frac{P_{DC}}{1mw}\right) \quad (10)$$

Where $L(f_{off})$ represents the PN at offset frequency and P_{DC} is the power consumption in mW. The comparison performance of the proposed works with other state of work is given in Table 3.

Table 3. A performance comparison of the proposed work with others

Specifications	This work	[18]	[38]	[11]	[39]
Process technology (µm)	0.18	0.13	0.18	0.18	0.18
Supply voltage (V)	1.8	1.0	1.8	0.5	1.8
Centre frequency (GHz)	2.46	2.28	2.45	2.34	2.47
Frequency range (GHz)	2.22 -2.71	2.17-2.40	2.42 -2.48	2.22-2.46	2.38-2.56
Tuning range (%)	19.87	10	2.44	10	7.28
PN (dBc/Hz @ 1 MHz)	-124.3	-114.7	-124	-119.4	-97.76
Power dissipation (mW)	2.10	0.262	2.86	3.23	3.78
FOM (dBc/Hz)	-189	-188.15	-187.25	-181.3	-161
Layout area (µm × µm)	477×545	365 ×473	521 × 234	390×860	-

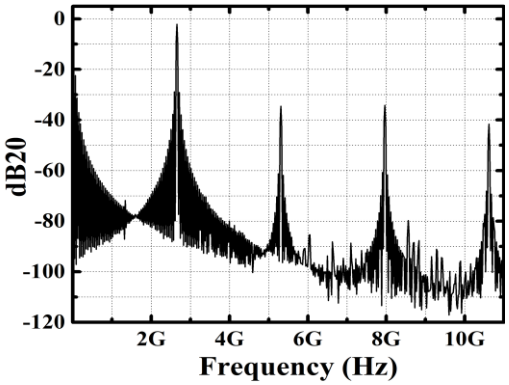


Figure 7. Output power spectrum

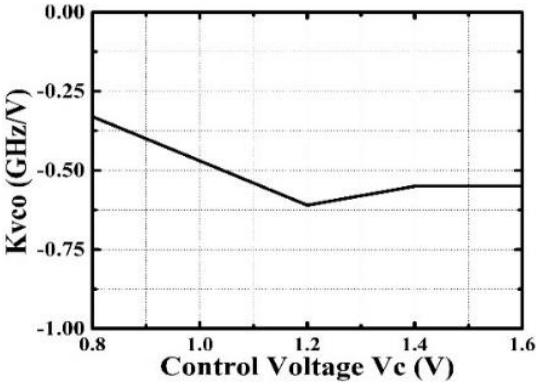


Figure 8. VCO gain with respect to tuning voltage

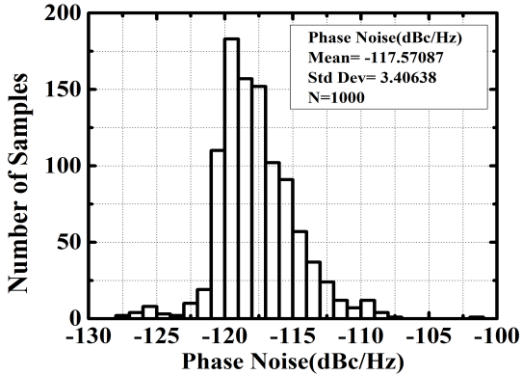


Figure 9. MC simulation-based histogram of PN

5. CONCLUSION

In this paper, the proposed design of LC-VCO was discussed with a focus on phase noise performance. The basic step in the design of VCO is the selection of a suitable topology. The design methodology for VCO was presented. The design, implementation, and layout of CMOS LC-VCOs were accomplished using Virtuoso analog design environment with UMC process parameter, and post layout simulations were performed using spectre. The low phase noise technique, namely inductive source degeneration were investigated. With low phase noise ISD, satisfactory performance of the VCO with phase noise of -124.3 dBc/Hz at 1 MHz offset frequency was obtained. The post layout simulation results confirm that these VCOs can meet the specification for applications in the 2.2 GHz to 2.7 GHz unlicensed ISM bands. The performance outcomes validate the effectiveness of the topologies and methodologies used in the design.

ACKNOWLEDGEMENTS

Authors extend thanks to SMDP-C2SD (A Project of Ministry of Electronics and Information Technology, Govtorment of India) for providing VLSI-Electronic Design Automation tools in the laborotary.

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