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Optimization of 14 nm double gate Bi-GFET for lower leakage current

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ABSTRACT

In recent years, breakthroughs in electronics technology have upgraded the physical properties of the metal oxide semiconductor field effect transistor (MOSFET) toward smaller sizes and improvements in both quality and performance. Hence, the growth field effect transistor (GFET) is being promoted as one of the worthy candidates due to its superior material characteristics. A 14 nm horizontal double-gate bilayer graphene field effect transistor (FET) utilizing high-k and a metal gate, which are composed of hafnium dioxide (HfO_2) and tungsten silicide (WSi_x) respectively. Silvaco ATHENA and ATLAS technology computer-aided design (TCAD) tools are used to simulate the design and electrical properties, while Taguchi L9 orthogonal arrays (OA) are used to optimize the electrical properties. The threshold voltage (V_{TH}) adjustment implant dose, V_{TH} adjustment implant energy, source/drain (S/D) implant dose, and S/D implant energy have all been investigated as process parameters, while the V_{TH} adjustment tilt angle and the S/D implant tilt angle have been investigated as noise factors. When compared to the initial findings before optimization, the I_{OFF} has a value of 29.579 nA/µm, indicating a significant improvement. Findings from the optimization technique demonstrate excellent device performance with an I_{OFF} of 28.564 nA/µm, which is closer to the international technology roadmap for semiconductors (ITRS) 2013 target.

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1. INTRODUCTION

For the past five decades, the scaling down of complementary metal-oxide semiconductor (CMOS) technology has been completely achieved by scaling down their physical dimensions and increasing device switching speed in accordance with Moore's law. Thus, maintaining the off-state power consumption for metal oxide semiconductor (MOS) devices became exceedingly challenging [1], [2]. Advanced CMOS technology is moving toward the development of shorter, thinner gate oxides. Smaller channel thicknesses are preferred to reduce drain-induced barrier lowering. However, the quantum effects limit the channel thickness selection. This leads to a substantial rise in quantum effects next to the silicon interface, which is primarily responsible for the carrier charge distribution in the channel, particularly in the inversion rule of the channel.

To accurately simulate a metal oxide semiconductor field effect transistor (MOSFET), all of these factors must be taken into consideration. When charge carriers are quantized in the continuous energy band, they must be transferred from the valence band to the conduction band, increasing the required gate voltage. In this scenario, the quantum mechanical (QM) phenomenon takes place, and as a result of this quantization phenomenon, the threshold voltage of the device increases [3]–[7]. Another design used to address the short channel effect (SCE) problems is the double gate (DG) MOSFET architecture [8]. It is because by raising the number of gates in the channel, the electrostatic regulation of the channel is improved, and the short-channel effects are decreased. Short-channel effects occur as a result of the impact of the electric field flowing from source to drain on the control of the gate channel. The multi-gate MOSFET is a good choice because it can deal with short-channel effects and keep the device stable [4]. The double gate MOSFET has faster switching operation than planar MOSFETs. Since it can be driven independently, the double gate MOSFET is frequently seen as being desirable in power applications [9], [10]. When compared to silicon, graphene is described as a crystalline allotrope of carbon with two-dimensional properties. It is considered to be the most attractive candidate since it has higher electron mobility, higher current capability and is less dense [11], [12]. Despite its excellent electrical properties, graphene field-effect transistors (GFETs) are still challenging to use in digital logic because graphene does not have a band gap in its normal state, making the field effect transistor (FETs) difficult to switch off. The only known material with an adjustable band gap is bilayer graphene, which is composed of two layers of carbon [13].

Leakage current (I_{OFF}) in a device is a crucial electrical characteristic to consider in device characterization, design, and circuit design since device downscaling has brought the drain area significantly closer to the source [14]. The increase in leakage current is believed to be triggered by changes in process parameters. According to a previous study, the temperature can affect ionic current, causing an increase in off-state current and a decrease in the I_{ON}/I_{OFF} current ratio, and it can also affect leakage current, causing an increase in leakage current due to the increase in heating current [15]. The process parameters employed in the design process, such as the V_{TH} adjustment implantation, the threshold voltage (V_{TH}) energy, the source/drain (S/D) implantation, and the S/D energy, must be optimized for a robust design. Various different input process characteristics need to be examined in order to identify the leakage current's (I_{OFF}) main causes. High-k dielectric materials are suggested as a gate oxide control strategy to deal with the excess I_{OFF} problem. To solve the issue of excessive I_{OFF}, it is being explored to introduce high-k dielectric materials as one of the gate oxide management solutions. Additionally, a high-k dielectric can be used to achieve a larger gate capacitance at a greater thickness [16], [17].

It has been discovered that hafnium dioxide (HfO_2) serves as a high-k dielectric material, and tungsten silicide (WSi_x) serve as a metal gate. HfO_2 is considered to be the most ideal high-k dielectric material for gate oxides because it exhibits the least amount of gate leakage and the highest performance when dealing with short channel effects such as subthreshold swings (SS), leakage current (I_{OFF}), and I_{ON}/I_{OFF} ratio, among others. Traditional polysilicon/silicon dioxide (poly-Si/SiO2) technology might still be used in small-scaled MOSFET devices to meet the International Technology Roadmap for Semiconductors (ITRS) 2013 requirements for low power (LP) technology. However, conventional poly-Si/SiO_2 technology is no longer practical because short channel effects and poly depletion effects degrade transistor performance below the 22 nm technology node. Furthermore, since silicon dioxide (SiO_2) has a higher subthreshold leakage than HfO_2, its leakage is bigger HfO_2 [18]. Due to the obvious high dielectric constant of HfO_2, it has been proposed as a potential high-k material [19], [20]. A decrease in the amount of gate voltage required to increase the drain current has been achieved by using WSi_x and HfO_2 as substitutes for polysilicon and SiO_2, respectively [21]. The thickness variation of the pillar is essentially nonexistent in a high-k/metal-gate design since there are no effects on polysilicon depletion. Since WSi_x is compatible with both negative channel metal oxide semiconductor (NMOS) and positive channel metal oxide semiconductor (PMOS) devices, the metal-gate work-function engineering patent facilitates its usage as a metal gate. WSi_x is believed to have a variety of applications and strong thermal stability and conductivity [17], [22].

The Silvaco application programme, as well as the ATHENA and ATLAS modules, were used to simulate the manufacturing process of virtual devices and analyse their electrical properties [23]. For optimising the process parameters to achieve a robust design at the lowest possible cost, the Taguchi approach is a crucial factor to consider. In a certain process or design, the Taguchi technique, also known as the optimal input process parameter values, can be used to identify the ideal input process parameter values to be used. The Taguchi approach was chosen for this investigation because of its time efficiency and high durability [24]. Various researchers have successfully used the L9 orthogonal array (OA) Taguchi technique to improve process parameters in order to achieve the lowest I_{OFF}, as anticipated in the ITRS 2013 report [25]–[27].

2. METHODOLOGY

It was conceivable to construct a 14 nm horizontal double gate n-channel bilayer graphene with a high-k/metal gate by using the ATHENA module of the Silvaco technology computer-aided design (TCAD) tools while the ATLAS module of the Silvaco TCAD tools was used to acquire the electrical properties of the device. The fabrication step uses the same current top transistor well-matched procedure to produce results that satisfy traditional ITRS requirements while varying a number of design factors, including doping density, energy, and tilt angle. It is used in this area of the device to dope boron at a dosage of 1.0×10^{14} ions/cm^3 and to dope a silicon substrate with an orientation of <100>, which is 8 nm in size and p-type. The threshold voltage adjustment is carried out in the channel area of the transistor using a boron dose of 1.13×10^{13} cm^3 at 20 KeV and a tilt of 10°. A bilayer graphene material with a thickness of 1 nm and a length of 24 nm was then deposited on top of the silicon layer, and the process was repeated. HfO_2 with a permittivity of 25 was used in this study [28]. A 2 nm thick layer of HfO_2 was placed on top of bilayer graphene with a length of 24 nm, which was followed by the deposition of a WSi_x with a 3 nm thick layer. After that, etching is employed to achieve the necessary thickness, and the gate length of 14 nm is accomplished. It was determined that the WSi_x gate would have a 4.5 eV metal-gate work function. For the source drain implant, arsenic was administered at a dose of 1×10^{17} at a frequency of 2 KeV tilted at 77° at a dose of 1×10^{17} cm^3. After that, a coating of aluminum was added to the structure, and any excess aluminum was etched aside. This allowed the contacts to be formed. Once the transistor has been exposed to the electrical characterization procedure using the ATLAS simulation module, it is possible to determine and examine the threshold voltage of the transistor in relation to ITRS. The value of the I_{OFF} must be lower than 100 nm for the 14 nm gate length in order for the device to function properly [29]. The summarized for the simulation recipe of 14 nm NMOS horizontal double gate is shown in Table 1.

Four control factors and two noise factors were selected for this study based on the findings of previous research and were tested [30]. The control factors in this study are the threshold voltage (V_{TH}) adjustment implant dose, threshold voltage (V_{TH}) adjustment implant energy, S/D)implant dose and S/D implant energy while the noise factors are S/D implant tilt angle and threshold voltage (V_{TH}) adjustment tilt angle. Table 2 shows the values of each parameter at various levels, while Table 3 shows the noise factors for n-type MOSFETs.

Table 1. Horizontal double gate fabrication recipe

Process step	n-type MOSFET parameters
Silicon substrate	<100> orientation
V_{th} adjust implant	1.13e13cm^3 Boron Dose
	20 KeV implant energy
	10° tilt
	30 rotations
Bilayer graphene deposition	Thickness: 0.001 µm
	length: 0.024 µm
High-k/metal gate deposition	HfO_2 thickness: 0.002 µm
	HfO_2 length: 0.024 µm
	WSi_x thickness: 0.05 µm
	WSi_x length: 0.014 µm
Source/drain implantation	1e17cm^3 implantation dose
	2 KeV implant energy
	77° tilt
	60 rotations
Aluminium deposition	0.016 µm

Table 2. Process parameters and their levels

Symbol	Process parameter	Unit	Level 1	Level 2	Level 3
A	V_{TH} adjustment implant dose	Atom/cm^3	1.03×10^{13}	1.13×10^{13}	1.23×10^{13}
B	V_{TH} adjustment implant energy	KeV	18	20	22
C	S/D implant dose	Atom/cm^3	0.8×10^{17}	1×10^{17}	1.2×10^{17}
D	S/D implant energy	KeV	1.8	2	2.2

Table 3. Noise factors and their levels

Symbol	Noise factor	Unit	Level 1	Level 2
X	V_{TH} adjustment implant tilt	Degree	10	12
Y	S/D implant tilt	Degree	77	79

3. RESULTS AND DISCUSSION
3.1. Fabrication Simulation Result

A set of software tools from Silvaco TCAD was used to conduct electrical characterization of the 14 nm n-channel horizontal double gate bilayer graphene field effect transistor (Bi-GFET). In Figure 1, Silvaco ATHENA is used to display the completed device for a 14 nm n-type horizontal double gate MOSFET with a bilayer graphene/high-k/metal gate. The device is shown in its completed form since it has been constructed. Due to the obvious change in the design of the gate, the amount of doping introduced into the device has changed because of the change in design. Figure 1 shows the silicon, graphene, high-k/metal gate, and aluminium configurations of the 14 nm NMOS horizontal double gate MOSFET design in 14 nm HfO_2/WSi_x technology. Figure 2 shows material measurements of the device, and Figure 3 shows the doping profile of the 14 nm NMOS horizontal double gate MOSFET design.

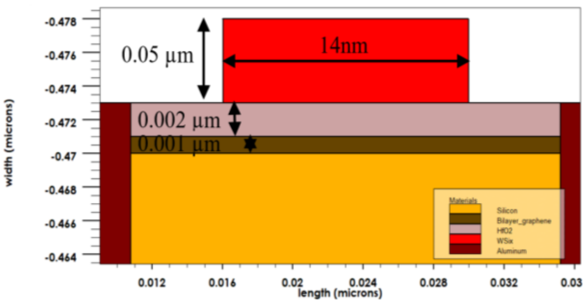

Figure 1. The measurement of the material in 14 nm horizontal double gate of NMOS transistor

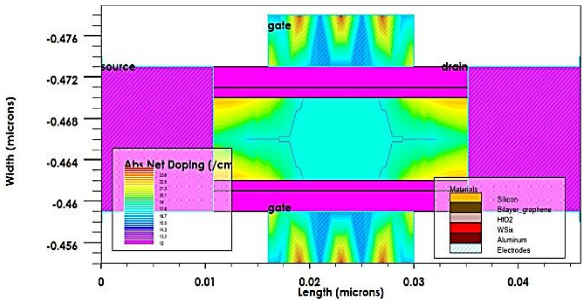

Figure 2. The doping profile of 14 nm double gate NMOS

3.2. Signal-to-noise ratio (SNR) analysis

Using the Taguchi L9 orthogonal array approach researchers were able to achieve the lower leakage current predicted by ITRS 2013. In this experiment, the smaller the grade attributes of the I_{OFF}, the better the grade attributes. The following stage was to discover the control parameters that have the greatest impact on the device features in order to have a better knowledge of the device characteristics. One of the steps is the analysis of the experiment's SNR. In this experiment, the I_{OFF} analysis is referred to as SNR smaller the better (STB), and the purpose of the analysis is to determine the amount of control factors that result in an outcome value that is as near to as possible to the predicted value by ITRS 2013, which is less than 100 nm in this experiment. When the signal to noise ratio of a process parameter is the highest, it is assumed that the factor has a stronger signal than the combination of the random effects of the noise factors. The best lowest quality characteristic type was chosen in this investigation to achieve the lowest I_{OFF} value predicted by ITRS. As indicated in Table 4 below, the L9 orthogonal array approach was used to optimize the I_{OFF} of the NMOS transistor, and the outcomes of this optimization are displayed.

Next, compute the factor effect percentage on SNR for NMOS transistors. The SNR of each level of the process parameter for I_{OFF} is outlined in Table 5. The Table 5 impact comes to illustrate that S/D implant energy (D) has the most elevated impact on minimizing I_{OFF} esteem within the NMOS device, with 94.09%, followed by S/D implant dose (C) with 4.82%. On the other hand, V_{TH} adjustment implant energy (B) only gives a 0.62% effect on the device, followed by the V_{TH} adjustment implant dose (A) with 0.46%.

Table 4. Result for I_{OFF} value based on L9 orthogonal array

Exp no.	Leakage current, I_{OFF} (nA/µm)				Overall mean	SNR
	$X1, Y1$	$X1, Y2$	$X2, Y1$	$X2, Y2$		
1	30.566	30.678	30.565	30.677		150.28
2	29.614	29.672	29.609	29.667		150.56
3	28.885	28.926	28.875	28.915		150.78
4	28.825	28.853	28.815	28.841		150.80
5	30.211	30.306	30.209	30.304	150.56	150.38
6	29.815	29.883	29.811	29.879		150.50
7	29.339	29.386	29.334	29.380		150.65
8	29.048	29.086	29.041	29.078		150.73
9	30.374	30.476	30.372	30.475		150.34

Table 5. SNR of each level of process parameters

Process parameter	SNR (dB)			Factor effect on SNR (%)
	Level 1	Level 2	Level 3	
V_{TH} adjustment implant dose	150.54	150.56	150.57	0.46
V_{TH} adjustment implant energy	150.58	150.56	150.54	0.62
S/D implant dose	150.50	150.57	150.60	4.82
S/D implant energy	150.33	150.57	150.77	94.09

Figure 3 shows factor effect plot of control factor levels for signal noise ratio smaller the better (SNR STB) in decibel (dB). On the graph shown, the dotted boundaries represent the values of the total mean of SNR (STB) which is 150.56 dB. Each process parameter's level value is shown on the graph as well. From the left, V_{TH} adjustment implant dose (factor A), V_{TH} adjustment implant energy (factor B), S/D implant dose (factor C) and S/D implant energy (factor D) are all shown in the graphs, with the slopes corresponding to each of them.

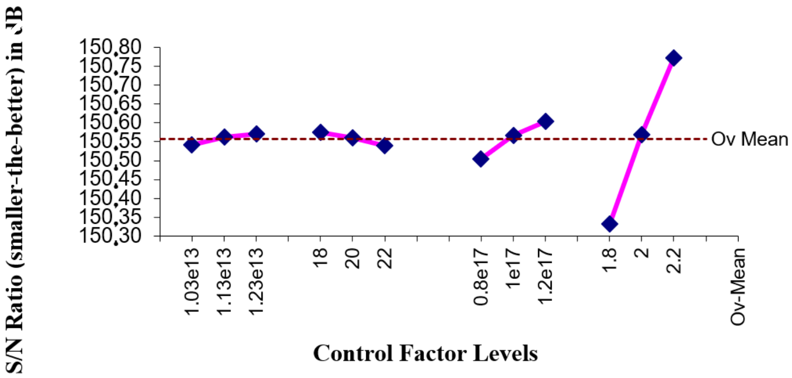

Figure 3. Factor effect plot for SNR (smaller the better)

3.2.1. Analysis of variance (ANOVA)

The variance (ANOVA) of the input process parameters is a commonly used statistical method for determining which of those input process parameters appears to have a significant impact on the performance character trait during an investigation [31]. The standard deviation of the experimental tests is used to determine the standard deviation of the experimental data from the mean value of data in data analysis. Table 6 displays the results of the ANOVA for the device under consideration. As a percentage of the factor effect on SNR, SNR shows which process parameters are most critical. In terms of the effect of factors on SNR, the influence of the Table 6 shows that S/D implant energy (D) has the most impact on reducing I_{OFF} esteem within the NMOS device with 94.09%. At present, S/D implant dose (C) has the largest instantaneous highest effect with 4.82%, followed by V_{TH} adjustment implant energy (B) with 0.62%, and lastly, V_{TH} adjustment implant dose (A) has the least percentage that gives effect to the device with 0.02%.

Table 6. Results of ANOVA for I_{OFF}

Process parameter	Factor effect on SNR (%)
V_{TH} adjustment implant dose	0.46
V_{TH} adjustment implant energy	0.62
S/D implant dose	4.82
S/D implant energy	94.09

Table 7. Best setting parameter for I_{OFF}

Symbol	Process parameter	Level	Best value (atom/cm^3)
A	V_{TH} adjustment implant dose	3	$1.23X10^{13}$
B	V_{TH} adjustment implant energy	1	18
C	S/D implant dose	3	$1.20X10^{17}$
D	S/D implant energy	3	2.2

3.2.2. Confirmation test

The optimum process parameter levels predicted by the L9 orthogonal array (OA) of the Taguchi technique were used to re-simulate the 14 nm Bi-GFET horizontal double gate device, as Table 7. The Table 7 shows the optimal process parameter levels. The SNR (mean) value with the highest value is the ideal level for device design in the event of I_{OFF}. According to the finalized standards, levels A3, B1, C3, and D3 are the finalized specifications for an I_{OFF} built exclusively for NMOS devices. Based on the Taguchi approach, Table 8 shows the optimal anticipated Taguchi method setting for the I_{OFF} process parameter combination. Using these final numbers and the noise factor, Table 8 displays the optimal I_{OFF} result with the lowest feasible value. Following the last step in the process to improve the noise factor parameter, the results with the I_{OFF} value are lower than the results with the ITRS prediction value.

Table 8. Confirmation results for I_{OFF} using L9 OA of Taguchi method

I_{OFF} 1(nA/µm) $X1, Y1$	I_{OFF} 2(nA/µm) $X1, Y2$	I_{OFF} 3(nA/µm) $X2, Y1$	I_{OFF} 4(nA/µm) $X2, Y2$
28.576	28.593	28.564	28.579

As another researcher of 14 nm have been reported was planar MOSFET design and fin field effect transistor (FinFET) design technology [32], [33]. According to ITRS 2013, the leakage current for 14 nm must be less than 100 nm, and this research revealed that the value of 28.564 nm is in accordance with ITRS 2013, indicating that the value is in line with ITRS 2013. When it comes to parameter optimization, the Taguchi technique is widely accepted. In this case, the Taguchi approach was used in the design of a 14 nm n-type MOSFET to achieve the lowest possible value of the I_{OFF} predicted by the ITRS. Throughout this finding, it was discovered that S/D implant energy (D) has the highest impact on decreasing I_{OFF} esteem within the NMOS device, with a reduction of 94.19% compared to base. Thus, minor changes in the energy of the S/D implant would have a significant impact on the I_{OFF} value. Table 9 shows the leakage current simulation results of 14 nm Bi-GFET horizontal double gate after optimize using Taguchi L9.

Table 9. Simulation results of 14 nm Bi-GFET horizontal double gate

Performance parameter	ITRS prediction	Non-optimized results	Optimized result
		29.579	28.564
I_{OFF} (nA/µm)	<100	Reduction value (%)	
		70.421	71.436

4. CONCLUSION

Consequently, using Silvaco ATHENA and ATLAS TCAD tools, the proposed structure of a 14 nm gate length horizontal double gate bilayer graphene field effect transistor with a high-k dielectric function and a metal gate HfO_2/WSi_x was simulated and modeled. The finalized layout was then optimized using Taguchi L9 OA. Prior to optimization, the results for the horizontal double gate design were 29.579 nm, with a reduced value of 70.431%, while the optimized results were 28.564, with a better reduction value of 71.436%, while the I_{OFF} value for the planar design from the earlier study is higher than the double gate, which is 77.11 nm. According to the author's knowledge, this study is the first to utilize a bi-layer graphene, high-k, metal gate, and horizontal double gate MOSFET and optimize by using L9 orthogonal array of the Taguchi method on a 14 nm device.

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