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Design of 15 level reduced switches inverter topology using multicarrier sinusoidal pulse width modulation

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ABSTRACT

In this proposed paper, multicarrier sinusoidal pulse width modulation (M-SPWM) method is implemented for design of 15 level reduced switches inverter topology. This inverter topology generates 15 level output-voltage with suitable switching pulse production using M-SPWM and altered level of voltages are attained with distinction of modulation index. The split inductor is used to diminish the harmonic content and flatted output current. This type of system which contains different range of different range of voltage supplies. As a result, this inverter reduces the difficulty in gating time calculation and there is no neutral point fluctuation issue. This paper illuminates the modes of switching and minimization of stress in voltage and harmonic diminution are examined. The grades of the projected multilevel inverter (MLI) system are verified using Matlab/Simulink and dsPIC controller respectively.

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1. INTRODUCTION

Multilevel voltage source inverters have been attracting a lot of coverage over the past few decades owing to their significant advantages, and have emerged as a practical option for high-power DC to AC conversion applications [1]–[4]. The amplitude of the voltage is raised using multilevel methodology, the tension in the switching devices is decreased, and the overall harmonics profile is enhanced. A multilevel inverter (MLI) is a linking system with several dc input rates (acquired from dc sources and/or capacitors) and semiconductor control devices to amalgamate a waveform of a staircase [5], [6]. For multilevel inverters three separate topologies have been proposed: diode-clamped [7] capacitor-clamped; and multi-cell cascaded with independent DC outlets. The power efficiency of multilevel converters is increased as the amount of rates at the output voltage decreases.

It also raises the number of switching devices and other parts, raises the difficulty of cost and control and helps to reduce the overall converter durability and performance. Multilevel inverter work proceeds to reduce the amount of switching devices counted and reduce the cost of producing, capacitor voltage balancing, which is the aim of our article [8]–[10]. This article is primarily regarding the topology of the h-bridge inverter. This multilevel inverter has the ability to be among three topologies most efficient. Because of its modularity it has the highest resistance, a function that enables the inverter to continue to work at lower power rates after cell failure [11]. After offering an description of multilevel inverters, we define our proposed five-level inverter.

Then we performed simulation tests that are obtained in the matlab-simulink setting. Eventually, we analyze the effects of the simulation and illustrate an change in the sinusoidal waveform [12].

Abundant modulation strategies were urbanized to organize converter power switches [13]. In that, the converter with high frequency pulse width modulation (PWM) methods like carrier based modulation, trapezoidal method, sinusoidal PWM, space vector modulation and multicarrier based PWM used [14], [15]. Moreover, selective and active harmonic exclusion nearest vector control method and synchronous optimal PWM are used for converter with low frequency PWM techniques [16], [17]. Reduced switches MLIs are predominantly used nearest state control and multicarrier based sinusoidal PWM (SPWM) schemes [18], [19].

In this projected work, system attains 15 level output voltage with minimized no of switches. It provides better description compare conventional methods like diminished total harmonic distortion (THD) low stresses across switches, and controlled output current and condense cost of the system. Switches used in this projected method are embarrassed by multicarrier based sinusoidal pulse width modulation, which avoids the shoot through problem.

2. POWER STAGE

2.1. Circuit configuration

Figure 1 shows the proposed novel topology for 15 level inverter. It consists of three DC source voltages are 10 V, 20 V and 40 V. The power switches S1, S2, S3, S4, S5, and S6 connected directly to DC sources, which decide the level output voltage from the proposed scheme. The switches S7, S8, S9, and S10 performing a voltage source inverter (VSI) bridge, which chooses the positive and negative assortment of output voltage ranges with R load is connected across bridge arrangement. The anticipated system generates 15 level output voltage with appropriate gate pulse production. Number devices used in this projected process determined by switch level ratio (SLR) relation, which enclose totally 10 power switches. Doesn't necessitate of any extra converter like boost or flyback or single-ended primary-inductor converter (SEPIC) converter to boost voltage to stability the required range.

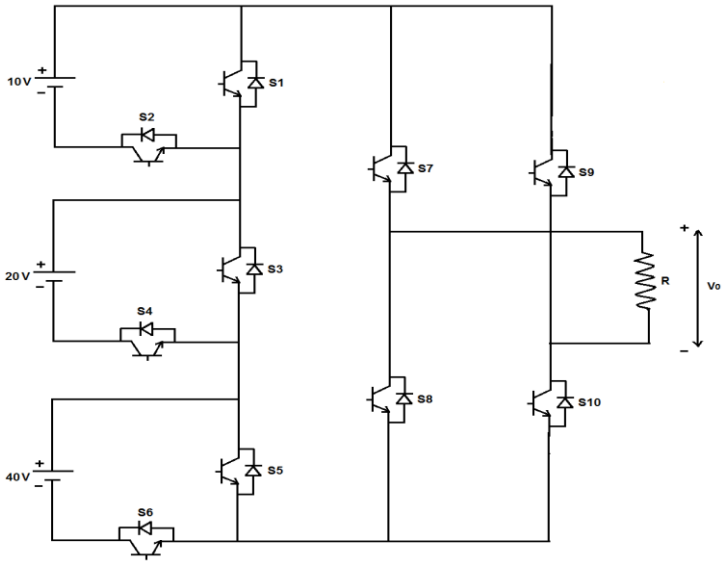


Figure 1. Circuit diagram for 15-level inverter with reduced switches

2.2. Modes of operation

The projected scheme engenders 15 level output voltages (+V_{dc}, +6/7 V_{dc}, +5/7 V_{dc}, +4/7 V_{dc}, +3/7 V_{dc}, +2/7 V_{dc}, +1/7 V_{dc}, 0, −1/7 V_{dc}, −2/7 V_{dc}, −3/7 V_{dc}, −4/7 V_{dc}, −5/7 V_{dc}, −6/7 V_{dc}, −V_{dc}).

a) To acquire output voltage of V_0 = +1/7 V_{dc}, switches S2, S3, and S5 reserved on to get 1/7th voltage from the power circuit and switches S7 and S10 are turned on to obtain positive level. Figure 2(a) illustrates the current flow path for this mode and Table 1 confirms the various switching permutation for 15 level output voltage.

b) To acquire output voltage of V_0 = +2/7 V_{dc}, switches S1, S4, and S5 reserved on to find 2/7th of supply voltage and from bridge circuit switches S7 and S10 are turned on to get optimistic level. Figure 2(b) demonstrates the current flow path for system.

c) To accomplish output voltage of V_0 = +3/7 V_{dc}, switches S2, S4, and S5 kept on to get 3/7th of supply voltage and from bridge circuit switches S7 and S10 are turned on to get optimistic level. Figure 2(c) demonstrates the current flow path for this mode.

d) To achieve output voltage of V_0 = +4/7 V_{dc}, switches S1, S3, and S6 reserved on to get 4/7th of supply voltage and from bridge course switches S7 and S10 are turned on to get positive output level. Figure 2(d) demonstrates the current flow path for this mode.

Similarly, the proposed system operated under different modes of operation, which is Table 1.

Table 1. Switching combinations of proposed system for 15-level output voltage

Level	Voltage ranges	On position
I	+ V_{dc}	S2, S4, S6, S7, S10
II	+6/7 V_{dc}	S1, S4, S6, S7, S10
III	+5/7 V_{dc}	S2, S3, S6, S7, S10
IV	+4/7 V_{dc}	S1, S3, S6, S7, S10
V	+3/7 V_{dc}	S2, S4, S5, S7, S10
VI	+2/7 V_{dc}	S1, S4, S5, S7, S10
VII	+1/7 V_{dc}	S2, S3, S5, S7, S10
VIII	0	S7, S9
IX	–1/7 V_{dc}	S2, S3, S5, S8, S9
X	–2/7 V_{dc}	S1, S4, S5, S8, S9
XI	–3/7 V_{dc}	S2, S4, S5, S8, S9
XII	–4/7 V_{dc}	S1, S3, S6, S8, S9
XIII	–5/7 V_{dc}	S2, S3, S6, S8, S9
XIV	–6/7 V_{dc}	S1, S4, S6, S8, S9
XV	–V_{dc}	S2, S4, S6, S8, S9

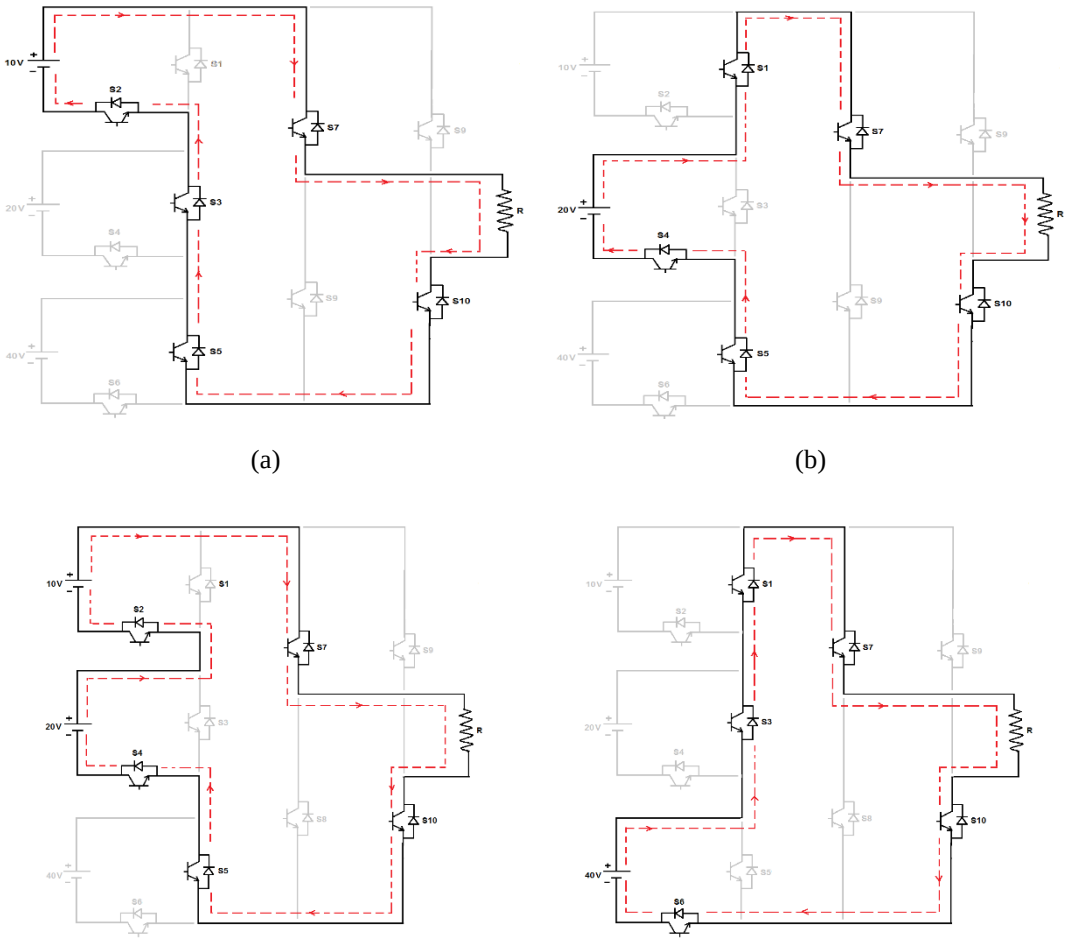


Figure 2. Modes of operations positive and zero level: (a) +1/7 V_{dc}, (b) +2/7 V_{dc}, (c) +3/7 V_{dc}, and (d) +4/7 V_{dc}

Commonly voltage balancing evils happens due to non-uniform switching, non-ideal DC link capacitors, and asymmetrical commutation switches, unsymmetrical current and inoculation of current flow. It belongings on presentation of inverter humiliate, augment of voltage stress, supplementary harmonic twist and augment in load current magnitude. But this projected scheme evades above reveal restrictions, due to that capacitor balancing not obligatory.

3. MULTICARRIER SINUSOIDAL PULSE WIDTH MODULATION

Multicarrier SPWM multicarrier sinusoidal pulse width modulation (MSPWM) control strategy is developed to acquire 15 level output from the projected system. In this technique sinusoidal reference is compared with multiple triangular carrier signal; by that the desired gate signal are engendered for switches placed in proposed 15-level inverter [20]–[23]. This method provides better performances compare to classical PWM methods. When number levels in the inverter increase with reduced number of switches, advanced PWM methods are not suitable like space vector pulse width modulation (SVPWM), hysteresis PWM, elimination-based methods [24], [25]. In this projected scheme, modulation index plays a major role to produce required gate pulses for the inverter circuit. Modulation index M_i is written as:

$$M_i = \frac{V_{sin}}{3 \times V_{tag}} \quad (1)$$

Then the output voltage of projected scheme based on the applied input voltage and modulation index, which is defined as:

$$V_0 = M_1 \times V_{dc} \quad (2)$$

To acquire 15 level output from the projected system, sinusoidal reference is compared with other signals, Figure 3 shows the M-SPWM with sine type reference signal, triangular type carrier signal and gate pulses. Based on this assessment gating pulse engendered for the power devices of projected inverter, this is distinct as:

- $V_{sin} < 0$ and $V_{sin} > V_{tag1}$ ⟶ S1 switched ON
- $V_{sin} > 0$ and $V_{sin} < V_{tag2}$ ⟶ S2 switched ON
- $V_{sin} > V_{tag4}$ ⟶ S4 switched ON and $V_{sin} < V_{tag}$ ⟶ S3 switched ON
- $V_{sin} > V_{tag5}$ ⟶ S5 switched ON and $V_{sin} < V_{tag4}$ ⟶ S6 switched ON
- $V_{sin} > V_{tag6}$ ⟶ S7 switched ON
- $V_{sin} > V_{tag3}$ ⟶ S8 switched ON

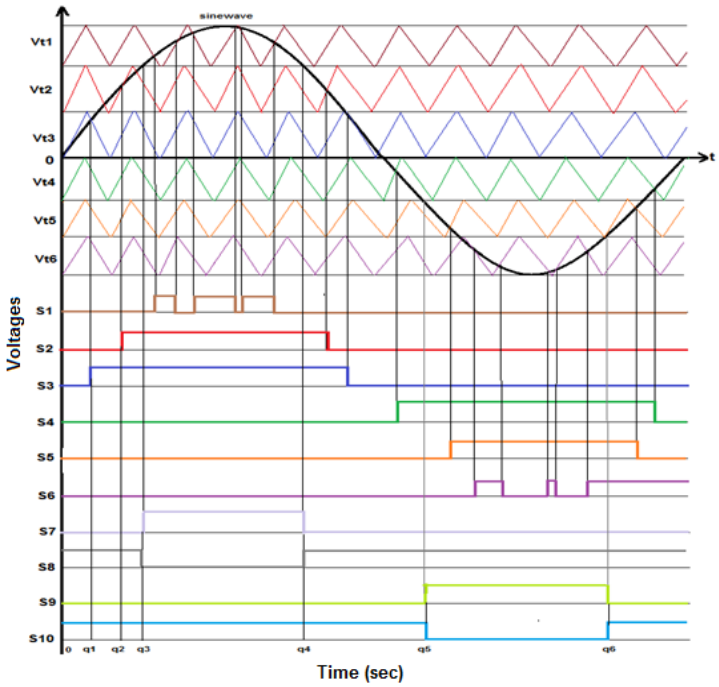


Figure 3. MSPWM reference and carrier types signal and gating pulses

4. SIMULATION RESULTS

The projected 15 level inverter topology is replicated using Matlab/Simulink 2016a. The simulation results are acquired with switching frequency of 10 kHz and gating pulses are engendered using M-SPWM with partial output (PO) technique. Projected scheme includes of three dc voltage input of V_a = 10 V, V_b = 20 V and V_c = 40 V. The simulation results projected system has the subsequent characters:

– It accomplishes diodes and passive components, when number level augment, tradition of diode will enlarge.
– Complication of the controller is supplementary, when integer of level augments.

The 15-level inverter includes power circuit and MSPWM technique. It includes proportional integral (PI) controller to tune actual voltage as a sinusoidal voltage. The projected 15-level output with 69.56 V, which is revealed in Figure 4. Total harmonic deformation for voltage range and proscribed current of planned 15 level schemes is 10.38% and 6.36% correspondingly, which is uncovered in Figure 5(a) and Figure 5(b). In Figure 6 shows inverter productivity voltage with attached inductor, which is worn to flat output voltage and current and also abolishs the tradition transformer that can diminish cost of the scheme and leakage current issues. Mi will formulate a pronouncement the output voltage ranges. When modulation index Mi of 0.75 with voltage of 48.9 V and Mi of 0.81 with voltage of 64.9 V and Mi of 0.95 with output voltage of 68.96 V, which is Figure 7(a), Figure 7(b) and Figure 7(c). In Figure 8 shows the comparison between number of levels and modulation index and Figure 9 shows comparison between SLR ratio and multilevel inverter.

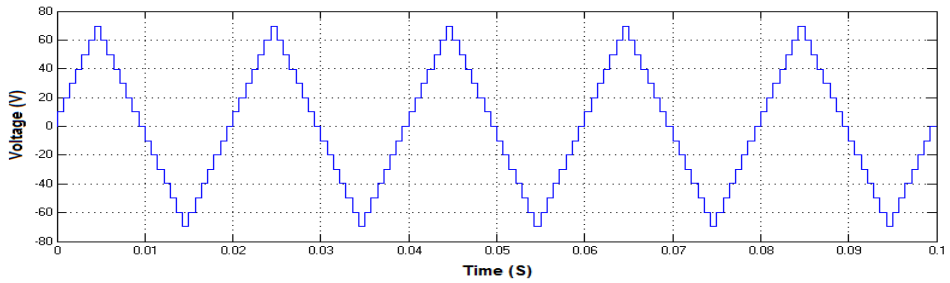
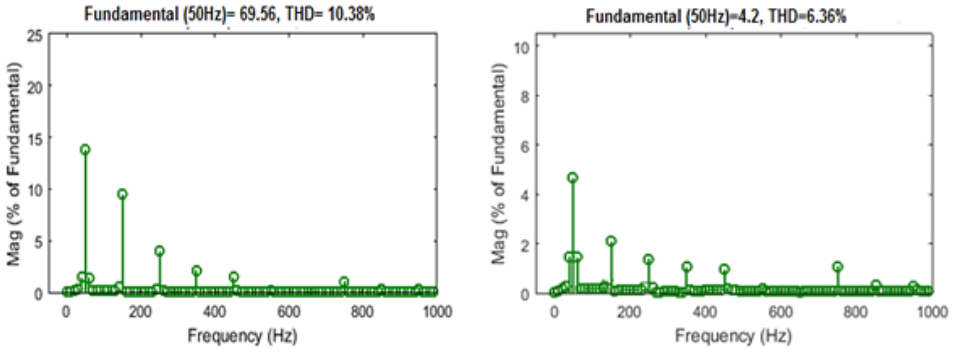


Figure 4. 15 level output voltage waveform



(a) (b)

Figure 5. THD analysis: (a) output voltage and (b) controlled current

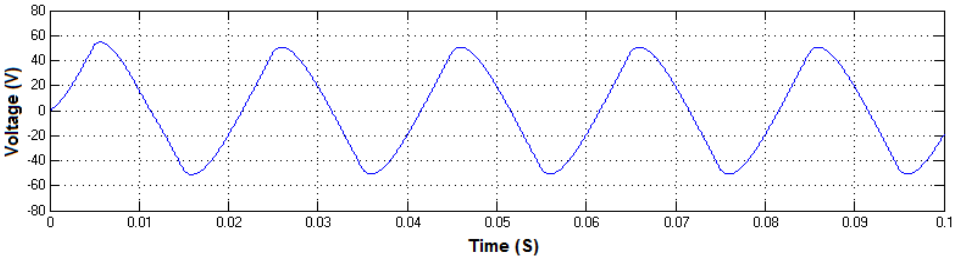
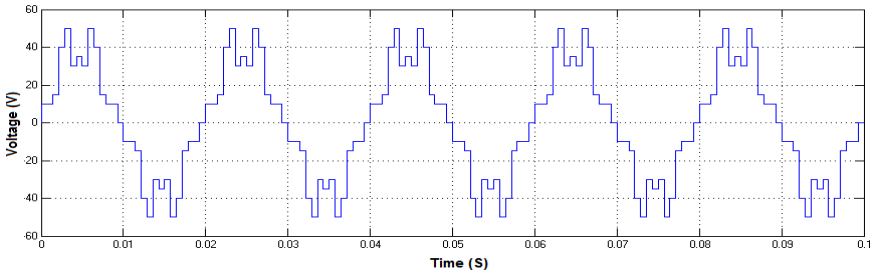
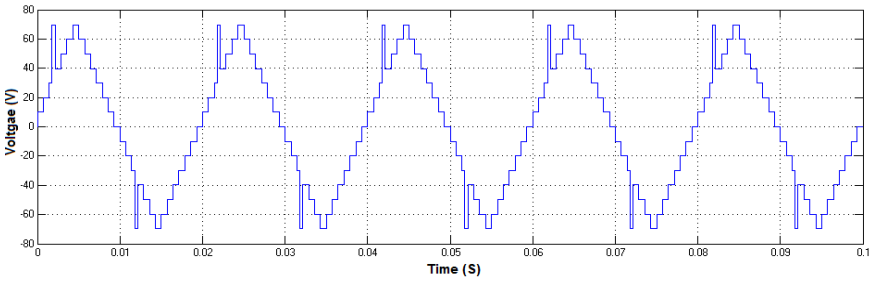


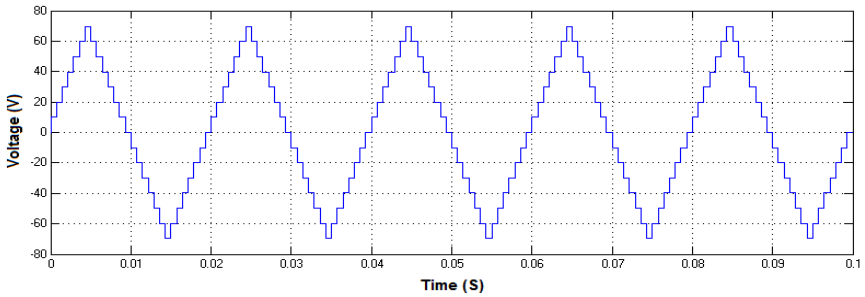
Figure 6. Inverter output voltage with split inductor



(a)



(b)



(c)

Figure 7. Output voltage for various MI: (a) 0.75, (b) 0.81, and (c) 0.955

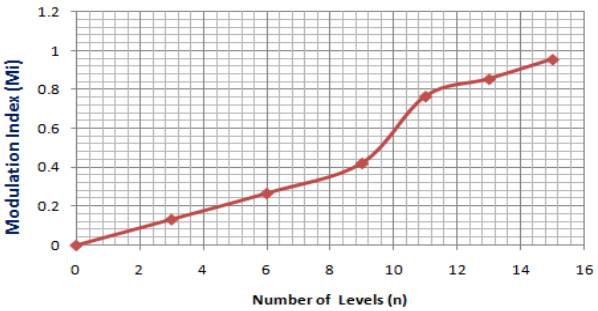


Figure 8. number of levels VS modulation index

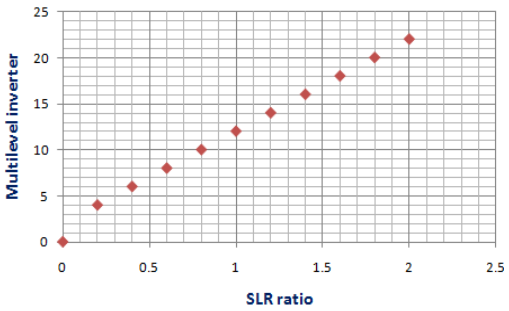


Figure 9. SLR ratio VS multilevel inverter

5. EXPERIMENTAL RESULTS AND DISCUSSION

To verify the simulation results of proposed novel 15-level inverter, the experimental setup was developed using dsPIC controller. The proposed novel 15-level inverter is connected and various parameters are calculated the resistive load condition. In Figure10 shows 15-level output voltage waveform, with 120 V and Figure 11(a) and Figure 11(b) shows the gating pulse for switches S1 and S2 for respectively. Voltage across the various switches has different voltage level, which is Figure 12.

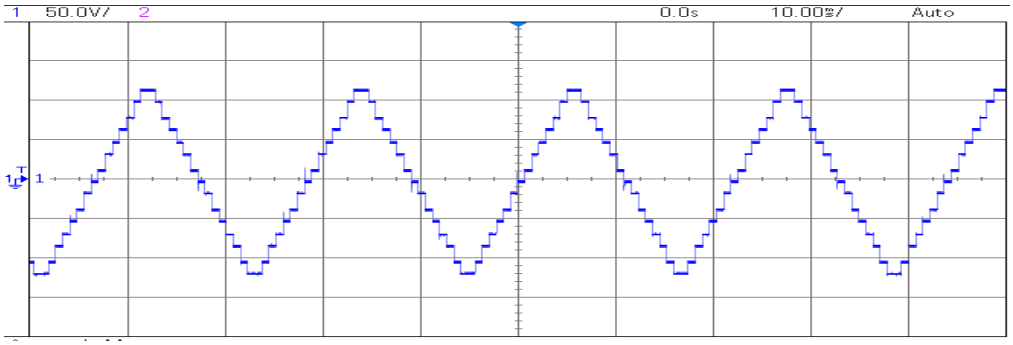
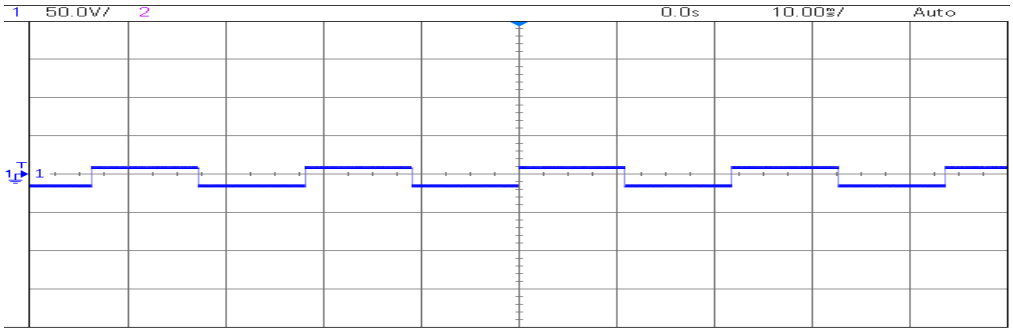
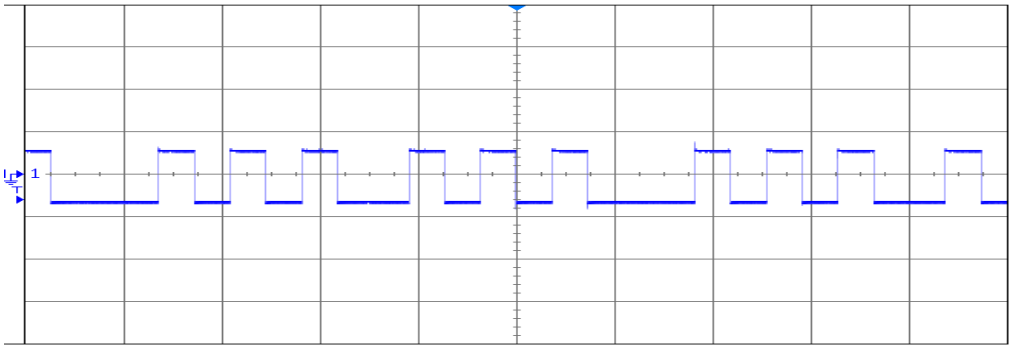


Figure 10. 15 level output voltage from the proposed inverter system



(a)



(b)

Figure 11. Gating pulses of proposed system: (a) S1 and (b) S2

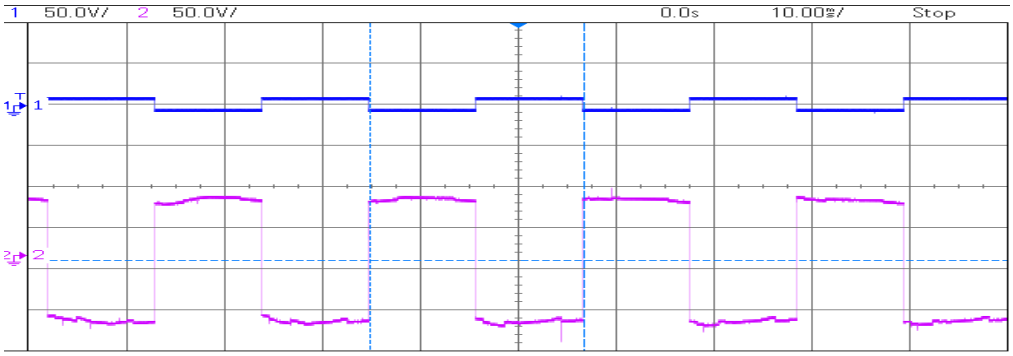


Figure 12. Voltage across switch S1 and S2

6. CONCLUSION

This paper is recognized an innovative 15 level DC-AC converters with determined switches. Based on SLR relation the number of devices and level of inverter can be accomplished. Projected inverter power devices are controlled by MSPWM control, and with help of coupled inductor which recommend high reliability output voltage and low leakage current issues. At the same time, plummeting of capacitor balancing, diminish the harmonic ranges and obtain approach from the shoot-through case. The projected 15-level inverter can achieve superior efficiency, low cost and elevated consistency. 15 level output voltage with help of 10 power switches with Mi = 0.95 and different level of output voltages are obtained with variation of Mi. Accomplished better current control and voltage control of 15-level proposed inverter scheme with THD of 6.26% and 10.28% respectively.

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