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Proposing a new method for calculating DC sources in an extended multilevel converter

Afzal Keivanlou Shahrestanaki[1], Rahim Ildarabadi[1], Mahmoud Zadehbagheri[2], Tole Sutikno[3,4]
[1]Department of Electrical Engineering, Hakim Sabzevari University, Sabzevar, Iran
[2]Department of Electrical Engineering, Yasuj Branch, Islamic Azad University, Yasuj, Iran
[3]Master Program of Electrical Engineering, Faculty of Industrial Technology, Universitas Ahmad Dahlan, Yogyakarta, Indonesia
[4]Embedded System and Power Electronics Research Group, Yogyakarta, Indonesia

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ABSTRACT

In this paper, we propose a method for calculating the DC source amplitude in an extended multilevel inverter (MLI) structure so that the maximum number of levels and the output voltage waveform are as close as possible to the sinusoidal wave with minimum total harmonic distortion (THD). For the developed structure, three algorithms are suggested to determine the amounts of DC voltage resources. The first important point about choosing the right amounts for the DC resources is that the number of levels should be as large as possible, and the second important point is that the intervals between the levels should be the same throughout the waveform. By observing these two points, the output voltage waveform can be as near as possible to the sinusoidal wave that we want. In this study, we used iteration-based methods to find suitable values for DC sources. Simulation results are offered to confirm the capability of the extended multilevel converter. After we solved the problem through calculation and analysis, a code was written in MATLAB with the aim that this time the code will tell us for what values of DC sources we will have the largest number of levels and as we expected, the output of the MATLAB code confirmed the correctness of the calculations.

Corresponding Author:

Rahim Ildarabadi
Department of Electrical Engineering, Hakim Sabzevari University
Sabzevar, Iran
Email: r.ildar@hsu.ac.ir

NOMENCLATUR

$I(t)$: Instantaneous current
n_p: Number of voltage levels
$V_{AN}(t)$: Voltage of phase-to-neutral
I_c: Current of conduction (through the switches)
N_{level}: Number of levels (output voltage waveform)
N_{switch}: Number of switches
T_{s-on}: Time switch (turn on)
$V(t)$: Instantaneous voltage
A_k: Switching angle
$d(t)$: Instantaneous duty cycle
V_{uc}: Upper arm instantaneous capacitor voltage
M: Index of modulation
N_L: Number of voltage levels
$V_{AB}(t)$: Instantaneous output voltage (line-to-line)
N_c: Number of capacitors (each arm)
Vdc: DC voltage source (isolated)
N_{step}: Number of steps
Ts_{-off}: Time switch (turn off)
T_{total}: Time total (switch is on)
V_{Block}: Blocking voltage (switch)
V_c: Voltage of conduction (through the switches)
Θ_o: Phase-shifted sinusoidal modulator
$V_n(t)$: Instantaneous voltage (switch of the nth inverter leg)
f_o: Frequency modulator

W_o: Angular frequency modulation
V_{LC}: Lower arm capacitor voltage
V_{of}: Voltage magnitude of fundamental component
V_{oi}: Voltage magnitude of harmonic components

1. INTRODUCTION

For the first time, David Prince published an article titled "Inverter" in General Electric Review in 1925. In that article, he listed almost all the parts needed in inverters [1]. Currently, inverters have become an integral part of many electrical appliances, from household appliances such as refrigerators and washing machines to advanced industrial and military equipment. From another viewpoint, inverters are used in all stages from producing electricity in power plants and transmission lines to the customer end. In simple terms, an inverter is a device that converts DC voltage to AC voltage with the desired frequency and amplitude [2]–[4]. There are different types of inverters depending on the type of application as well as the type of circuit topology. One of the most widely used inverters is multilevel inverters (MLIs), which have been widely studied today. The most important challenge for this type of inverter is to increase the number of output voltage levels to bring the output voltage waveform closer to the sine wave, as well as to reduce the number of components and voltage sources used in them, provided that reducing the components does not reduce the quality of the output waveform, and we see that many papers have been published in recent years with the phrase "reduced device count" and similar phrases in the title of the paper [5]–[8]. Today, MLIs are used in a variety of industrial applications. Such as renewable energy (RE) and flexible AC transmission system (FACTS) devices. Multilevel converters have many benefits, such as improving the output voltage, reducing the total harmonic distortion (THD) and reducing the stress on the switches compared to typical two-level converters [9].

MLIs have several different topologies, such as H-bridges, neutral point clamps (NPCs), and flying capacitors (FCs). They can also be used to drive induction motors. One of the most popular topologies for induction motor drives is the NPC type introduced in [10], in which the voltage of capacitors is unbalanced and requires balancing methods [11]. FC topology was introduced in the 1990s by Lavieville *et al*. [12]. A cascaded H-bridge (CHB) multilevel converter was introduced in [13]. It is a suitable topology for FACTS devices such as STATCOM. The disadvantages that can be considered are the level of reliability due to the use of a high number of parts [14] and the high variety in the magnitude of DC voltage sources in CHB inverters [15]. The most common configurations for CHB topology are *binary* and binary; if each voltage source is twice the previous source, the configuration will be binary, and if it is three times, the configuration will be trinary [16], [17].

A new structure of high-level multilevel converter is presented in [18]. The problem focuses on minimizing the number of power MOSFETs for a given number of levels. Different combinations of topologies are presented and the corresponding mathematical relations are obtained. This paper offers optimized curves to obtain the relationship between the minimum number of power semiconductors required for a given number of levels. For example, a CHB converter with three batteries can produce 15 voltage levels in binary and 27 voltage levels in trinary configurations. Therefore, choosing the value of DC sources in multilevel inverters can be one of the most challenging steps for design and researchers may propose several methods for selecting the amplitude of dc sources for each presented topology [19], [20].

PV system converters usually include two section: A DC to DC converter and a PWM inverter. This cascade structure has drawbacks such as reduced efficiency and problems in maximum power point tracking [21]. Introduces a single phase 9-level hybrid inverter (H9LI). An innovative method has been used to balance the voltage of the capacitors in this inverter.

An optimized topology of a 3-phase MLI is presented, in which the parts of level production and sequence generation are separated from each other and become modular [22]. The advantage of this modular structure is that to produce more voltage levels in this inverter, we have to increase the number of components only in the level production part because in this structure, DC sources are shared equally between each phase, and the "asymmetry of the phases" problem is solved [23]. A new method for generating more voltage levels by stacking or connecting multilevel converters that have a spatial vector structure is proposed, one of the advantages of which is the number of DC sources needed less than other structures [24]. A limitation of MLIs is the limitation in switching frequency due to the increase in heat loss, especially at high powers. On the other hand, the smaller the switching frequency, the more harmonics in the output waveform of the inverter, and this is not to our liking [25], [26].

A method was introduced to remove harmonics in the output waveform at low switching frequencies [27]. However, the main idea of this manuscript is obtained from [17], where the author provided a new extended multilevel topology that can be extended in both horizontal and cascade extension modes. After introducing the topology, the main problem is how to choose the value of each DC source for generating maximum voltage levels at the output.

Alishah *et al*. [17], two methods for calculating the value of DC sources in both horizontal and cascade modes are extended, but the reason for using those methods is not mentioned. In this paper, we will show why

the method is presented by [17] in the case of horizontal expansion. In subsection 2.1, the basic unit topology presented by [17] is introduced, and the magnitude of DC sources in the primary unit for creating the maximum voltage levels is calculated in subsection 2.2. Then, the submultilevel topology is introduced in subsection 2.3, and again, the magnitude of DC sources in the submultilevel topology for creating the maximum voltage levels is calculated in subsection 2.4. Finally, in section 3, according to the described process, a MATLAB code was introduced. This code can calculate the best values for DC sources, and its most important feature is that it can be used for any other CHB-based topology [18], [28]. A method for removing the DC component of the output current of transformerless inverters is proposed [19]. The use of two separate paths for two half-cycles of the flow in order to minimize circulating currents has also been suggested in [29].

A new topology for multi-level inverter circuit with series connection is introduced, which is used to connect distributed generation sources to the grid without the need for transformers [1]. Usually, the design of such circuits is based on the ability to inject current and power into the network, minimizing output current harmonics and some physical limitations such as isolating distributed generation sources from the network. In addition to injecting the maximum possible active power, the circuit proposed in this article can also compensate some harmonics of the load current indicator as an active filter. Basic multi-level modules based on switched capacitors are presented for cascade applications, which use series and parallel methods for automatic capacitor voltage balancing [30].

In this paper, a method for calculating the DC source amplitude in an extended multilevel converter topology was presented. The topology consists of a basic module that can be extended to produce more voltage levels. In previous articles, the authors introduced methods to calculate the range of resources, but they did not provide a reason for introducing these methods.

In this research, at the beginning, all the possible modes were extracted to produce voltage at the output. Then, they were sorted from large to small based on the proposed algorithm. Finally, the values of the DC sources were calculated in such a way as to create the maximum number of voltage levels with the same intervals, which leads to a reduction in THD and a smaller number of parts. After we solved the problem through calculations and analysis, a code was written in MATLAB with the aim that this time the code will tell us for what values of DC sources we will have the highest number of levels.

As we expected, the output of the MATLAB code confirmed the correctness of the calculations. This MATLAB code can be used for any other topology in such a way that first, the voltages that can be generated at the output of the circuit are parametrically extracted and fed to the MATLAB code. The most important application of the newly proposed structure is in the drive of electric motors used to remove harmonics using switching and optimization algorithms such as particle swarm optimization (PSO) and Bee. Additionally, direct torque control is another application of the proposed structure in induction motors, which provides less torque ripple.

Additionally, the proposed topology is used in power system applications such as high voltage direct current (HVDC), reactive power compensation, voltage drop compensation, and photovoltaic systems. To show the advantages and capabilities of the proposed structure in this paper, the proposed algorithms are compared with the algorithms and topologies of other papers. As shown in Table 1, these comparisons are studied from the point of view of the number of insulated-gate bipolar transistors (IGBTs), cost, number of voltage levels, number of capacitors and power diodes, and number of impedance sources.

Table 1. Comparison of the number of sources, IGBTs, and cost comparison

References	Algorithm	Number of sources	Number of IGBTs	Number of voltage levels	Number of capacitors	Number of power diodes	Total cost (USD)
[5]	First, second third	6	18	125	4	0	81.5
[11]	Symmetrical	8	20	17	5	8	111.95
[14]	First, second	3	10	13	0	0	66.75
[15]	First, second, third (PWM)	10	20	11	3	0	80.63
[31]	asymmetric	2	9	13	4	0	63.33
[19]	CHB-MLI	5	20	11	0	1	75.03
[20]	First, second third	2	8	11	3	14	141
[24]	First, second, third, fourth	7	16	63	0	19	126.5
[17]	First, second	4	10	39	2	1	–
This paper	First, second, third	4	10	17	0	0	–

2. INTRODUCING THE TOPOLOGY

2.1. Introducing the basic unit topology

The basic circuit of the topology is shown in Figure 1. This topology consists of two bidirectional switches, six unidirectional switches and four DC voltage sources. Each unidirectional switch includes an antiparallel diode and an IGBT. The type of bidirectional switches is a common emitter and consists of two IGBTs and two antiparallel diodes and requires only one gate pulse [5], [30]. The two sources have the same amplitude V1, and the other two sources have the same amplitude $\bar{V}1$. As mentioned, this circuit is a basic circuit that has the ability to produce 17 voltage levels, and the way they produce levels is given in Table 2. To produce more levels, the basic unit can be extended to a submultilevel circuit, as shown in Figure 2.

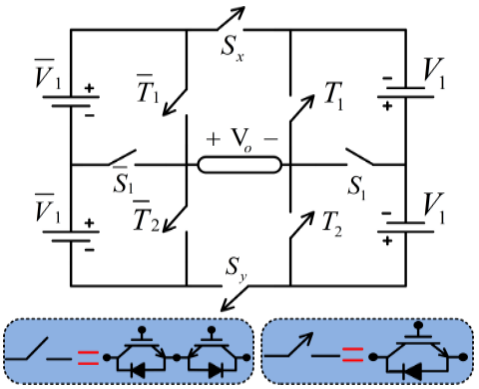

Figure 1. Basic unit circuit for new extended multilevel converter topology

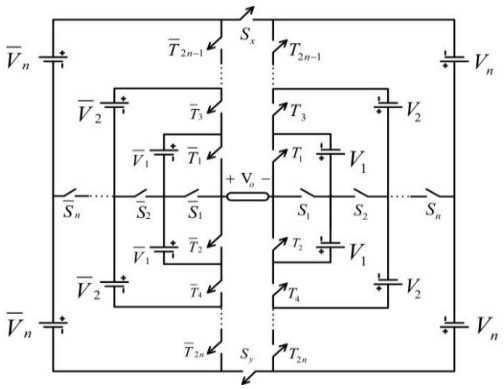

Figure 2. Proposed submultilevel topology

Table 2. Switching states for the basic unit for extended multilevel converter topology

State	ON switches	V_{out}
1	$\bar{T}_1, S_x, T_1$	0
	$\bar{T}_2, S_y, T_2$	
2	$\bar{S}_1, T_2, S_y$	$\bar{V}_1$
3	$\bar{S}_1, T_1, S_x$	$-\bar{V}_1$
4	$S_1, \bar{T}_2, S_y$	V_1
5	$S_1, \bar{T}_1, S_x$	$-V_1$
6	$\bar{T}_1, T_2, S_y$	$2\bar{V}_1$
7	$T_1, \bar{T}_2, S_x$	$-2\bar{V}_1$
8	$T_1, \bar{T}_2, S_y$	$2V_1$
9	$\bar{T}_1, T_2, S_x$	$-2V_1$
10	$S_1, \bar{S}_1, S_y$	$\bar{V}_1 + V_1$
11	$S_1, \bar{S}_1, S_x$	$-(\bar{V}_1 + V_1)$
12	$\bar{T}_1, S_1, S_y$	$2\bar{V}_1 + V_1$
13	$\bar{T}_2, S_1, S_x$	$-(2\bar{V}_1 + V_1)$
14	$\bar{S}_1, T_1, S_y$	$\bar{V}_1 + 2V_1$
15	$\bar{S}_1, T_2, S_x$	$-(\bar{V}_1 + 2V_1)$
16	$T_1, \bar{T}_1, S_y$	$2\bar{V}_1 + 2V_1$
17	$T_2, \bar{T}_2, S_x$	$-(2\bar{V}_1 + 2V_1)$

2.2. Determining the DC sources amplitude for the basic unit

To determine the amplitude of DC voltage sources at each level, Alishah *et al*. [17] proposed two methods, first and second. The procedure is the same in both methods, but the number of levels in the second method is greater than that in the first method, so we only investigate the second method. In this method, the relationships are as (1) and (2) [20], [32].

$$\bar{V}_1 = V_{dc} \quad (1)$$

$$V_1 = 3\,V_{dc} \quad (2)$$

The problem that can be introduced in both methods and the author did not answer to it is that what is the basis of the mentioned relations for calculating the amplitude of DC voltage sources? why the value of V should be 3 times of the value of $\overline{V}$? why not, for example, 4 or 5 times? this is a question that the author has not answered and we will answer to it in this manuscript. As mentioned earlier, all the voltage levels that can be generated using the basic unit shown in Figure 1 are listed in Table 2. There are no other levels because the absolute value of the largest voltage that can be generated is $2\overline{V}_1 + 2V_1$ and the smallest voltage level after zero is $\overline{V}_1$ Additionally, to generate all voltage levels, the spacing between the two levels must be $\overline{V}_1$ because it is the smallest unit of voltage that can be generated by the circuit. If all voltage levels become calculated for various values of V_1 as an integer coefficient of $\overline{V}_1$ just for positive polarity (the negative is similar) from Table 2, we would have:

$$If: V_1 = \overline{V}_1 \xrightarrow{thelevelsare} 0, \overline{V}_1, \overline{V}_1, 2\overline{V}_1, 2\overline{V}_1, 2\overline{V}_1, 3\overline{V}_1, 3\overline{V}_1, 4\overline{V}_1 \quad (3)$$

$$If: V_1 = 2\overline{V}_1 \xrightarrow{thelevelsare} 0, \overline{V}_1, 2\overline{V}_1, 2\overline{V}_1, 3\overline{V}_1, 4\overline{V}_1, 4\overline{V}_1, 5\overline{V}_1, 6\overline{V}_1 \quad (4)$$

$$If: V_1 = 3\overline{V}_1 \xrightarrow{thelevelsare} 0, \overline{V}_1, 2\overline{V}_1, 3\overline{V}_1, 4\overline{V}_1, 5\overline{V}_1, 6\overline{V}_1, 7\overline{V}_1, 8\overline{V}_1 \quad (5)$$

$$If: V_1 = 4\overline{V}_1 \xrightarrow{thelevelsare} 0, \overline{V}_1, 2\overline{V}_1, 4\overline{V}_1, 5\overline{V}_1, 6\overline{V}_1, 8\overline{V}_1, 9\overline{V}_1, 10\overline{V}_1 \quad (6)$$

$$If: V_1 = 5\overline{V}_1 \xrightarrow{thelevelsare} 0, \overline{V}_1, 2\overline{V}_1, 5\overline{V}_1, 6\overline{V}_1, 7\overline{V}_1, 10\overline{V}_1, 11\overline{V}_1, 12\overline{V}_1 \quad (7)$$

It is clear from (5) that for $V_1 = 3\overline{V}_1$, all values are unique, so all 17 voltage levels can be achieved. For $V_1 = 4\overline{V}_1$ and higher coefficients, some levels are lost [33].

2.3. Proposed sub-multilevel converter

To produce more voltage levels, the basic unit can be extended in a way (shown in Figure 2) Alishah *et al*. [17] named it "*Submultilevel*". The topology consists of several legs. Each leg has two dc sources with the same magnitude. However, the magnitude of dc sources in each leg differ from other legs. To calculate the value of DC sources in each leg, the author proposed a method as (8) and (9):

$$\overline{V}_j = 10^{j-1} V_{dc} \; for j = 1,2, \dots, n \quad (8)$$

$$V_j = 3 \times 10^{j-1} V_{dc} \; for j = 1,2, \dots, n \quad (9)$$

In this method, the number of voltage levels is equal to:

$$N_{levels,S} = 16 \times 10^{n-1} + 1 \quad (10)$$

Where n is half the number of legs. Again, the author has not provided any proof for the mentioned relationships, and we will prove them. First, we have listed all possible states where at least one voltage source and V_o can be placed in a closed circuit such that no source is short circuited [34]. These modes are extracted for the circuit shown in Figure 3. To do this, first you need to write down all the combinations that can be made by all the voltage sources. In other words, we need to list all the combinations where 1, 2, 3,…,7 or 8 sources can be selected from among the eight voltage sources. The total number of combinations is 255. Then, we have to check in which cases a closed circuit is created with at least one voltage source; the total number of cases is 98. The next step is to define the sign of the sources relative to the output voltage [35], [36]. These items are extracted and listed in Table 3. Only positive modes are listed, and negative modes are similar because if we look at Figure 3, we can see that the circuit is divided into two halves by the dotted red line and that these two halves are the same. If we want to create a positive voltage at the output, the sources specified in Table 3 should be placed in a closed circuit by the S_y key, and if we want to create a negative voltage, the corresponding sources with the same values in the other half of the circuit should be placed in a closed circuit by the S_x key. To extract all possible states for creating voltage at the output, we replaced the source names with the values shown in Figure 4.

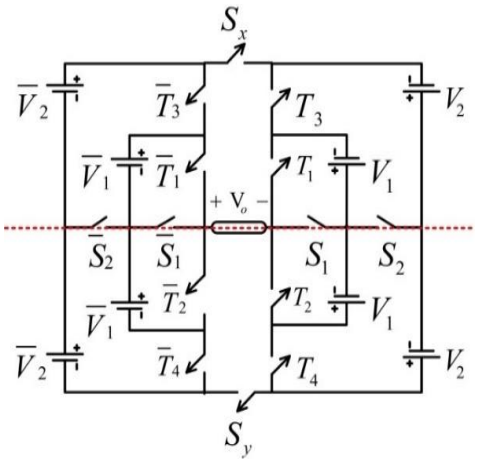

Figure 3. Submillilevel topology with n=2

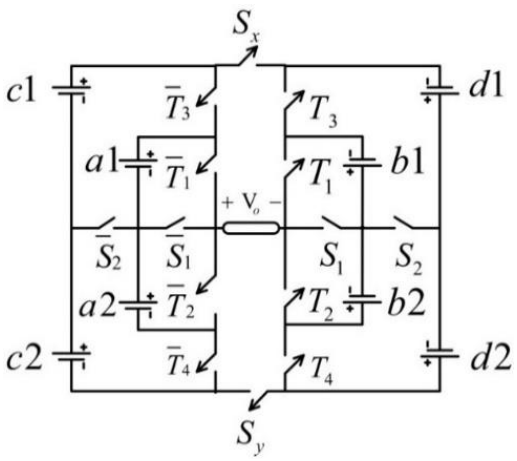

Figure 4. Figure 3 with new source names

Table 3. Possible combinations for creating positive V_O in the circuit shown in Figure 4

State	V_{out}	State	V_{out}	State	V_{out}
1	A1+A2	34	-A1-A2-B2+C1+C2+D2	67	-A2-B1+C2+D1+D2
2	A1+C2	35	-A1-A2+C1+C2+D1+D2	68	A2-B1-B2+C1+D1+D2
3	A1+A2+B2	36	A1-B1-B2+C2+D1+D2	69	-A2-B1-B2+C2+D1+D2
4	A1+A2+D2	37	-A1-B1+C1+C2+D1+D2	70	B1+B2
5	A1+B2+C2	38	-A1-A2-B1+C1+C2+D1+D2	71	B1+D2
6	-A1+C1+C2	39	-A1-B1-B2+C1+C2+D1+D2	72	B1+B2+C2
7	A1+C2+D2	40	-A1-A2-B1-B2+C1+C2+D1+D2	73	B1+C2+D2
8	A1+A2+B1+B2	41	A2	74	-B1+D1+D2
9	A1+A2+B1+D2	42	A2+B2	75	B1+B2+C1+C2
10	A1+A2+B2+D1	43	A2+C1	76	-B1-B2+D1+D2
11	A1+A2-B2+D2	44	-A2+C2	77	B1+C1+C2+d2
12	-A1-A2+C1+C2	45	A2+D2	78	-B1+C2+D1+D2
13	A1+A2+D1+D2	46	A+B1+B2	79	-B1-B2+C2+D1+D2
14	A1+B1+B2+C2	47	A2+B1+D2	80	-B1+C1+C2+D1+D2
15	A1+B1+C2+D2	48	A2+B2+C1	81	-B1-B2+C1+C2+D1+D2
16	-A1+B2+C1+C2	49	-A2+B2+C2	82	B2
17	A1+B2+C2+D1	50	A2+B2+D1	83	B2+C2
18	A1-B2+C2+D2	51	A2-B2+D2	84	B2+D1
19	-A1+C1+C2+D2	52	A2+C1+D2	85	-B2+D2
20	A1+C2+D1+D2	53	-A2+C2+D2	86	B2+C1+C2
21	A1+A2-B1+D1+D2	54	A2+D1+D2	87	B2+C2+D1
22	-A1-A2+B2+C1+C2	55	A2+B1+B2+C1	88	-B2+C2+D2
23	-A1-A2+C1+C2+D2	56	-A2+B1+B2+C2	89	B2+C1+C2+D1
24	-A1+B1+B2+C1+C2	57	A2+B1+C1+D2	90	-B2+C1+C2+D2
25	-A1+B1+C1+C2+D2	58	-A2+B1+C2+D2	91	C1+C2
26	A1-B1+C2+D1+D2	59	A2-B1+D1+D2	92	C1+C2+D2
27	-A1+B2+C1+C2+D1	60	A2+B2+C1+D1	93	C1+C2+D1+D2
28	-A1-B2+C1+C2+D2	61	-A2+B2+C2+D1	94	C2
29	-A1+C1+C2+D1+D2	62	-A2-B2+C2+D2	95	C2+D2
30	-A1-A2+B1+B2+C1+C2	63	A2+C1+D1+D2	96	C2+D1+D2
31	-B1-B2+A1+A2+D1+D2	64	-A2+C2+D1+D2	97	D1+D2
32	-A1-A2+B1+C1+C2+D2	65	A2-B1-B2+D1+D2	98	D2
33	-A1-A2+B2+C1+C2+D1	66	A2-B1+C1+D1+D2		

2.4. Determining the values of DC sources in the sub-multilevel topology

After we have extracted all the possible states to create the voltage at the output, we should discuss the determination of the source values. Given that:

$$a1 = a2 = a\ b1 = b2 = b\ c1 = c2 = c\ d1 = d2 = d \tag{11}$$

$$a < b < c < d \tag{12}$$

$$b = 3a \tag{13}$$

Replacing ralations 11 in Table 3 results in Table 4. Now, it is time to sort the contents of Table 4 from large to small. The flowchart shown in Figure 4 is proposed by this paper. Based on the proposed procedure, we are sure that the largest V_O that can be produced by the circuit is $2c + 2d$. The largest V_O before $2c + 2d$ must be $-a + 2c + 2d$ because the interval between each two consecutive levels must equal to the amount of the smallest DC source. (i.e., a). Now, we have to check whether this voltage level $-a + 2c + 2d$ exists in Table 4, and the answer is YES. Likewise, the largest V_O before $-a + 2c + 2d$ must be $-2a + 2c + 2d$, which exists in Table 4, and the next V_O must be $-3a + 2c + 2d$, which does not exist in Table 4; however, instead, there is $-b + 2c + 2d$, and from (13), we have ($b = 3a$). If we continue like this, we would have Table 5. The next relation after $-2a - 2b + 2c + 2d$ should be $-3a - 2b + 2c + 2d$ or $-b - 2b + 2c + 2d$, and none of them exist in Table 4. We must search for the largest voltage level among the remaining V_O's and that's $a + c + 2d$ because assuming that relationship 12 is established ($c > a$), all the other voltages are smaller than $a + c + 2d$. Next, V_O after $-a - 2b + c + 2d$ should be $-2a - 2b + c + 2d$ or $a - b - 2b + c + 2d$, and none of them exist in Table 4. We must search for the largest V_O among the remaining $2a + 2d$ in Table 3 because of the following assumption:

$$d > a + 2c \tag{14}$$

Table 4. Table 3 values after replacing (11)

State	V_O	State	V_O	State	V_O
1	*2A*	34	*-2A-B+2c+D*	67	*-A-b+C+2d*
2	*A+c*	35	*-2A+2c+2D*	68	*A-2b+C+2d*
3	*2A+b*	36	*A-2B+c+2D*	69	*-A-2b+C+2d*
4	*2A+d*	37	*-A-B+2c+2D*	70	*2B*
5	*A+B+C*	38	*-2A-B+2c+2D*	71	*B+D*
6	*-A+2c*	39	*-A-2B+2c+2D*	72	*2B+c*
7	*A+C+D*	40	*-2A-2b+2c+2D*	73	*B+c+D*
8	*2A+2b*	41	*A*	74	*-B+2D*
9	*2A+B+d*	42	*A+B*	75	*2B+2c*
10	*2A+b+d*	43	*A+C*	76	*-2B+2D*
11	*2A-b+d*	44	*-A+C*	77	*B+2c+D*
12	*-2A+2c*	45	*A+d*	78	*-B+c+2D*
13	*2A+2d*	46	*A+2B*	79	*-2B+c+2d*
14	*A+2B+c*	47	*A+B+d*	80	*-B+2c+2d*
15	*A+B+C+D*	48	*A+B+c*	81	*-2B+2c+2D*
16	*-A+b+2C*	49	*-A+B+c*	82	*B*
17	*A+b+C+D*	50	*A+b+d*	83	*b+c*
18	*A-b+c+D*	51	*A-b+d*	84	*b+d*
19	*-A+2c+D*	52	*A+c+d*	85	*-b+d*
20	*A+c+2D*	53	*-A+c+d*	86	*b+2c*
21	*2A-b+2D*	54	*A+2d*	87	*b+c+d*
22	*-2a+b+2C*	55	*A+2b+C*	88	*-b+c+d*
23	*-2A+2c+D*	56	*-A+2b+C*	89	*B+2c+D*
24	*-A+2b+2c*	57	*A+b+C+D*	90	*-B+2c+D*
25	*-A+B+2c+d*	58	*-A+b+C+D*	91	*2c*
26	*A-B+c+2d*	59	*A-b+2D*	92	*2c+D*
27	*-A+B+2c+D*	60	*A+b+C+D*	93	*2c+2D*
28	*-A-B+2c+D*	61	*-A+b+C+D*	94	*C*
29	*-A+2C+2d*	62	*-A-b+C+D*	95	*c+D*
30	*-2A+2B+2c*	63	*A+C+2D*	96	*c+2D*
31	*-2B+2a+2D*	64	*-A+C+2D*	97	*2D*
32	*-2A+b+2c+D*	65	*A-2B+2D*	98	*D*
33	*-2A+b+2c+D*	66	*A-B+c+2D*		

Figure 5 shows the proposed algorithm for sorting the values of Table 4 from large to small. All the other voltages are smaller than $2a + 2d$. Finally, the next voltage level after $-2b + 2d$ should be $-a - 2b + 2d$ or $2a - b - 2b + c + 2d$, and none of them exist in Table 4. We must search for the largest voltage among the remaining V_Os in Table 4, which is $b + 2c + d$. From the 10th and 26th rows of Table 5, we have:

$$-9a + 2c + 2d = a + c + 2d \rightarrow c = 10a \tag{15}$$

$$-7a + 2d = b + 2c + d \xrightarrow{c=10a} d = 30a \tag{16}$$

Table 5. Values of Table 4 in order from large to small

State	V_O values after subtracting "a" in order from largest to smallest	The equivalent expression in the Table 3
1	*2C+2D*	*2C+2D*
2	*-A+2c+2D*	*-a+2c+2D*
3	*-2A+2c+2D*	*-2A+2c+2D*
4	*-3A+2c+2D*	*-b+2c+2D*
5	*-4A+2c+2D*	*-A-b+2c+2D*
6	*-5A+2c+2D*	*-2A-b+2c+2D*
7	*-6A+2c+2D*	*-2b+2c+2D*
8	*-7A+2c+2D*	*-A-2b+2c+2D*
9	*-8A+2c+2D*	*-2A-2b+2c+2D*
10	*-9A+2c+2D*	*A+c+2D*
11	*C+2D*	*c+2D*
12	*-A+c+2D*	*-A+c+2D*
13	*-2A+c+2D*	*A-b+c+2D*
14	*-3A+c+2D*	*-b+c+2D*
15	*-4A+c+2D*	*-A-b+c+2D*
16	*-5A+c+2D*	*A-2b+c+2D*
17	*-6A+c+2D*	*-2b+c+2D*
18	*-7A+c+2D*	*-A-2b+c+2D*
19	*-8A+c+2D*	*2A+2D*
20	*A+2D*	*A+2D*
21	*2D*	*2D*
22	*-A+2D*	*2A-B+2D*
23	*-3A+2D*	*-B+2D*
24	*-4A+2D*	*-2B+2a+2D*
25	*-6A+2D*	*-2B+2D*
26	*-7A+2D*	*B+2c+D*

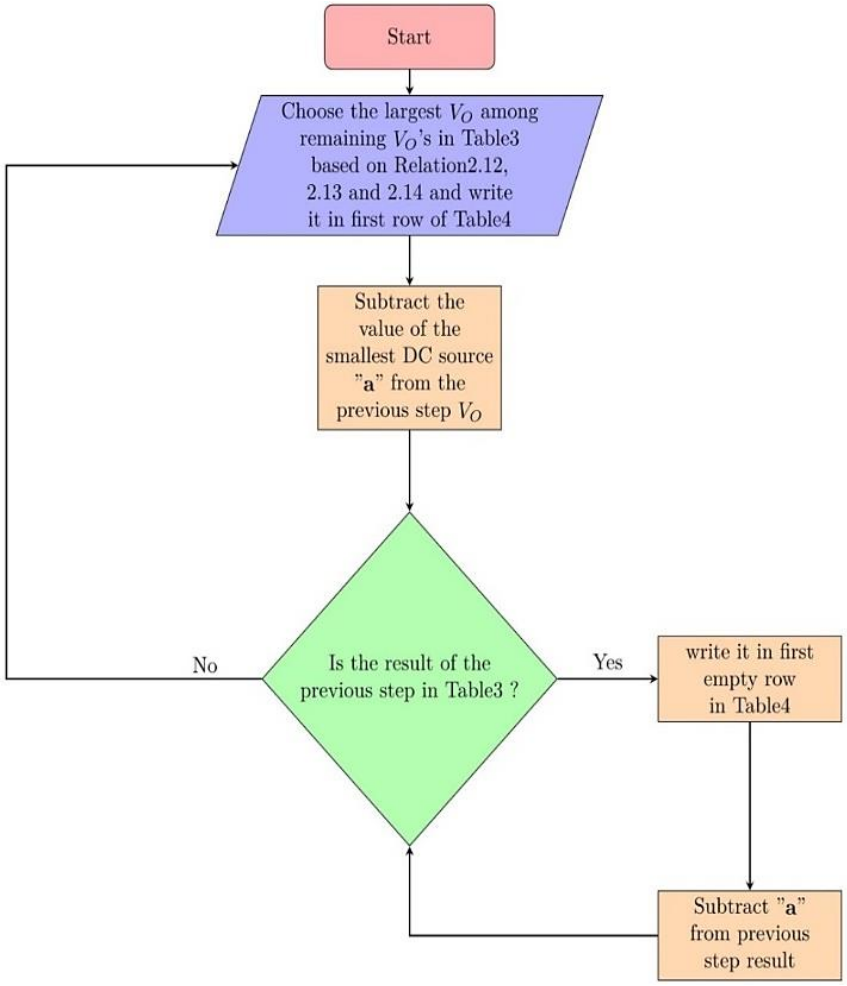

Figure 5. Proposed algorithm to sort the values of Table 4 from large to small

By determining the b, c, d coefficients, the ramaining V_os can be easily sorted. Due to the repetition of some levels, among the 98 positive voltage levels listed in Table 4, 80 levels are unique. These levels can also be created in negative polarity. Including the zero voltage level, a total of 161 voltage levels can be created by the circuit of Figure 3.

3. VALIDATION BY MATLAB PROGRAM

In this section, the MATLAB program is used to confirm the correctness of the obtained results. For this purpose, we wrote a MATLAB code, the flowchart of this code is presented in Figure 6, after entering the relations mentioned in Table 4 shows us for what values of b, c, and d as integer coefficients of a, the numbers obtained from them will have the same intervals and how many levels can be created. For this, we must assign a range to b, c, and d in the "for" loop. After running the program, the bar chart will be executed as shown in Figure 7. The red bars indicate that corresponding A, B, C, and D cannot form numbers with equal distances. The blue bars mean that corresponding A, B, C, and D can form numbers with equal distances, which is our preference. Corresponding A, B, C, and D are also shown the bars. After testing different amounts for B, C, and D by the MATLAB program, we concluded that the best amounts for b, c, and d are 3, 10, and 30 times a, respectively. In this case, we will have the largest number of levels (161 level for both positive (+) and negative (-) polarity and 0 (zero) level), while the distances between the levels are the same. This is the same result obtained from equations 15, 16, and 13.

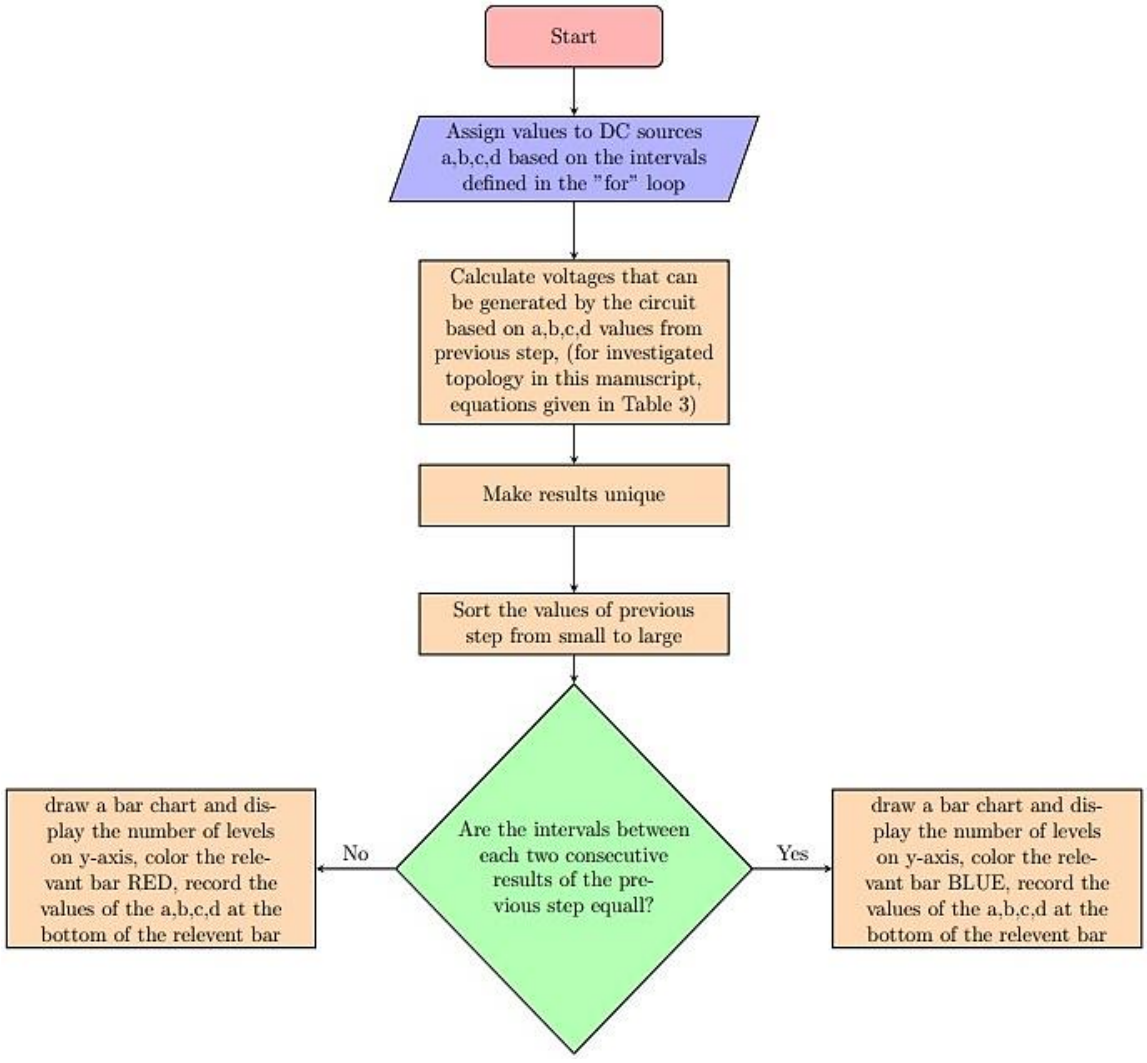

Figure 6. Proposed algorithm for MATLAB code

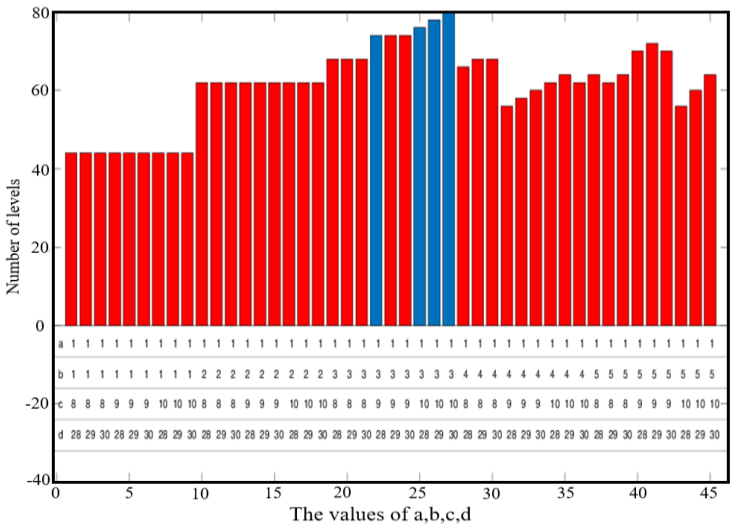

Figure 7. MATLAB code output

4. CONCLUSION

In this paper, a method for calculating the DC source amplitude in an extended multilevel converter structure was presented. This method consists of a basic module that can be expanded to generate additional voltage levels. In the past research, methods were introduced to calculate the DC source amplitude, but none of them provided a reason for presenting these methods. First, all possible states for creating voltage at the output were extracted. Then, according to the suggested algorithm, they were sorted from large values to small values. Finally, the amplitudes of the DC sources are calculated to generate the maximum number of equally spaced voltage levels, resulting in a lower THD and fewer parts. After we solved the problem through calculation and analysis, a code was written in MATLAB with the aim that this time the code will tell us for what values of DC sources we will have the largest number of levels, and as we expected, the output of the MATLAB code confirmed the correctness of the calculations. This MATLAB code can be used for any other topology in such a way that first, the voltages that can be generated in the output of the circuit are extracted parametrically and fed to the MATLAB code. This code tells us for what amounts of the amplitude of DC sources, the maximum number of levels can be created and whether the intervals between two consecutive levels are the same throughout the output waveform. In this study, we used iteration-based methods to find suitable values for DC sources. We did not obtain results from other methods except the iteration-based method; for example, using graph theory for circuit analysis did not give results. Therefore, in future studies, analytical methods can be used to find the best amounts for DC voltage sources. Additionally, presenting an application with the aim of finding the best amounts for DC sources after feeding a proposed topology to it would be an attractive topic.

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BIOGRAPHIES OF AUTHORS

Afzal Keivanlou Shahrestanaki was born in Sabzevar, Iran in May 1990. In 2013 he received his B.S. in Electrical Engineering from Birjand University. He is currently studying for a master's degree in Power Electronic and Electrical Machines at Hakim Sabzevari University. His current research interests include multilevel inverters, electric motor drives and solar inverter, maximum power point tracker, and battery chargers. He can be contacted at email: afzalkeivanlou@yahoo.com.

Rahim Ildarabadi was born in Sabzevar, Iran in 1975. He received the Ph.D. degree from Ferdowsi University of Mashhad in 2010. He is a full-time faculty member at Sabzevar, Hakim Sabzevari University. His main area of interests is automation system, electrical machine drive, renewable energy, instruments, and measurement. He is currently an assistant professor of Electrical Engineering at Hakim Sabzevari University. He can be contacted at email: rahim.ildarabadi@gmail.com.

Mahmoud Zadehbagheri was born in Yasouj, Iran, in October 1979. He received a B.S. degree in Electrical Engineering from Kashan University, in 2003, an M.S. degree in Electrical Engineering from Islamic Azad University, Najafabad Branch, in 2008, and the joint Ph.D. degree in Electrical Engineering from Universiti Teknologi Malaysia (UTM), Johor, Skudai, Malaysia, and Hakim Sabzvari University, Khorasan, Iran, in 2017. He is with the Department of the Electrical Engineering, Islamic Azad University, Yasouj Branch. He is currently collaborating as a reviewer and editorial board with the journals applied energy, hydrogen energy, IJRER, micro machines, sensors, energies, EPCS, IJPEDS. His research interests include the fields of power electronics, FACTS devices, optimization methods, renewable energy, energy hub, and power quality. He can be contacted at email: ma.zadehbagheri@iau.ac.ir.

Tole Sutikno is a lecturer in Department of Electrical Engineering at the Ahmad Dahlan (UAD) University, Yogyakarta, Indonesia. He received his B.Eng., M.Eng. and Ph.D. degrees in Electrical Engineering from Diponegoro University, Universitas Gadjah Mada and Universiti Teknologi Malaysia, in 1999, 2004, and 2016, respectively. Since July 2023, he has been a full professor at Universitas Ahmad Dahlan in Yogyakarta, Indonesia, after previously serving as an associate professor since June 2008. He is currently an editor-in-chief of the TELKOMNIKA since 2005, and the head of the Embedded Systems and Power Electronics Research Group since 2016. His research interests include the field of digital design, industrial applications, industrial electronics, industrial informatics, power electronics, motor drives, renewable energy, FPGA applications, embedded system, artificial intelligence, intelligent control, and digital library. He can be contacted at email: tole@te.uad.ac.id.