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High-efficiency rectifier achieves 63% power conversion in low start-up voltage for UHF RFID tags in 180 nm CMOS technology

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ABSTRACT

This paper presents an N-metal-oxide semiconductor (NMOS) rectifier designed for efficient radio frequency (RF) energy harvesting and wireless power transmission in passive ultra-high frequency (UHF) radio frequency identification (RFID) applications. The rectifier's efficiency is improved through an innovative diode with a new block connection, reducing the threshold voltage compared to conventional diode transistors. This enhancement significantly boosts output voltage and efficiency. A seven-stage configuration, based on the proposed diode and optimized via a superposition method, has been evaluated for its ability to increase DC output voltage and power conversion efficiency (PCE), particularly at low RF input power levels. Simulations show a PCE of 63% at 900 MHz with an RF input of -11 dBm, delivering 1.610 V across a 0.518 MΩ load. Notably, the rectifier maintains a PCE above 30% across a wide input power range from -32 dBm to -5 dBm, overcoming a key challenge of maintaining efficiency under low input power conditions. The circuit architecture was implemented using standard 180 nm TSMC CMOS technology, showcasing its practical applicability in RFID systems.

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1. INTRODUCTION

Recent technological advances in identification and communication play a crucial role in modern society. The ongoing development of these technologies has led to the emergence of new applications that play an essential role in knowledge sharing [1] and contribute greatly to economic growth by facilitating the exchange and dissemination of information. These technologies are used in a variety of areas, such as wireless sensor networks (WSNs) [2], internet of things (IoT) [3], biomedicine [4], industry [5], agriculture [6], distribution [5], logistics [5], traceability [3], health, and safety [4], bringing significant improvements to these sectors. One of the most popular technologies for these applications is radio frequency (RF) radio frequency identification (RFID), where an RFID system comprises two main components, the tag and the reader. For widespread adoption, RFID tags must be compact, affordable, and extremely low power.

RFID tags are classified into three main types according to their energy source: active, semi-active, and passive. Active and semi-passive tags are powered by an internal battery [7]-[9], while passive tags

obtain all the energy they need from the RF energy transmitted by the reader [10]. Longevity, low cost, and self-sufficiency are desirable features. However, the reliance of passive tags on transmitted RF energy complicates interface design [11], [12]. An essential part of an RF-powered wireless device is the RF-DC converter (rectifier) depicted in Figure 1, which primarily serves to convert incident RF energy into a stable DC voltage to power subsequent circuits [13]-[17].

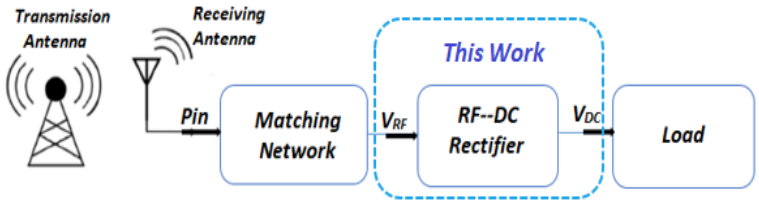

Figure 1. Diagram of the basic components of an RF energy harvesting system

Rectifiers are assessed based on their power conversion efficiency (PCE), a commonly used performance measure defined as in (1) [14], [18]-[20]:

$$PCE = \frac{P_{out}}{P_{in}} \quad (1)$$

Where P_{in} represents the average real input power accessible at the rectifier input, and P_{out} denotes the average output power generated at the rectifier output, as well as by the DC voltage they output, estimated using (2):

$$V_{out} = 2 * (V_{RF} - V_{th}) \quad (2)$$

Where V_{RF} is the voltage amplitude of the applied RF signal and V_{th} is the threshold voltage of the diode.

To efficiently generate higher amplitude output voltages as well as a large PCE, a multi-stage rectifier, such as a Dickson charge pump is often chosen. Although Schottky diodes are frequently used in this configuration due to their low threshold voltage (see Figure 2(a)), each diode contributes to a problematic voltage drop [21], [22]. In addition, the integration of these diodes into integrated technologies poses additional challenges and costs.

One way of reducing this drop is to use MOS transistors connected as diodes as illustrated in Figure 2(b) [23]. This method provides the flexibility to adjust diode dimensions to the specific needs of the application, overcoming the limitations of conventional diodes as such. Although the PCE of a circuit with a MOSFET is sometimes lower than that of a Schottky diode in view of a higher threshold voltage (V_{th}), the application of sophisticated Vth-cancellation techniques can significantly improve PCE. This paves the way for innovations to solve this considerable problem and maximize yields in applications requiring high output voltages [19].

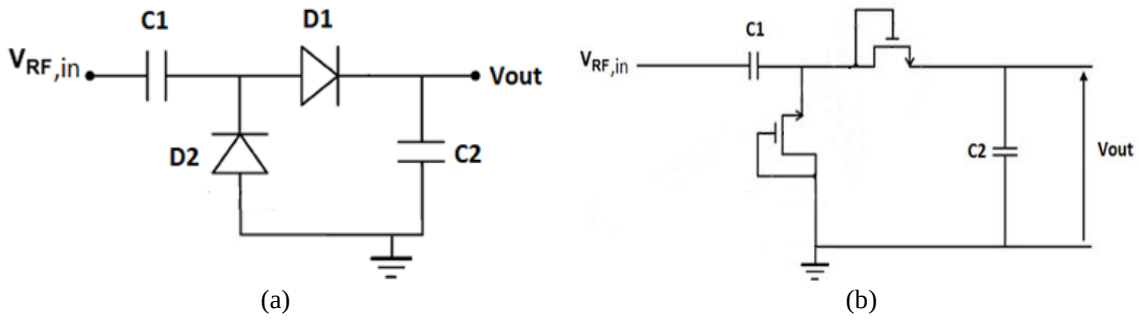

Figure 2. The conventional single-stage Dickson rectifier for: (a) Schottky diodes and (b) NMOS transistors connected as diodes

Several RF-DC converter architectures, incorporating various threshold voltage compensation techniques, were presented, contributing as such to improved energy efficiency for energy harvesting applications. A complementary metal-oxide semiconductor (CMOS) RF rectifier discussed in [24] employs a threshold voltage cancellation technique. This design utilizes positive feedback to reduce the threshold voltage of the transistors. However, a drawback of this approach is that energy efficiency fluctuates significantly with the input RF signal. The researcher introduced a 10-stage cross-connected rectifier utilizing the threshold voltage adjustment method [25]. The architecture detailed in [26] also suggests a threshold voltage cancellation approach appropriate for RF energy harvesting applications. A self-compensation method is described, where independent body biasing is applied to triple-well N-metal-oxide semiconductor (NMOS) transistors [27]. However, these transistors are not accessible in every CMOS technology [28], they are used as rectifier devices. Papotto *et al*. [29] presents a 17-stage rectifier with a self-adjusting configuration, capable of supplying 1.2 V to a 1 MΩ load. To maintain high system efficiency, [30] proposes a multipath energy harvesting architecture. The design of [31] unveils a cross-connected differential CMOS rectifier, with the goal of reducing leakage current and offsetting the threshold voltage of the rectifying component.

Previous research has mainly focused on optimizing PCE at specific input power levels, neglecting the crucial challenge of efficiently harvesting RF energy across a broad spectrum of low input powers. Some authors have favored multi-stage configurations, such as author in [29] with 17 stages and [25] with 10 stages. However, this approach led to an increase in rectifier size, generating high costs without exceeding a significant PCE threshold, e.g., 11% at -18 dBm in [29] and 42.4% at -16 dBm in [25]. Other researchers have adopted a logical number of stages, but the PCE peaks remain modest, not exceeding 47% at 1 dBm in [27], 25% at -5 dBm in [28], and 33% at -8 dBm in [31]. In all cases, energy efficiency varies rapidly in response to the RF input signal, limiting the range of low input powers to achieve high PCE.

To overcome these shortcomings, our study Introduces a novel RF-DC converter engineered specifically to enhance RF energy harvesting while sustaining high PCE over a broad range of low input powers. The converter configuration incorporates a seven-stage Dickson structure, featuring a threshold voltage cancellation technique suitable for energy harvesting applications. The performance of this RF-DC circuit surpasses that of existing solutions, representing a significant advance in the field as such.

The structure of this document follows a logical progression. Section 2 establishes the method for designing and optimizing a highly efficient NMOS rectifier, it examines in detail the impact of the threshold voltage V_{th} of NMOS transistors functioning as diodes on the efficiency of the PCE, this section also includes an analytical study of the (I-V) characteristic of the NMOS transistor for an in-depth understanding of its operation, the ultimate method is then determined to validate V_{th} cancellation, giving rise as such to a new highly efficient rectifier circuit. Section 3 is dedicated to discussion and analysis of the simulation results of the proposed circuit. Lastly, the conclusion is outlined in section 4.

2. METHOD TO DESIGN A HIGHLY EFFICIENT NMOS RECTIFIER

Before turning to this section, and given that rectifiers are evaluated according to their PCE, a preliminary examination of the impact of the NMOS transistor threshold voltage is crucial. This in-depth analysis is essential to understanding how these key characteristic influences power conversion and, consequently, the device's energy efficiency.

2.1. Impact of NMOS transistor threshold voltage on rectifier power conversion efficiency

Since the conversion, PCE is characterized as the ratio of output power P_{out} to input power P_{in} [32], [33], we can write:

$$PCE = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (3)$$

where P_{out}, P_{in}, and P_{loss} are DC output power, RF input power and rectifier power loss respectively [19].

The input power Pin is equivalent to the total of the output power P_{out} and P_{Diode} [34], which designates the power loss in the MOS transistors connected as diodes, so:

$$P_{loss} = N * P_{Diode} \quad (4)$$

where N represents the number of rectifier stages, hence:

$$PCE = \frac{P_{out}}{P_{out} + N.P_{Diode}} \quad (5)$$

and according to the diode characteristic (I-V) illustrated in Figure 3, the current flows solely when the applied voltage attains V_{th} and the time-averaged current corresponds to the rectifier current V_R [13].

$$P_{Diode} = \frac{1}{T}\int_{t_0}^{t_2} v_D(t).i_D(t)dt = V_{th}.\frac{1}{T}\int_{t_0}^{t_2} i_D(t)\,d(t)dt \quad (6)$$

then

$$P_{Diode} = V_{th}.I_{out} \quad (7)$$

Where I_{out} is the output current.
Knowing that P_{out} is expressed as (8):

$$P_{out} = V_{out}.I_{out} \quad (8)$$

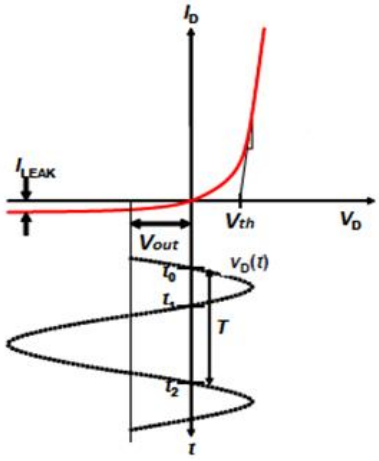

Figure 3. (I-V) characteristics of an MOS transistor utilized as a diode, accompanied by the representation of the RF voltage waveform applied [32]

In addition, since: V_{out}=N.V_R N is the count of transistors employed as diodes, and from (2) we can infer:

$$V_{out} = 2N\left(V_{rf} - V_{th}\right) \quad (9)$$

hence

$$P_{out} = 2N\left(V_{rf} - V_{th}\right).I_{out} \quad (10)$$

Therefore, from (5), (7), and (10) we obtain (11):

$$PCE = \frac{2(V_{rf}-V_{th})}{2(V_{rf}-V_{th})+V_{th}} = \frac{2V_R}{2V_R+V_{th}} \quad (11)$$

where V_R, V_{th}, and V_{rf} are the rectifier output DC voltage, the transistor diode threshold voltage and the peak voltage magnitude of the input RF signal, respectively [24], [25].

So once again, we conclude that a low V_{th} is essential to get a high PCE from a rectifier. To achieve this, we need to design a rectifier which must have a new NMOS transistor connected as a diode and which meets this requirement (V_{th}→0).

2.2. Conventional NMOS transistor connected as a diode: unveiling its weaknesses

To design a rectifier that meets the requirement deduced in the previous section (V_{th} tends to 0), it is crucial to analyze the structure and characteristics of the NMOS transistor deployed in the rectifier, as illustrated in Figure 4(a) [26], [27]. Derived from the (I-V) characteristics of the transistor depicted in

Figure 4(b), the voltage versus current curve is segmented into four regions: the front region, the subthreshold region, the inverse region, and the breakdown region.

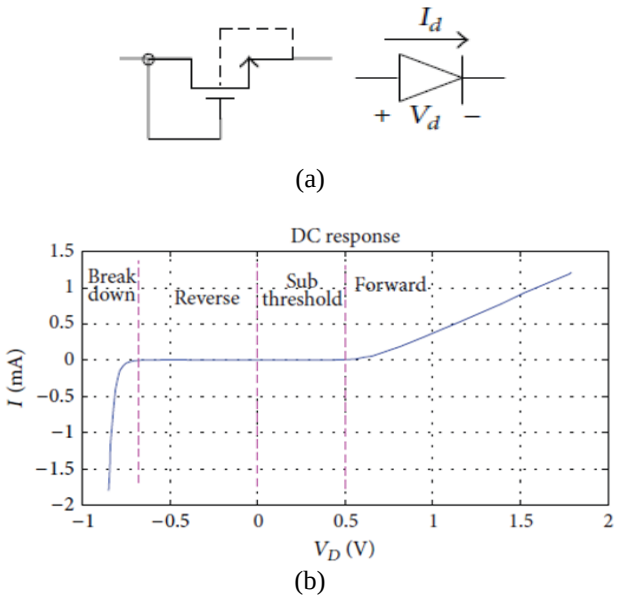

Figure 4. The NMOS transistor connected as a diode for: (a) the conventional configuration and (b) the (I–V) characteristic of the transistor [35], [36]

In a standard MOS transistor, when the source is not tied to ground, a phenomenon called the body effect may change the threshold voltage as shown by (12) [28], [29]:

$$V_{th} = V_{th0} + K_1\left(\sqrt{\varphi_S + V_{SB}} - \sqrt{\varphi_S}\right) + K_2 V_{SB} \quad (12)$$

Where parameters K_1 and K_2 are influenced by the channel doping, V_{th} represents the transistor's threshold voltage, V_{th0} is the intrinsic threshold voltage of the transistor, V_{SB} is the voltage between the transistor's source and ground, and ϕs is dependent on CMOS technology.

In (12) illustrates that when the voltage V_{SB} between the source and ground of a MOS transistor is positive, the threshold voltage increases, giving rise to the undesirable phenomenon of body effect. Conversely, when V_{SB} is negative, the threshold voltage decreases. This indicates that applying a fixed negative voltage between the source and ground could potentially alleviate this effect [27], [30].

However, as indicated by (13) and (14) from [37]-[39], applying a negative voltage between the source and ground results in an increase in the transistor's leakage current. Consequently, this type of transistor, when connected as a diode, may perform well in the forward and subthreshold regions, but it exhibits significant leakage current in the reverse region. This is an undesirable effect in rectifier design, compromising its overall efficiency [27], [28].

$$I_{Reverse} = I_{Leakage} = I_{SO} \cdot \left(\frac{W}{L}\right) \cdot \left(1 - e^{\frac{-V_D}{V_T}}\right) \cdot (1 + \lambda_{sub} V_D) \quad (13)$$

$$I_{SO} = \sqrt{\frac{q\varepsilon_{si} N_{ch}}{2\varphi_S}} \cdot V_T{}^2 \cdot e^{\frac{(-V_{th} - V_{off})}{nV_T}} \quad (14)$$

After this analysis, which highlights the various weak points of conventional transistors connected as diodes, it becomes clear that the threshold voltage (V_{th}) reduction requirement for a high-performance rectifier is also linked to other criteria associated with the forward current and leakage current of the transistor in question. In conclusion, a diode suitable for MOS rectifier design must have substantial forward current at low threshold voltages, higher subthreshold current in the subthreshold region, while maintaining very low reverse leakage current [27], [31], [39].

2.3. Proposed NMOS transistor connected as a diode

To meet the criteria set out in the previous section, we present a new NMOS transistor connected as a diode. This is an NMOS transistor with a special connection (bulk-drain connection) where ground is connected to drain. See Figures 5(a) and (b) for further details [27], [30].

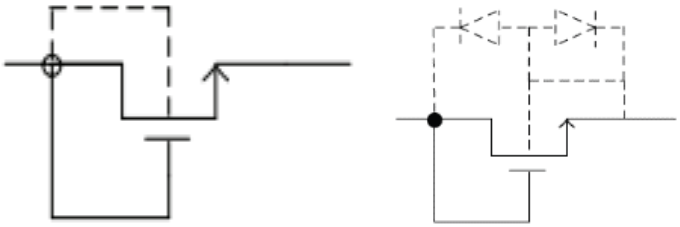

Figure 5. The proposed NMOS transistor connected as a diode for: (a) the transistor configuration and (b) the intrinsic PN junctions of the NMOS transistor [36], [39]

When the suggested diode is operated in direct mode, the voltage between source and transistor ground becomes negative, as such causing a decrease in the transistor's threshold voltage and an increase in the diode's DC current compared to conventional NMOS transistors connected as a diode [27], [29]. Conversely, when the suggested diode is reverse-biased, the voltage between the transistor source and ground becomes positive, as such reducing the reverse diode current. More detailed theoretical explanations of the operation of the proposed circuit can be found in [36], [38], [40].

This particular configuration has a dual impact on rectifier operation, generating an increase in forward mode current and a decrease in reverse mode current. These modifications contribute significantly to improving the performance of the NMOS transistor used as a diode in a rectifier circuit. The verification of this demonstration, carried out in [19], [34], [40], was supported by a comparative analysis between the outcomes of the simulation of the conventional rectifier circuit and those of the proposed new rectifier circuit. The conclusions of this comparison will be presented in the next section. Figure 6 illustrates the new single-stage rectifier utilizing the suggested diode rather than the traditional diode.

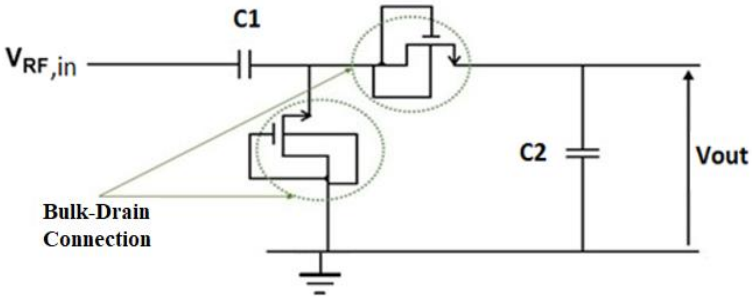

Figure 6. Single-stage rectifier using NMOS transistors connected as proposed diodes

As we know, to further optimize rectifier performance, efficiently producing output voltages with greater amplitude and better energy efficiency, we often opt for a multi-stage rectifier, but this time it will be the new topology proposed, see Figure 7. Although efficiency improves with additional stages, leading to higher DC output voltage and PCE performance, it eventually peaks before declining. This decline is attributed to the increasing number of transistors, leading to losses associated with leakage current and threshold voltage. To determine the optimum number of stages for high efficiency, we carried out simulations with different stage configurations. Our aim was to determine the ideal number of stages that maximizes PCE.

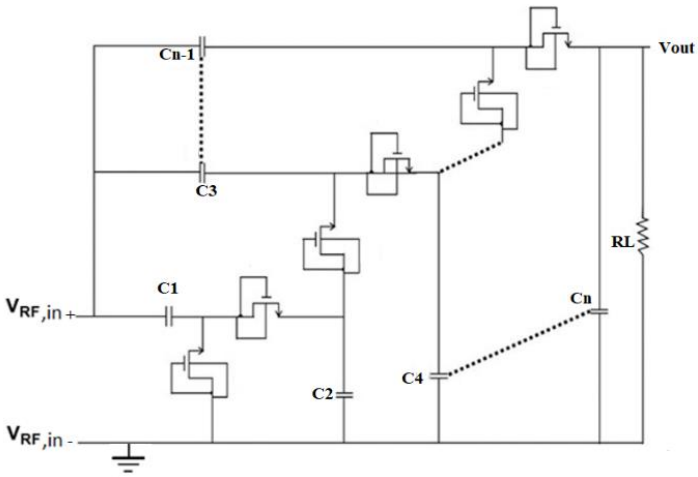

Figure 7. Dickson N-stage rectifier with proposed topology

3. FINDINGS AND ANALYSIS

To assess our rectifier circuit, we carried out three types of simulations. First, we compared the output voltage versus time of two single-stage NMOS rectifiers, one using our proposed topology and the other a conventional topology. Next, we analyzed the PCE for multi-stage configurations to find the ideal number of stages. Finally, we verified the circuit's correct operation by simulating output voltage relative to RF input power for four distinct configurations, with and without our topology. The results will be presented with a concise analysis and compared with existing literature. Simulations were performed with ADS software, using TSMC 0.18 µm RF CMOS technology, at a frequency of 900 MHz.

3.1. Simulation results: output voltage vs time for single-stage NMOS rectifier

Figure 8 illustrates the transient output voltage of two single-stage NMOS rectifiers. One incorporates the proposed NMOS transistor (circuit shown in Figure 6), while the other uses the conventional NMOS transistor acting as a diode (circuit shown in Figure 2(b)). As Figure 8 clearly demonstrates, a significant improvement in output voltage is observed. The outcomes of this simulation validate that the use of the suggested NMOS transistor in conventional rectifiers leads to a significant improvement in output performance. This is attributed to the improvements in the diode's front and rear (I-V) characteristics, resulting from the suggested bulk-drain connection.

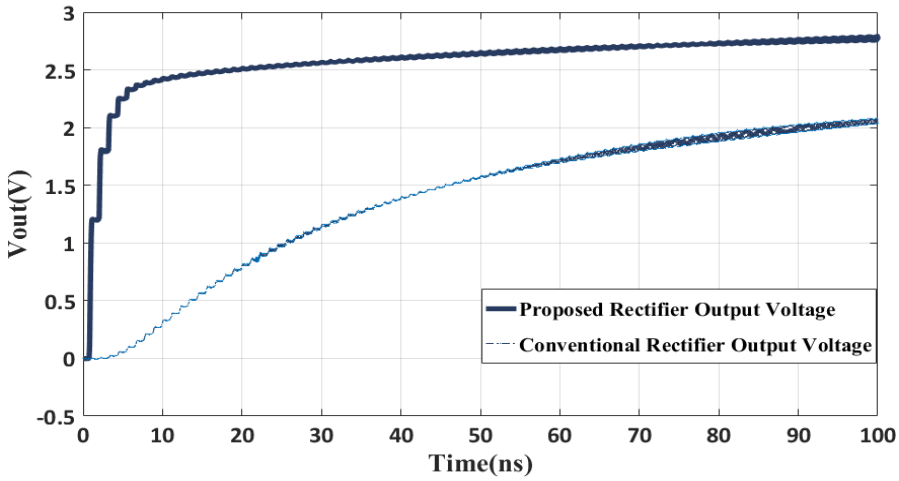

Figure 8. Output voltage versus time for a single-stage NMOS rectifier using the proposed diode NMOS and conventional NMOS

3.2. Simulation: PCE vs input power for seven-stage Dickson rectifier with proposed topology

Through a series of simulations involving rectifier circuit configurations ranging from one to eight stages, incorporating of course the proposed new topology, we identified that the optimum PCE was achieved with a circuit consisting of seven stages, as illustrated in Figure 9. Beyond seven stages, we observed a degradation in PCE. Figure 10 shows the simulation results for different rectifier circuits, ranging from three to eight stages. This illustration highlights a significant degradation of the PCE above seven stages, confirming as such that the choice of seven stages is optimal, see Figure 11. It is important to note that simulations of single-stage and two-stage circuits showed relatively low efficiencies, which is why they are not shown in the Figure 10.

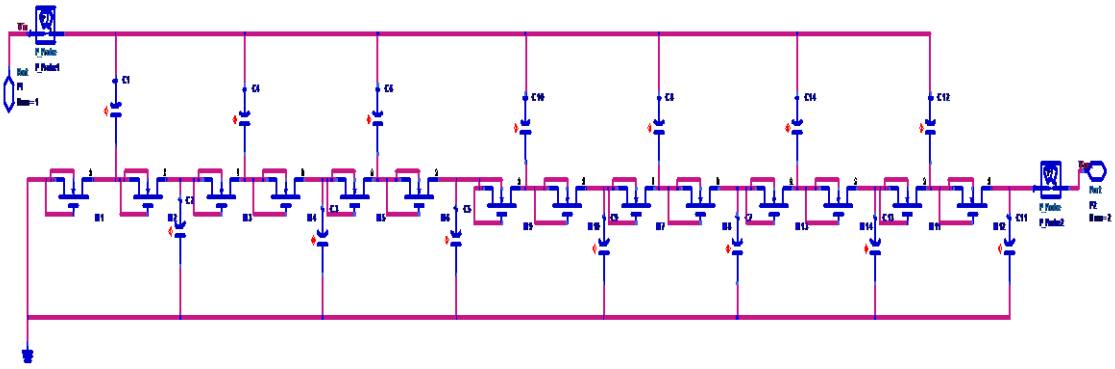

Figure 9. Dickson 7-stage rectifier with proposed topology

Figure 11 shows a clear improvement in the power-to-efficiency ratio PCE for the suggested rectifier configuration, reaching a maximum efficiency of 63% with an input power level of -11 dBm. However, above this value, efficiency decreases proportionally with increasing RF input power. In addition, a slow progression of the PCE versus input power (Pin) curve is observed, maintaining a significant PCE of over 30% over a wide range of low input powers, from -32 dBm to -5 dBm. This presents a significant advantage compared to previous research results, where rectifier circuits were hindered by rapid variations in energy efficiency contingent upon the input RF signal, restricting the range of low input power for achieving high PCE.

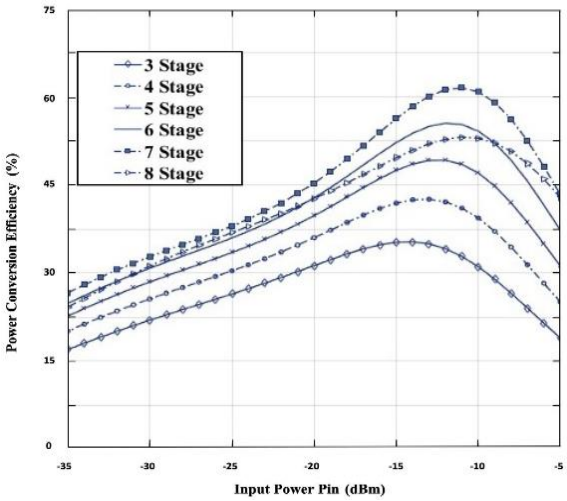

Figure 10. PCE of multistage Dickson rectifier with proposed topology vs RF input power

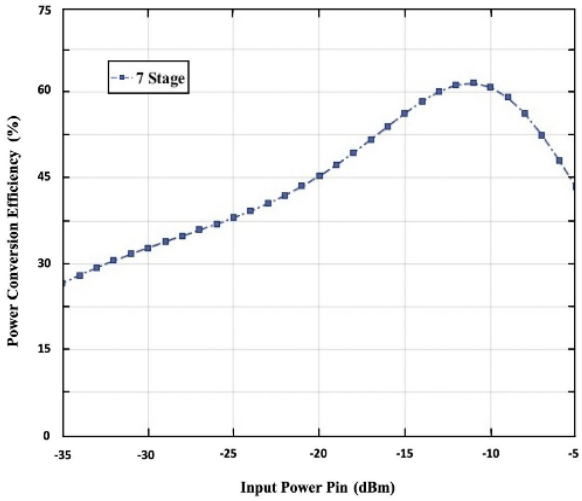

Figure 11. PCE vs input power of a seven-stage Dickson rectifier

3.3. Simulation results: VDC output voltage relative to RF input power for four rectifier configurations with and without the proposed topology

Figure 12 shows the variation of output voltage V_{DC} versus RF input power (Pin) for four various configurations. The conventional single-stage and seven-stage topology, as well as the suggested single-stage and seven-stage topology. The underlying aim of this analysis is to validate that the adoption of seven stages for the Dickson rectifier charge pump, combined with the bulk-drain connection recommended in each NMOS transistor-connected as diode making up this configuration, represents the optimum solution for enhancing circuit performance.

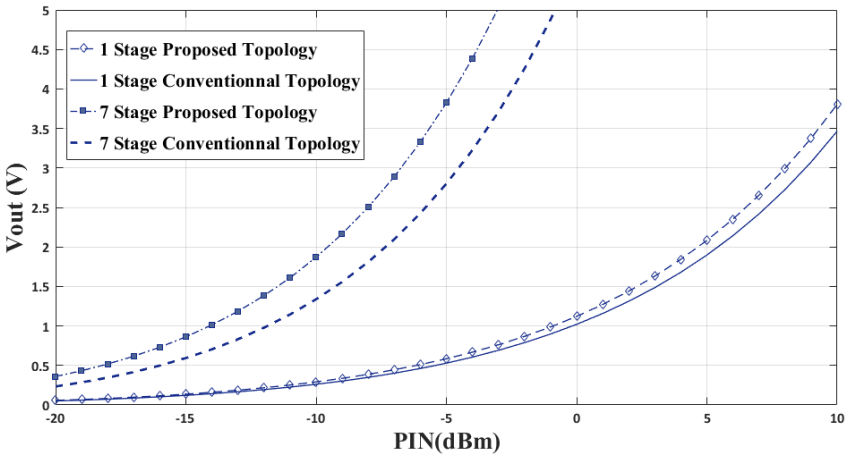

Figure 12. Output voltage of one stage and seven stage configurations with and without proposed diode, versus RF input power

While the output voltage (Vout) of the four simulated configurations increases with Pin, its value varies based on the stage count and topology. For both single-stage conventional and proposed topologies, there's no significant difference in Vout at low input power levels (-20 dBm to -5 dBm). However, a disparity arises at higher input power (Pin> -5 dBm), where the topology with bulk-drain connection yields higher Vout than the conventional one. For instance, at Pin=-11 dBm, the conventional topology outputs 0.226 V, while the proposed one outputs 0.252 V, albeit this difference isn't substantial. Unlike the two seven-stage topologies, where Vout distinction persists even at low Pin levels (Pin<-5 dBm), this difference grows with Pin increase. For example, at PCE peak (Pin=-11 dBm), the conventional seven-stage outputs 1.146 V, while the proposed seven-stage outputs 1.610 V.

The dual design of the proposed rectifier maintains exceptional features, yielding a beneficial DC output voltage of 3.823 V at low input power (-5 dBm), achieved by effectively reducing the threshold voltage V_{th} of NMOS transistors. These results are detailed in Table 1. It should be noted that a drawback arises due to the high performance of this proposed rectifier circuit: at short distances separating the reader and the tag, the received power can be very high and may lead to the failure of transistors or components in the circuit. Hence, it is essential to utilize a voltage limiter to reduce the voltage to an acceptable level for the process.

Table 1. Calculated efficiency of the rectifieroptimized configuration

Input power (dBm)	Input power (mWatt)	Vout (V)	PCE (%)
-20	0.01	0.360	45
-15	0.0316	0.862	54
-11	0.0794	1.610	63(peak)
-5	0.3162	3.823	42

3.4. Performance summary

Table 2 summarizes the performance of the innovative circuit, outperforming most reference works. It demonstrates the circuit's remarkable efficiency, with a peak PCE of 63% at -11 dBm and a significantly improved output voltage. PCE remains above 30% across a broad spectrum of low input powers levels, resolving the major challenge of efficiency over a diverse range of low input power levels.

Table 2. Performance summary and comparative analysis by previous work report

Publication	2014 [34]	2019 [17]	2019 [27]	2021 [12]	2022 [25]	2022 [13]	This work
Technology	90 nm	65 nm	180 nm	65 nm	130 nm	180 nm	180 nm
Frequency	868 MHz	2.45 GHz	0.902 GHz	2.45 GHz	915 MHz	1.05 GHz	900 MHz
Topology	Differential cross-coupled	Differential Cross-coupled		Cross-coupled	Cross-coupled	Cross-connected	Dickson multi_stage
Numbre of stages N	5	1	-	1	10	3	7
RLoad @peak PCE	0.33 MΩ	--	-	--	0.45 MΩ	470 KΩ	0.518 MΩ
Pin (dBm)	−17 dBm	−22.7 dBm	1.6	−14.1 dBm	-16 dBm	−10 dBm	−11 dBm
and Vout(V)	--	0.4V		0.4 V		1V	1.610V
Peak PCE	40%	48.3%	47%	32.3%	42.4%	45%	63%

4. CONCLUSION

This study presents the design of an optimized NMOS rectifier dedicated to RF energy harvesting. The proposal of a highly efficient V_{th} voltage compensation technique is based on the utilizing an NMOS transistor as a diode, with a bulk-drain connection. This approach improves the transistor's characteristics by reducing the V_{th} threshold voltage, decreasing the leakage current and increasing the forward current, in addition, evaluation of a configuration based on a 7-stage Dickson charge pump, incorporating the proposed diode, revealed considerably improved performance, as such leading to a significant increase in PCE across a broad spectrum of low input powers.

Using standard 180 nm TSMC RF CMOS technology, this configuration achieved a remarkable PCE of 63% at 900 MHz with an RF input power of -11 dBm while delivering 1.610 V at an output load of 0.518 MΩ. In addition, over 30% PCE was measured over an input power range from -32 dBm to -5 dBm. At -5 dBm, the notable output voltage of 3.823 V was produced. Overall, a wide range of high PCEs was observed, underlining the outstanding performance of this rectifier in Low Star-tup Voltage for UHF RFID applications.

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