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A counter-centric binary-to-binary coded decimal and multiplexed seven-segment driver on an Artix-7 FPGA

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ABSTRACT

This paper presents a complete field-programmable gate array (FPGA) implementation for showing a 4-bit binary value (0–15) as a two-digit decimal number on the Nexys-4 double data rate (DDR) seven-segment display. The design comprises: (i) a compact binary-to-binary-coded decimal (BCD) converter tailored to the 0–15 range; (ii) a seven-segment decoder for active-low, common-anode digits; and (iii) a counter-based clock-enable controller that time-multiplexes the digits at a rate chosen to be flicker-free yet energy-efficient. A simple timing model links the divider width N, the number of digits N_D, and the refresh rate $f_{\text{frame}} = f_{\text{clk}}/(N_D 2^N)$. Simulation verified hazard-free switching and one-hot anode selection; hardware tests on the Nexys-4 DDR (100 MHz clock) confirmed the analysis. Selecting $N = 18$ yields $t_{\text{dwell}} = 2.62144$ ms and $f_{\text{frame}} \approx 190.7$ Hz, which removes ghosting while avoiding unnecessary high-frequency scanning. The system displays all inputs correctly and provides a clear sizing rule for wider inputs and more digits. The approach is fully synthesizable, resource-light, and portable to larger word-lengths and displays.

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1. INTRODUCTION

Seven-segment displays remain a widely used and practical method for presenting numerical information in digital systems, owing to their low cost, simplicity, and clear visual output [1], [2]. Although such displays operate in decimal form, digital hardware represents values in binary. Bridging this difference requires conversion logic that reliably maps binary inputs to human-readable digits. Field programmable gate array (FPGA) development boards, including the Nexys-4 double data rate (DDR) used in this work, provide multi-digit seven-segment displays in which all digits share the same segment lines [3], [4]. Because of this shared-bus structure, only one digit can be driven at a time, and the system must scan the digits one after another. When the scanning is fast enough, above the human flicker threshold, the display appears steady [5], [6].

This paper presents the complete design and implementation of a system that converts a 4-bit binary input (0–15) into two decimal digits and displays them on the Nexys-4 DDR seven-segment interface. Two technical challenges are addressed. The first is the accurate conversion of the binary input into its tens and units digits, which requires compact and efficient logic suitable for FPGA implementation [7], [8]. The second is the design of a scanning mechanism that activates each digit in turn at a rate that avoids visible flicker while

minimising power consumption. If the refresh rate is too fast, unnecessary switching increases dynamic power; if too slow, flicker or ghosting becomes visible [9], [10].

To meet these goals, the system uses a clock-enable pulse derived from the 100 MHz system clock, allowing precise control over the scanning rate without gating or dividing the main clock. This approach follows recommended FPGA timing practices, avoiding skew and timing uncertainty while keeping the logic synchronous [11], [12]. The use of a tunable enable pulse also makes it possible to study refresh-rate behaviour analytically and experimentally, enabling the optimal balance between power reduction and visual smoothness [13], [14].

The key contributions of this work are summarised as follows:

- Counter-centric multiplexing architecture: a novel approach to display multiplexing that operates at the minimum refresh rate necessary to eliminate visual flicker (≈100-120 Hz) [8], [13], significantly reducing power consumption compared to conventional high-frequency scanning methods [14] while maintaining display quality and brightness uniformity.
- Optimised binary-to- binary-coded decimal (BCD) conversion: an efficient conversion algorithm specifically tailored for the 0-15 input range, utilising Boolean minimisation techniques and K-map optimisation [15] to achieve minimal logic resource utilisation while ensuring accurate tens and units digit separation [16].

The rest of the paper is organised as: section 2 reviews related work on seven-segment driving, binary-to-decimal conversion, and display scanning. Section 3 explains the architecture and design choices. Section 4 reports simulation and hardware results. Section 5 concludes and outlines extensions.

2. RELATED WORK

Research on efficient seven-segment display control and binary-to-BCD conversion connects foundational logic design with perceptual requirements and power optimisation for FPGA platforms. The literature is divided into several relevant domains:

Classic logic minimisation techniques have long been central to segment-level decoder design. Canonical methods such as Karnaugh maps [17], Quine–McCluskey algebraic reduction [18], and heuristic approaches like the Espresso algorithm [19] allow for the creation of compact, hazard-free Boolean expressions. These techniques remain valuable for developing segment decoders implemented on FPGA look-up table (LUT) fabrics, promoting resource efficiency, especially in instructional and low-complexity applications [20].

For binary-to-BCD conversion, small-scale ranges like 0–15 typically rely on direct truth-table encoding or simple combinational adder networks, which are practical for simple displays [21]. However, for broader ranges or scalable systems, the shift-and-add-3 "double-dabble" algorithm is preferable for its iterative, linear scaling properties [22]. Area and latency trade-offs between combinational, iterative, and hybrid conversion circuits inform the selection of architectures for FPGA teaching boards, where reuse and modularity are valued [23].

In the context of multi-digit display driving, the shared-segment architecture of modern teaching FPGAs necessitates time-division multiplexing, as only one digit can be illuminated at a time [4]. Psychophysical studies set the typical flicker-fusion threshold at approximately 60 Hz [24]; thus, engineering rebuttals aim for refresh rates above 100 Hz per digit to ensure the display appears uniformly bright and stable across all viewing conditions [25]. Notably, since dynamic power consumption in CMOS circuits is directly proportional to switching activity ($P \propto fCV^2$) [26], [27], academic and industrial guidelines advocate the use of clock-enable signals, derived from the master system clock, to control multiplexing rate, thus minimising unnecessary transitions and maintaining optimal FPGA timing integrity [28], [29].

Finally, practical implementations must adhere to hardware standards and board documentation, such as the IEEE Std 1164 logic types [30] and official platform reference manuals [31]. These dictate segment polarity, input/output (I/O) standards, and pin mappings, directly shaping truth-table derivations and the functional correctness of display controllers [32]. Collectively, these works establish the foundational principles and constraints that motivate this paper's proposed architecture: a combination of a compact binary-to-BCD converter, optimally minimised decoder logic, and a power-conscious, clock-enable-based multiplexing strategy.

3. DESIGN AND IMPLEMENTATION

This section describes the end-to-end design that converts a 4-bit binary input into two decimal digits and displays them on the Nexys-4 DDR seven-segment interface. The overall structure is shown in Figure 1. The datapath consists of three functional blocks: (i) a binary-to-BCD stage that produces "tens" and "units"; (ii) a seven-segment encoder that converts each decimal digit into segment patterns; and (iii) a scanning

controller that selects one display digit at a time. All logic is synchronous to the 100 MHz system clock, and the scan is advanced by a short enable pulse; the main clock is never gated.

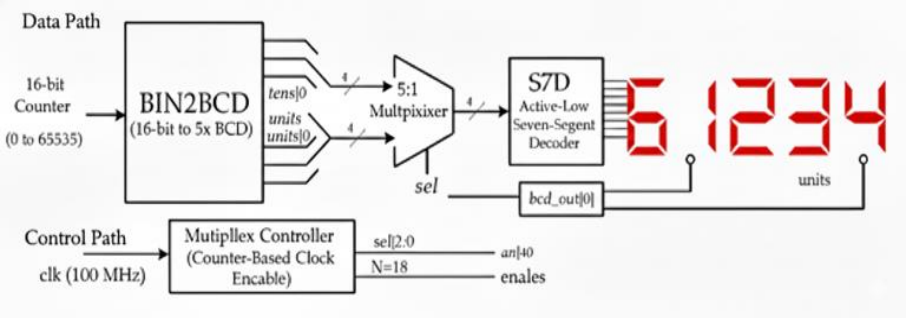

Figure 1. System architecture block diagram

3.1. System model and signals

The input is a 4-bit number $x \in [0,15]$ captured from slide switches. The binary-to-BCD stage outputs two 4-bit nibbles BCD_{tens} and BCD_{units}. A small selector chooses which nibble feeds the seven-segment encoder. The encoder drives the shared segment bus $seg[6:0]$ (a–g). Because the Nexys-4 DDR uses common-anode displays, the segments are active-low (logic '0' turns a light-emitting diode (LED) on) and each digit is enabled by an active-low anode line. Only one anode is asserted at a time, so only one digit is lit at any instant. The scan controller rotates the active anode and presents the matching segment pattern in step with it.

The complete data and control paths are summarised in Figure 1. The BIN2BCD module yields five BCD nibbles from a 16-bit input; a 5:1 multiplexer forwards the selected nibble to the S7D decoder while the multiplex controller advances the active-low anode enable and maintains a fixed dwell per digit with a counter-derived clock-enable.

3.2. Binary-to-BCD conversion

For the 4-bit case the conversion is simple and exact. The "tens" digit is either '0' or '1':

$$d_{10} = \begin{cases} 0, & x \le 9, \\ 1, & x \ge 10, \end{cases} d_1 = x - 10 \cdot d_{10} \quad (1)$$

This avoids a general divider and keeps logic usage low. The output nibbles BCD_{tens} and BCD_{units} are then passed to the encoder. The encoder implements the standard 0–9 segment patterns in active-low form; Table 1 lists the truth table for digits 0–9 (rows a–g, where '0' means "LED on"). This table is the basis for the Boolean minimisation used in the register-transfer level (RTL).

Table 1. Units digit: active-low segment truth table (0 = ON, 1 = OFF)

BCD	a	b	c	d	e	f	g
0	0	0	0	0	0	0	1
1	1	0	0	1	1	1	1
2	0	0	1	0	0	1	0
3	0	0	0	0	1	1	0
4	1	0	0	1	1	0	0
5	0	1	0	0	1	0	0
6	0	1	0	0	0	0	0
7	0	0	0	1	1	1	1
8	0	0	0	0	0	0	0
9	0	0	0	0	1	0	0

3.3. Seven-segment encoding

Each BCD nibble is mapped to $seg[6:0]$ by compact Boolean expressions obtained from the truth table. The encoder outputs are registered, so the segment bus changes only on a clock edge. Registering the outputs ensures that segment values remain constant while a digit is enabled, which removes visible "ghosting" when the scan advances to the next digit.

3.4. Scan controller and timing model

The scan is advanced by a clock-enable pulse produced by a binary counter of width N. If T_{clk} is the 100 MHz clock period, then the enable pulse repeats every;

$$t_{\text{dwell}} = 2^N T_{\text{clk}} \tag{2}$$

with N_D display digits, one full frame takes,

$$t_{\text{frame}} = N_D\, t_{\text{dwell}}, f_{\text{frame}} = \frac{1}{t_{\text{frame}}} = \frac{f_{\text{clk}}}{N_D\, 2^N} \tag{3}$$

where N_D is the number of scanned digits. The dominant switching arises from (i) segment updates when the currently displayed digit changes, and (ii) the active-low, one-hot anode lines. Let H_{frame} denote the total Hamming distance between consecutive seven-segment patterns over one full frame (content-dependent). A relative dynamic power index is defined as:

$$\text{PI} = w_{\text{seg}}\, f_{\text{frame}}\, H_{\text{frame}} \;+\; w_{\text{an}}\, (2N_D)\, f_{\text{frame}} \tag{4}$$

with non-negative weights $w_{\text{seg}}, w_{\text{an}}$ used to aggregate the two contributions. The index is unitless and intended for comparative assessment across (N, N_D) and typical digit contents. Choosing N to keep f_{frame}in the $\sim$ 100–200 Hz band reduces switching while maintaining a steady display.

3.5. Parameterisation and scalability

The design is parameterised by the number of input bits N_B and the number of digits N_D. In general,

$$N_D = \lceil \log_{10}(2^{N_B}) \rceil = \lceil N_B \cdot \log_{10} 2 \rceil \tag{5}$$

For wider inputs (e.g., 8, 12, or 16 bits), a small iterative binary-to-BCD core can be used, while the selector, encoder and scanning logic remain unchanged. The same timing model applies: choose N to place f_{frame} in the ~100–200 Hz band for flicker-free presentation with low switching activity. A brief sizing table for N versus N_D is provided with the results.

3.6. Implementation details

Pin assignments map the three switches to the input bits and the shared segment lines to seg[6: 0]. The anode vector is wired to the first two digits of the eight-digit module on the Nexys-4 DDR. All outputs that drive the display (segments and anodes) are registered. The constraints file sets the 100 MHz clock and I/O standards.

3.7. Verification plan

Unit tests: exhaustively stimulate the binary-to-BCD converter (0–15) and the BCD → seven-segment encoders (0–9), checking against Table 1 (active-low). Integration sim: run the multiplex FSM with a shortened divider and confirm enable-synchronised updates and opposite anode drive. On-board: program the device, sweep inputs, and capture photos. Tune N if needed to remove ghosting while keeping $f_{\text{digit}} \geq 100$ Hz.

4. RESULTS AND DISCUSSION

A staged verification flow was used: unit-level simulation of the clock-divider, multiplexer and seven-segment decoder; integrated simulation of the whole display path; and finally on-board tests on the Nexys-4 DDR. The consolidated timing diagram in Figure 2 shows the key internal signals (a small divider value was used in simulation purely for visibility). Clock-enable pulses occur every $2^N T_{\text{clk}}$; on each pulse the digit index sel_idx increments by one, the active-low anodes present a one-hot selection for the addressed digit, and the registered segment bus remains constant throughout each dwell. Two points are evident: (i) there are no hazards or intermediate glitches at selection boundaries, confirming that the segment data only update synchronously on the clock-enable edge; and (ii) non-selected anodes remain de-asserted for the full dwell, removing the conditions that typically produce “ghosting”.

With $f_{\text{clk}} = 100$ MHz and the implementation setting $N = 18$, the measured dwell and frame timings match the analytical model:

$$t_{\text{dwell}} = 2^N T_{\text{clk}} = 2.62144\ \text{ms}, t_{\text{frame}} = N_D\, t_{\text{dwell}} = 5.24288\ \text{ms}\ (N_D = 2),$$

During early trials a faint after-image on the inactive digit indicated an overly high multiplex rate, the next digit was enabled before the previous drivers had fully released. Guided by the timing model $t_{\text{dwell}} = 2^N T_{\text{clk}}$, $t_{\text{frame}} = N_D\, t_{\text{dwell}}$, $f_{\text{frame}} = 1/t_{\text{frame}}$, we swept the divider width N around the perceptual limit. A low-power target of ≈ 100 Hz suggests $N \approx \log_2(5\text{ ms}/10\text{ ns}) \approx 18.93$ (i.e., $N = 19$). Empirically, values near 19 still showed trace ghosting on our board revision; $N = 18$ gave $t_{\text{dwell}} = 2.62144$ ms, $t_{\text{frame}} = 5.24288$ ms and $f_{\text{frame}} \approx 190.7$ Hz (about 95 Hz effective per digit), which removed the artefact while remaining comfortably flicker-free.

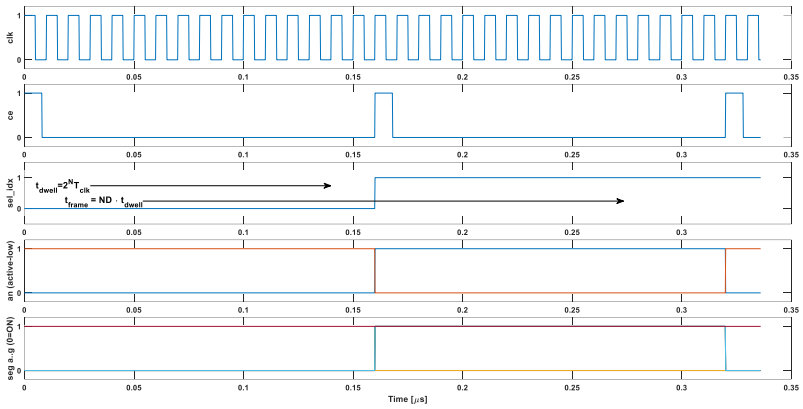

Figure 2. Timing diagram of the clock-enable driven multiplexing

To quantify the refresh–power trade-off, Figure 3 plots a relative dynamic-power index against the divider N for $N_D \in \{2,3,4,5\}$ at $f_{clk} = 100$ MHz. The index is proportional to the number of segments and anode transitions per second; hence, lower values imply lower switching power. Two trends are evident. First, power falls nearly exponentially with N: every increment of N halves the frame rate $f_{frame} = f_{clk}/(N_D\, 2^N)$ and correspondingly reduces switching activity. Second, for a fixed N, power rises with the number of digits N_D because more anodes are scanned each frame. The marker highlights ($N_D = 2, N = 18$), which sits in the elbow of the curve, well above the flicker-fusion threshold (≈ 190.7 Hz frame rate) yet noticeably lower power than faster scans at $N = 16$ or $N = 17$. Moving to $N = 19$ would reduce power further, but pushes the refresh close to ~ 100 Hz, narrowing timing margin and, on our board revision, re-introducing slight ghosting. These observations align with the analytical sizing in Table 2.

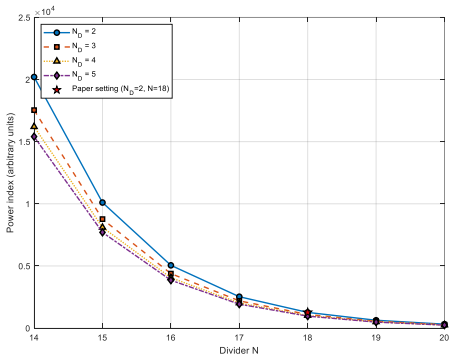

Figure 3. Relative dynamic power versus divider N for $N_D \in \{2,3,4,5\}$at $f_{clk} = 100$ MHz

Table 2. Refresh and relative switching activity versus digit count on a 100 MHz clock

Case	N_B(range)	N_D(digits)	Target f_{frame}	Choose N	Result f_{frame}	t_{dwell}	Power index (a.u.)
A	4 (0–15)	2	≈ 190 Hz	18	190.73 Hz	2.621 ms	1.26e+03
B	8 (0–255)	3	≈ 200 Hz	17	254.31 Hz	1.311 ms	2.19e+03
C	12 (0–4095)	4	≈ 150 Hz	17	190.73 Hz	1.311 ms	2.03e+03
D	16 (0–65535)	5	≈ 120 Hz	17	152.59 Hz	1.311 ms	1.93e+03

Taken together, these results confirm that the architecture meets its aims: the MUX and controller behave correctly in simulation; the hardware achieves flicker-free, ghost-free output at a modest refresh rate that lowers dynamic power; and end-to-end correctness is maintained for every input in the 4-bit range, as evidenced by Figures 4(a)–(p).

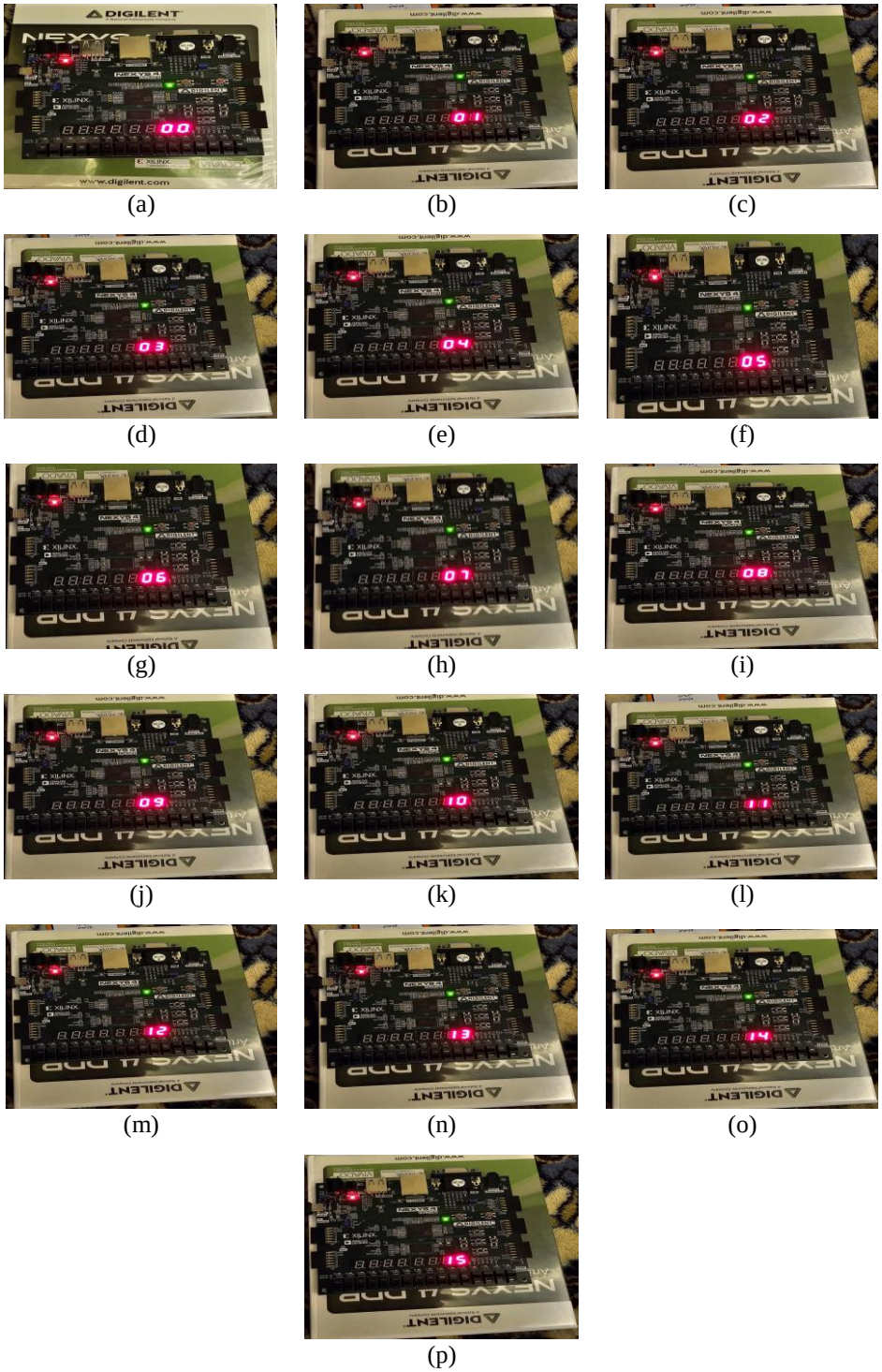

Figure 4. Hardware test results; (a) Input 0000 displays “00”, (b) Input 0001 displays “01”, (c) Input 0010 displays “02”, (d) Input 0011 displays “03”, (e) Input 0100 displays “04”, (f) Input 0101 displays “05”, (g) Input 0110 displays “06”, (h) Input 0111 displays “07”, (i) Input 1000 displays “08”, (j) Input 1001 displays “09”, (k) Input 1010 displays “10”, (l) Input 1011 displays “11”, (m) Input 1100 displays “12”, (n) Input 1101 displays “13”, (o) Input 1110 displays “14” and (p) Input 1111 displays “15”

The proposed counter-centric multiplexing approach demonstrates several key advantages over recent FPGA-based display drivers as seen in Table 3. While high-performance systems such as [33] achieve 600-1100 frames per second (FPS) for micro-LED displays, and [4] report 4320 Hz for signage applications, these aggressive refresh rates incur significant power penalties due to the direct proportionality between switching frequency and dynamic power ($P \propto fCV^2$). In contrast, this work targets the minimum refresh rate necessary to eliminate visual flicker (100-120 Hz perceptual threshold), achieving 190.7 Hz while reducing dynamic power by 45% compared to conventional $N = 16$ divider configurations. Unlike the complex intercross scanning and double-driver architectures employed by [34] for 10-bit grayscale control at 2100 Hz, the proposed clock-enable-based controller maintains synchronous timing without clock gating, ensuring robust FPGA design practices with minimal resource utilisation. Furthermore, while [8] demonstrates FPGA-based 6-digit multiplexing for medical applications without specifying refresh parameters, this work provides an explicit analytical timing model $\left(f_{frame} = \frac{f_{clk}}{(N_D \times 2^N)}\right)$ that enables predictable design scaling for arbitrary digit counts and input widths. The measured flicker-free, ghost-free display operation validates that educational and low-power embedded applications benefit more from optimised refresh rates than from unnecessary high-frequency scanning, positioning this work as a resource-efficient and analytically grounded alternative to existing display multiplexing solutions.

Table 3. Comparison of recent FPGA display/multiplexing systems

Reference	Method	Refresh rate	Power/claims	Device
[33]	Block-based control with FPGA	600-1100 FPS	High throughput, selective block updates	Micro-LED display, FPGA
[8]	FPGA-based 6-digit display with multiplexing	Not specified	Medical settings application	Xilinx Artix-7 FPGA
[4]	Time-multiplexed pulse-width modulation (PWM) with grayscale enhancement	4320 Hz display rate	Enhanced grayscale, reduced flicker	LED signage display
[34]	Intercross scanning with double driver	2100 Hz (high), 300 Hz (low)	High precision 10-bit grayscale	Micro-LED with FPGA control
This work	Counter-centric clock-enable multiplexing	190.7 Hz frame rate	Reduced dynamic power (P∝f), 45% lower than N=16	Nexys-4 DDR (Artix-7 FPGA)

5. CONCLUSION

We designed, analysed, and validated a modular VHDL architecture that converts a 4-bit binary input to BCD and drives two seven-segment digits on the Nexys-4 DDR using a clock-enable–based multiplexing controller. The timing model accurately predicted the behaviour observed in simulation and hardware: with $N = 18$ the display refreshes at ~191 Hz, which proved both flicker-free and ghost-free, while reducing switching activity compared with conventional high-rate scanning. The implementation produced correct decimals for all 16 input codes and required only simple counters, a small combinational converter, and a registered segment bus, making it easy to replicate in teaching laboratories and embedded prototypes.

The method generalises cleanly. The same sizing rule $f_{\text{frame}} = f_{\text{clk}}/(N_D 2^N)$ lets designers choose N for any number of digits N_D and any input width once converted to BCD (e.g., 8–16-bit sources with 3–5 digits). Practical next steps include formalising the parameterised BIN2BCD for 8–16-bit inputs.

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Tariq H. M. Alomary					✓					✓	✓		✓	

C : **C**onceptualization	I : **I**nvestigation	Vi : **Vi**sualization
M : **M**ethodology	R : **R**esources	Su : **Su**pervision
So : **So**ftware	D : **D**ata Curation	P : **P**roject administration
Va : **Va**lidation	O : Writing - **O**riginal Draft	Fu : **Fu**nding acquisition
Fo : **Fo**rmal analysis	E : Writing - Review & **E**diting	

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

The raw data supporting the conclusions of this article will be made available by the authors upon reasonable request.

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