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High-efficiency Doherty amplifier with metamaterial harmonic control for sub-6 GHz 5G base station

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ABSTRACT

This paper presents a broadband Doherty power amplifier (DPA) for Sub-6 GHz 5G wireless applications, integrating a metamaterial-based harmonic control circuit to suppress the 2nd and 3rd harmonics. The design employs a CGH40010F transistor on a Rogers RO3004C substrate. All results are obtained from simulations, while the resonator has been experimentally validated. The proposed approach enhances drain efficiency under output back-off (OBO) conditions without compromising linearity. Simulation results show a gain of 12.2–16.18 dB, with drain efficiency from 50.42 % to 79.83 %. Efficiency remains high at 3 dB and 6 dB back-off, ranging from 50.8–75.6 % and 36–62.8 %, respectively. These findings demonstrate the DPA's potential for next-generation base stations requiring compact, efficient, and wideband amplifiers, offering a practical solution for modern wireless communication systems. The novelty lies in combining broadband DPA design with harmonic suppression via metamaterials, providing improved efficiency and spectral performance.

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1. INTRODUCTION

Modern wireless communication systems, including third generation (3G), fourth generation (4G), and emerging fifth generation (5G) standards, rely on highly spectrally efficient modulation schemes to increase data throughput and fully exploit system capacity. Technologies such as wideband code division multiple access (WCDMA), code division multiple access 2000 (CDMA2000), and long term evolution (LTE) employ digital modulation formats characterized by a high peak-to-average power ratio (PAPR). As a consequence, radio-frequency (RF) power amplifiers (PAs) are required to operate predominantly in output power back-off (OBO) conditions to satisfy stringent linearity constraints.

To avoid signal distortion, conventional RF power amplifiers are typically biased in Class A or Class AB modes. These amplifiers must operate with an output power back-off of at least 6–9 dB. However, their efficiency degrades significantly in this region, leading to excessive power dissipation. This limitation becomes even more critical in modern wireless systems, where miniaturization and cost reduction impose simpler cooling solutions. As a result, achieving high efficiency under back-off conditions has become a key challenge for RF power amplifier design.

To address this issue, the Doherty power amplifier (DPA) architecture was introduced. By employing two parallel amplifying paths (main and auxiliary) the Doherty structure enhances efficiency in the back-off

region through active load modulation. In addition to efficiency, gain remains a critical parameter, as sufficient amplification is required without compromising linearity. Therefore, the design of DPAs inherently involves a trade-off between efficiency, linearity, and gain, particularly for high-PAPR wireless signals [1].

In recent years, significant progress has been made in DPA design, as reported in several studies [2]–[9], aiming to improve bandwidth, efficiency, linearity, and gain. Various harmonic control and impedance transformation techniques have been proposed. For instance, the work in [2] employs a Wilkinson power divider to achieve harmonic suppression; however, the overall efficiency remains limited to approximately 40%. In study [3], a high-efficiency DPA operating in the 5G band is presented, achieving high drain efficiency at saturation through digital predistortion (DPD). Other approaches rely on modified power dividers with resonant structures [4], generalized combiners for continuous-mode operation [5], or coupled-line phase compensation networks to extend bandwidth [6]. Although these techniques improve performance, they often increase circuit complexity, size, or design sensitivity. Furthermore, the non-ideal behavior of auxiliary amplifiers and parasitic effects continue to limit efficiency and broadband impedance stabilization, as discussed in [8], [9].

Despite these efforts, few studies have addressed the integration of metamaterial-based structures for simultaneous broadband impedance stabilization, harmonic control, and circuit miniaturization in DPAs. Existing harmonic control techniques such as post-matching networks, harmonic traps, or hybrid combiners typically involve lumped elements or complex distributed networks, which increase losses and physical size. In this context, metamaterial-inspired transmission lines offer unique advantages for wideband DPA design. Their inherent properties enable compact implementations, flexible phase compensation, and efficient harmonic suppression within a single multifunctional structure. These features make metamaterials particularly attractive for broadband Doherty architectures, where size reduction, harmonic control, and load modulation must be achieved simultaneously.

This paper presents a novel broadband DPA incorporating a harmonic control circuit based on composite right-hand/left-hand transmission lines. The proposed approach enables high efficiency and gain while effectively suppressing the second and third harmonics over a wide frequency range. The amplifier operates from 1.8 to 2.5 GHz, making it suitable for Sub-6 GHz 4G and 5G wireless applications. Within this band, the measured gain ranges from 12.2 to 16.18 dB, while the drain efficiency varies from 50.42% to 79.83%. At 3 dB and 6 dB output power back-off, the drain efficiency remains between 50.8%–75.6% and 36%–62.8%, respectively. Beyond power amplifier design, metamaterial-based resonators have demonstrated strong potential in various microwave and electromagnetic applications, including antennas, filters, and emerging terahertz systems. Their ability to provide compactness and enhanced electromagnetic control has motivated their increasing adoption in advanced wireless architectures [10]–[17].

Motivated by the growing demand for high-efficiency and compact solutions in Sub-6 GHz 5G base station systems, this work proposes an original front-fed DPA architecture integrating a metamaterial-based harmonic control circuit. This integration enables improved efficiency, extended bandwidth, and enhanced linearity within a compact layout. As illustrated in Figure 1, the proposed DPA is positioned within the transmitter chain of a 5G base station, where efficient and linear power amplification is essential. Figure 2 further highlights the interaction between the DPA and wireless sensors in practical deployment scenarios.

The main contributions of this work are summarized as follows:

- Proposal of a novel front-fed DPA topology integrating a metamaterial-based harmonic control circuit, enabling compact, efficient, and linear operation for Sub-6 GHz 5G applications.
- Design of a metamaterial-inspired harmonic control network that enhances gain and drain efficiency over a wide operating bandwidth.
- Development of an analytical model based on zeroth-order resonator theory and S-parameter analysis, allowing accurate prediction of transmission zeros and harmonic suppression behavior.
- Experimental validation of the proposed harmonic control circuit, demonstrating its effectiveness in terms of efficiency, gain, compactness, and broadband performance.
- Demonstration that the use of a Doherty architecture maintains good drain efficiency at 3–6 dB back-off. Unlike conventional amplifiers, whose efficiency drops significantly outside saturation, the Doherty structure dynamically adapts to signal variations through its main and auxiliary paths, ensuring efficient power management for complex 5G modulation schemes.
- Implementation of a harmonic control circuit without lumped elements or soldering, resulting in a cost-effective, low-loss, and space-efficient solution. Moreover, the modular nature of the resonator cells enables straightforward extension to higher-order harmonic control.

Figure 1 provides an overview of the DPA and highlights its key role in modern RF systems. It illustrates Figure 1(a) the functional integration of the DPA within the RF front-end of a radio unit, emphasizing its importance in the transmission chain, Figure 1(b) the conventional DPA architecture based on the main and

auxiliary amplifier paths, and Figure 1(c) an enhanced DPA architecture incorporating a metamaterial-based harmonic control circuit, aimed at improving efficiency and spectral performance.

The structure of this paper is as follows: section 2 provides a theoretical analysis of load modulation in the low-power region, along with harmonic control based on composite right/left-handed transmission lines. Section 3 outlines the design methodology, presents the results, and includes a comparative performance analysis. Finally, section 4 concludes the study by summarizing the main contributions and highlighting potential future directions.

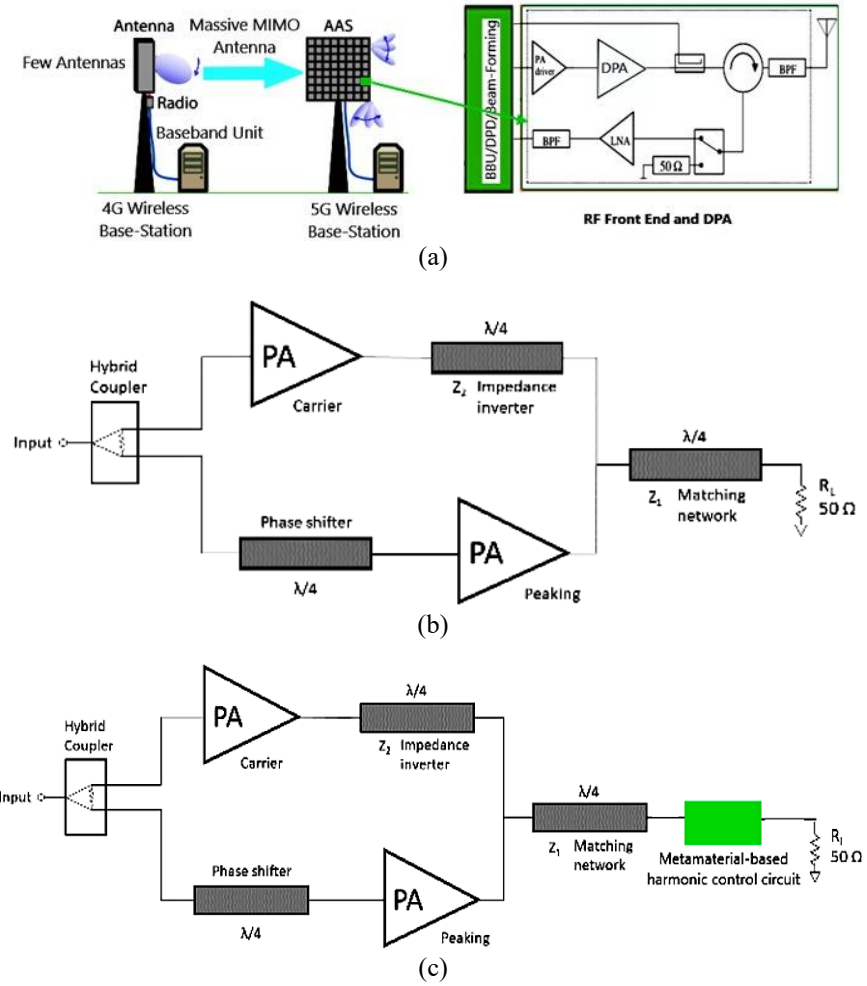

Figure 1. Overview of the DPA and its role in RF systems: (a) the function of the DPA within the RF front-end of a radio unit, (b) the DPA architecture, and (c) the DPA architecture with a metamaterial-based harmonic control circuit

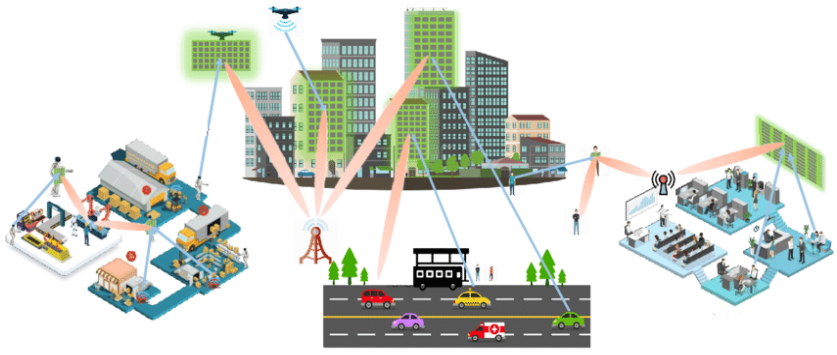

Figure 2. Link between the 5G base station DPA and everyday wireless sensors

2. THEORETICAL ANALYSIS

The proposed DPA architecture is based on the integration of two transistors, referred to as "carrier" and "peak," each associated with an input impedance matching network (IMN). A power combiner is employed to aggregate the output power from both transistors while dynamically modulating the load, as illustrated in Figure 3. The amplifier is loaded with an impedance R_L. It should be noted that if this impedance differs from 50 Ω, an output matching network becomes necessary. For the sake of simplicity, the study assumes a symmetrical configuration in which the "carrier" and "peak" transistors are identical. In order to enhance power conversion efficiency at lower power levels, a harmonic suppression circuit has been incorporated into the design. This circuit, based on composite right left-handed transmission line (CRLH-TL), effectively attenuates the second and third harmonic components, as shown in Figure 3. Figure 3 illustrates the simplified schematic of our DPA, incorporating a harmonic control circuit intended to improve efficiency and gain performance.

According to the theoretical analysis presented in [18], the optimal Doherty combiner can be simplified as shown in Figure 4(a). In this Figure 4, the carrier and peak transistors are modeled by current generators IC and IP, respectively. The combiner consists of two transmission lines, TL1 and TL2, as shown in Figure 4(a). The electrical lengths of TL1 and TL2 must be $\theta_1 = 90°$ and $\theta_2 = 180°$, respectively, at the center operating frequency f_c. In addition, the characteristic impedance of the TL1 and TL2 lines must be $Z_1 = Z_2 = R_0$, where R_0 represents the optimum impedance of the transistor used. In addition, the combination load is given by $R_L = R_0/2$.

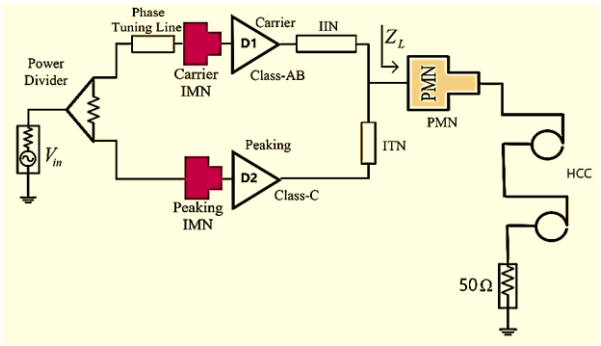

Figure 3. Simplified block diagram of the proposed DPA with harmonic control circuit

2.1. Load modulation at low power region

In the low-power region, the peak transistor is deactivated. The structure of the DPA is shown in Figure 4(b). At this point, the cascade network formed by TL1 and TL2 is described by an ABCD matrix [19].

$$\begin{bmatrix} A_{BO} & B_{BO} \\ C_{BO} & D_{BO} \end{bmatrix} \tag{1}$$

where the terms A_{BO}, B_{BO}, C_{BO}, and D_{BO} are expressed as:

$$A_{BO} = \cos(\theta_1.f) - \frac{Z_1}{Z_2}.\sin(\theta_1.f).\tan(\theta_2.f) \tag{2}$$

$$B_{BO} = j.Z_1.\sin(\theta_1.f) \tag{3}$$

$$C_{Bo} = \frac{j\,sin(\theta_1,f)}{z_1} + \frac{j\,cos(\theta_1,f)\,tan(\theta_2,f)}{z_2} \tag{4}$$

$$D_{BO} = \cos(\theta_1.f) \tag{5}$$

In the above equations, f denotes the normalized frequency, relative to the center frequency f_c. By applying (1) to (5), the fundamental load impedance of the carrier transistors in the low-power region can be determined using (6).

$$z_{CB} = \frac{A_{BO}R_L + B_{Bo}}{C_{BO}R_L + D_{BO}} \tag{6}$$

This expression provides critical insight into how the matching network transforms the output load impedance seen by the carrier device, ensuring optimal load modulation across the amplifier's operating bandwidth, even in the absence of the peaking path. Such an analysis is essential for achieving high efficiency in back-off conditions, a key advantage of the Doherty architecture.

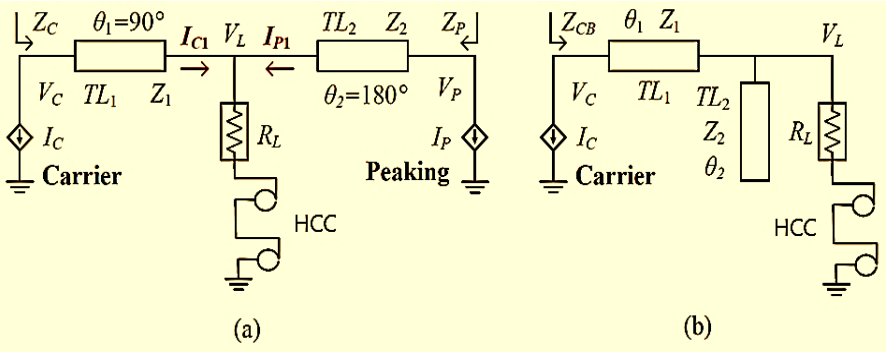

Figure 4. Overview of the proposed DPA illustrating its operation under different power regimes: (a) simplified schematic representation of the proposed DPA and (b) simplified schematic representation of the DPA in the low-power region

2.2. Harmonic control using CRLH-TL

Split-ring resonators based on composite right/left-handed transmission lines represent a significant advancement in metamaterials and high-performance RF/microwave devices [20]. These structures, built from periodic unit cells combining capacitive and inductive elements, exhibit both left-handed (LH) and right-handed (RH) behaviors depending on the frequency, enabling wideband operation and tunable responses. Unlike conventional transmission lines, CRLH-TLs account for parasitic elements, providing a realistic representation of physical behavior. A key feature is the zero-order resonance, allowing device miniaturization without performance loss, which makes them ideal for compact filters, multiband antennas, harmonic control circuits, and high-efficiency amplifiers.

In this work, we employed these zero-order resonators to suppress the second and third harmonics, improving both drain efficiency and overall gain of the Doherty amplifier. This approach enhances spectral purity, reduces interference, and maintains high efficiency even in back-off mode, making the amplifier robust and suitable for wideband wireless applications in 4G, 5G, and future communication systems.

The resonance characteristics of these zero-order resonators (ZOR) are described using the CRLH-TL dispersion relation, which was derived by applying the theory of Bloch and Floquet in (7) [20].

$$\beta_n = \frac{n\Pi}{l} \ (n=0, \pm1, \pm2, \ldots) \tag{7}$$

Such that βn represents the phase constant of the CRLH transmission line for resonance mode n.

One of the most interesting aspects of ZORs is the independence of the resonant frequency from the physical length of the transmission line. This means that the resonance frequency can be adjusted without the need to modify the physical size of the resonator, making these devices particularly attractive for a variety of applications. In addition to their main function of eliminating certain unwanted frequencies, these resonators also play a crucial role in impedance matching in specific circuits, making them multifunctional and valuable in the design of microwave systems [20].

These ZOR resonators resonate at ω_{res} as shown in (8) [20], [21].

$$\omega_{res} = \frac{1}{\sqrt{L_L C_R}} \tag{8}$$

where L_L is the inductance associated with the left-hand circular polarization, and C_R is the capacitance associated with the right-hand circular polarization.
With

$$L_L = \mu_0 R_m \left(\ln\left(\frac{8R_m}{h+W_a}\right) - 0.5\right) \text{ [22]} \tag{9}$$

where μ_0 is the vacuum permeability, W_a is the ring width, h is the ring height and R_m is the mean radius, calculated using (10).

$$R_m = R + \frac{W_a}{2} \quad (10)$$

where R is the internal radius of the SRR (Figure 5).

$$C_R = \varepsilon_0 \varepsilon_r \frac{D.W_l}{H} \text{ [23]} \quad (11)$$

Where D is the length of the microstrip line, ε_0 is the permittivity of the vacuum, W_l is the width of the microstrip line, ε_r is the relative permittivity of the substrate and H is the height of the substrate (Figure 6). Assuming that the CRLH-TL resonator is lossless, the equivalent schematic is presented in Figure 7 [22]. Such as C_R is the capacitance associated with right-hand circular polarisation, C_L is the capacitance associated with left-hand circular polarisation, L_R is the inductance associated with right-hand circular polarisation and L_L is the inductance associated with left-hand circular polarisation.

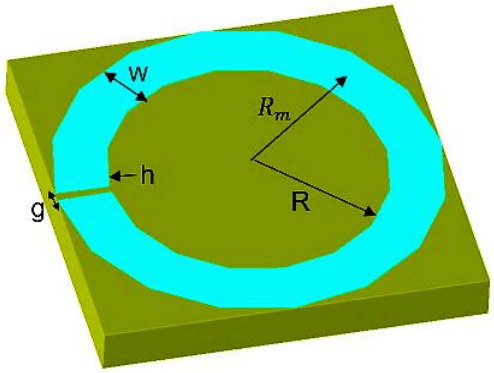

Figure 5. Split ring resonator

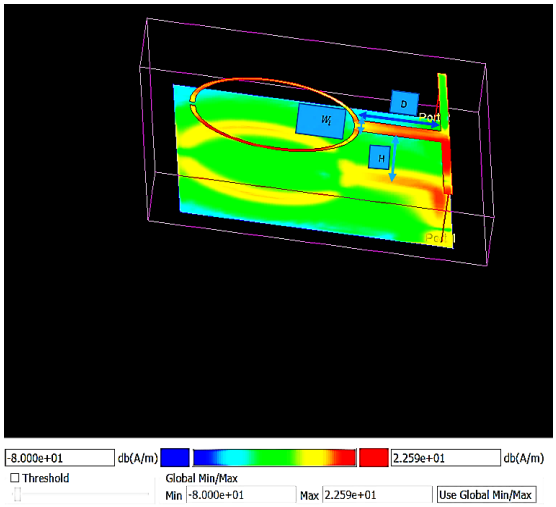

Figure 6. The structure of the CRLH resonator

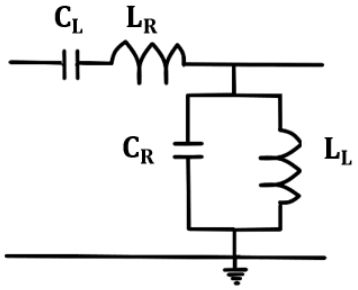

Figure 7. Equivalent electrical schematic of our proposed CRLH-TL type circuit

3. RESULTS AND DISCUSSION

In this section, we present and discuss the experimental results of the CRLH-TL resonator and the simulation results of the DPA. This section serves as an extension of the previously discussed theory and aims to validate our main contribution: the use of compact, fully distributed CRLH-TL resonators to achieve highly precise suppression of the second and third harmonics. These resonators are miniaturized, simple, cost-effective, and their fully distributed design requires neither lumped elements nor soldering, facilitating integration into the DPA.

For the DPA, the study focuses on the key performance metrics: gain and linearity at full power, as well as the simulated drain efficiency, evaluated at saturation and at 6 dB OBO. The simulations also include OIP3 and IMD performance. The operating frequency band of the DPA extends from 1.8 to 2.5 GHz. The results clearly demonstrate the superiority of our design in terms of efficiency, gain, and harmonic suppression precision, while validating the theory presented in the previous section.

3.1. Experimental results of the resonator

The layout of these two ZOR resonators is shown in Figure 8. Simulation results for the S parameters, in particular S_{11} and S_{21}, are shown in Figure 9. Since we were working in the 1.8 to 2.5 GHz frequency band, we were particularly interested in the harmonics of the 2.4 GHz frequency, in addition to the center frequency. This avoids the effect of resonance over the operating band, allowing us to achieve better results in our design. Figure 8 shows the frequency response of the resonator, confirming the effective suppression of the second- and third-order harmonics.

The layout of these two ZOR resonators is presented in Figure 8. The simulation results of the S-parameters, particularly S_{11} and S_{21}, are shown in Figure 9. Since we were working within the 1.8 to 2.5 GHz frequency band, we focused on the harmonics around 2.4 GHz rather than those of the center frequency. This approach helps to avoid unwanted resonance effects within the operating band, allowing us to achieve improved performance in our design.

Figure 10 shows the photograph of the zero-order resonator designed in this study. Figure 11 presents the measurement results obtained from this resonator. The experimental results indicate a practical resonance frequency of 1.79 GHz. This measured value is particularly significant as it can be directly compared to the theoretical predictions derived from our modeling approach. Based on the precise dimensions of the resonator provided in Table 1, and using the adapted equations developed to calculate the capacitances L_L and C_R, we computed the theoretical resonance frequency of the device. The theoretical calculation yields a resonance frequency of 1.7 GHz, which is very close to the experimentally measured value.

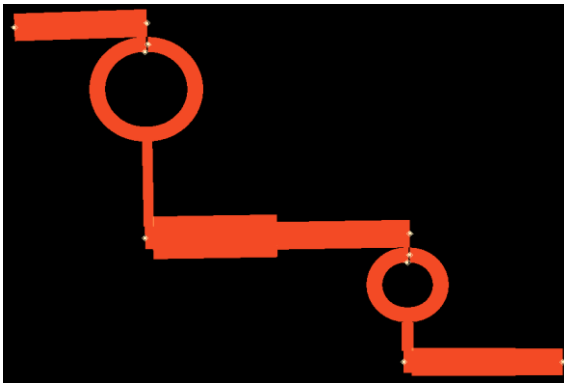

Figure 8. Proposed zero-order resonators layout

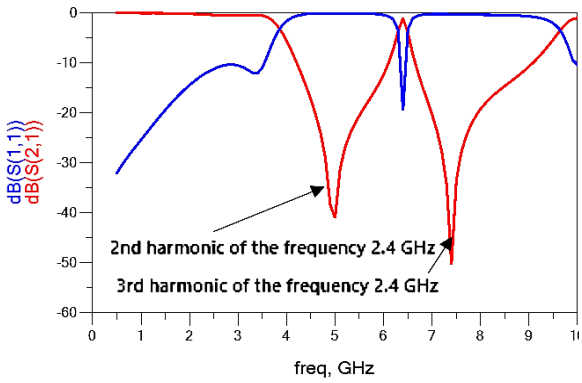

Figure 9. Frequency response of the resonators' S_{11} (reflection coefficient) and S_{21} (transmission coefficient) parameters

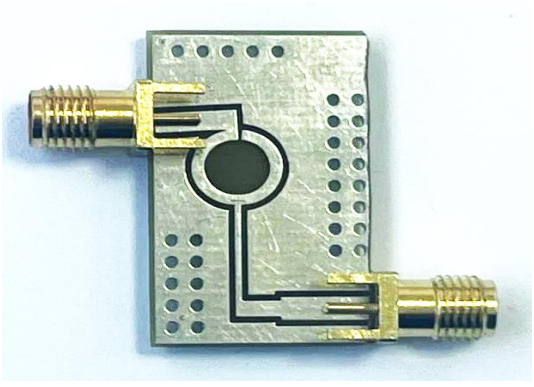

Figure 10. Photograph of the zero-order resonator used for harmonic suppression

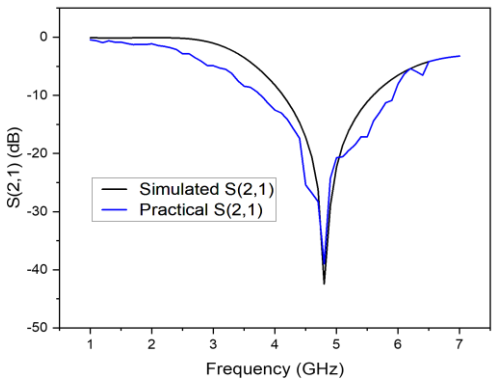

Figure 11. Transmittance of the resonators shown in Figure 9

Table 1. Parameters used to design our CRLH-TL resonator

μ_0 (H/m)	R_m (mm)	R (mm)	W_a (mm)	H (mm)	
12×10^{-7}	3	2.65	1	35×10^{-3}	
ε_0 (F/m)	ε_r	D (mm)	W_l (mm)	H (mm)	g (mm)
8.854×10^{-12}	3.38	6	0.5	0.813	0.1

This strong agreement between experimental and theoretical results serves as a robust validation of our innovative method, allowing highly accurate prediction of the resonance frequency of zero-order resonators. This capability to precisely control the resonance frequency is a major advantage, enabling optimized control of the electromagnetic properties of the resonators. Furthermore, these zero-order resonators have a wide range of applications within RF systems. One of the major challenges in this field is the effective manipulation of frequencies, particularly the suppression of unwanted frequencies that can degrade signal quality or interfere with circuit operation. These resonators not only facilitate the filtering of unwanted frequencies but also enable multiband behavior, which is crucial for modern communication systems that must operate simultaneously over multiple frequency bands.

Thus, the flexibility and precision offered by zero-order resonators make them key components for numerous RF applications, including advanced filters, low-noise amplifiers, miniaturized antennas, and wireless communication devices. This innovative technology contributes to enhancing the performance, compactness, and reliability of RF equipment, meeting the increasing demands of current and future telecommunication networks. These resonators offer numerous advantages that make them highly suitable for modern microwave circuit applications. One of their most significant features is their exceptional compactness. Unlike conventional resonators whose size is determined by the wavelength, CRLH-TL resonators can operate in the zero-order mode, according to Bloch–Floquet theory. As a result, their resonant frequency is independent of physical length, allowing for the design of extremely small components without compromising performance.

This property leads to lightweight, low-cost, and easy-to-fabricate structures. These resonators can be implemented using standard microstrip technologies and materials, reducing manufacturing complexity and production costs. Their minimal size makes them ideal for high-density integration in compact or portable RF and microwave systems, including low-noise amplifiers, filters, and multifunctional antennas.

In this work, we conducted a detailed and rigorous study to determine the resonant frequency with high precision using adapted analytical equations. Unlike most studies in the literature, which generally present resonance frequencies through simulations or measurements, our approach provides an accurate theoretical estimation. The calculated resonance frequencies showed excellent agreement with both simulated and measured results, demonstrating the reliability and accuracy of the proposed method. This ability to precisely predict the resonant behavior of CRLH-TL resonators is rarely addressed with such depth in existing works and constitutes a novel and significant contribution. Consequently, these resonators stand out as compact, cost-effective, and precisely engineered components for the next generation of microwave and RF devices.

Beyond these advantages, resonators play a fundamental role in the design of radiofrequency and microwave circuits, being integrated into various components such as antennas, low-noise amplifiers, mixers, oscillators, filters, and other passive and active devices. Their importance lies in their ability to provide high frequency selectivity, effective impedance control, and targeted suppression of unwanted signals, while enabling precise manipulation of electromagnetic wave propagation within compact structures.

These resonators address major technical challenges in modern RF systems, notably the management of electromagnetic interference, especially in dense spectral or multi-band environments. Their well-defined frequency response allows selective rejection of unwanted signals while maintaining transparency at desired frequencies. Another key advantage is circuit miniaturization. Unlike traditional modular architectures, which often involve multiple functional blocks and increased bulk, resonators enable denser functional integration due to their resonant behavior and compact structure. This multifunctionality helps reduce the overall circuit size, simplify design, and limit losses associated with interconnections.

In this work, we employed these resonators as harmonic control circuits specifically within power amplifiers. This application helped reduce nonlinear distortions, improve linearity, and enhance overall energy efficiency. Thus, resonators act as filters capable of attenuating undesired harmonic components generated by nonlinearities of active devices. In addition, this technique eliminates the need for lumped components or soldering, which significantly reduces insertion losses at high frequencies.

Finally, their compatibility with planar fabrication technologies, such as microstrip structures, facilitates integration into monolithic or hybrid circuits while maintaining optimal electrical performance. This adaptability fosters their growing use in emerging fields such as 5G, the internet of things (IoT), compact radar systems, and satellite communications, where demands on selectivity, compactness, and performance are increasingly stringent.

3.2. Construction and simulation results of the DPA

This section details the full design procedure of our DPA, outlining each stage in a clear and systematic manner. We emphasize the engineering decisions and methodologies applied to enhance the amplifier's performance within the desired frequency range. The comprehensive results achieved during this development are presented and evaluated to demonstrate the solution's effectiveness and relevance.

To contextualize our work within the current research landscape, we performed an extensive comparison with recent studies in the area of Doherty amplifiers. This evaluation underscores notable advancements introduced by our design, especially regarding power efficiency and signal linearity. The findings confirm that our approach delivers improved performance, reinforcing the significance and reliability of our contribution relative to existing approaches.

3.2.1. DPA design

The proposed DPA is implemented on a Rogers RO3004C substrate, selected for its low loss and frequency stability, with a relative permittivity of 3.38, a loss tangent of 0.0027, and a thickness of 0.813 mm. The complete circuit architecture, including the type of transistor used, the bias conditions, and the operating classes of the carrier and peaking transistors, is presented in detail in Figure 12 [24]. The input and output matching networks are designed to ensure optimal impedance matching at the center operating frequency and to guarantee proper operation of the DPA in both low- and high-power regimes.

For the proposed design, the GaN CGH40010F HEMT transistor from the CREE foundry is selected due to its broadband capability, operating from DC to 6 GHz, and its ability to deliver up to 10 W of output power with a drain bias voltage of V_{DS} = 28 V. In the DPA architecture, two identical CGH40010F transistors are employed. The first transistor operates as the main (carrier) amplifier, biased at V_{DS} = 28 V and V_{GS} = −2.6 V, corresponding to Class-AB operation, while the second transistor acts as the auxiliary (peaking) amplifier, also biased at V_{DS} = 28 V but with V_{GS}= −6.8 V, enabling Class-C operation. The DPA biasing scheme relies on a single common drain supply for both transistors, whereas the gate bias voltages are independently adjusted to set the required operating class of each branch, ensuring effective load modulation and enhanced efficiency under power back-off conditions.

To accurately control the intrinsic impedances of the selected transistor, a parasitic network extraction is carried out. As illustrated in Figure 12, a de-embedding procedure is applied to the commercial large-signal model of the CGH40010F, allowing access to the intrinsic gate and drain terminals by removing the parasitic networks located between the intrinsic and extrinsic reference planes at both the input and output. This step is essential for precise impedance tuning over the operating band and enables proper fundamental matching as well as effective harmonic suppression. The performance of the proposed DPA is evaluated under large-signal excitation using the manufacturer-provided nonlinear transistor model, which accounts for saturation, compression, and harmonic generation effects. Altogether, these design choices ensure the consistency of the presented results and allow the reproducibility of the proposed DPA design.

The DPA is designed through a step-by-step process, presented in this section:

- Step 1 : the Doherty load Z_L is set to 15 Ω. An impedance matching network (PMN) is designed to match 15 Ω to a standard 50 Ω impedance. The PMN consists of four microstrip lines connected in series, allowing efficient matching between these two impedances. It is important to note that, in our operating band, the optimum impedance at the output is 30 Ω, while at the input it is 10 Ω [25]. Furthermore, since Z_L=15 Ω, the load impedance of the main and auxiliary PAs must be equal to 30 Ω at the maximum power level due to active load modulation.
- Step 2 : the impedance matching networks at the input of the main and auxiliary power amplifiers (IMN_C and IMN_P) are implemented to match the PAs, respectively, at their input terminals. A Wilkinson-type power divider is designed to divide the input power evenly between the main and auxiliary paths, ensuring correct power distribution between the two amplifiers.
- Step 3 : The final combiner is made by combining the main and auxiliary transistors with the PMN. A 25 Ω impedance transmission line (ITL), with an electrical length of 180°, must be inserted behind the auxiliary PA, while another 25 Ω impedance transmission line (IIL), with an electrical length of 90°, must be inserted behind the main PA. This ensures the correct operation of both transistors by allowing optimum impedance matching in both signal paths.
- Stage 4 : At this stage, metamaterial-based resonators are inserted into the circuit to eliminate the 2nd and 3rd harmonics. These resonators effectively reduce unwanted interference and improve the overall performance of the DPA by optimizing drain efficiency even under reduced-power (back-off) operating conditions.

The complete layout of the designed DPA, resulting from the proposed step-by-step design methodology, is shown in Figure 13. The layout integrates the load modulation network, input matching networks, power division and combining structures, as well as metamaterial-based resonators for harmonic suppression, reflecting the practical implementation of the overall DPA architecture. This high-efficiency DPA

incorporates an innovative harmonic control circuit based on zero-order resonators, which are known for their compact size, lightweight structure, low cost, and ease of fabrication in microstrip technology. The proposed design features a single drain supply shared between the main and auxiliary amplifiers, both of which are structurally identical, resulting in a fully symmetrical topology.

The overall dimensions of the circuit are 18.9×9 cm², reflecting a successful miniaturization while maintaining optimal performance. Thanks to this compact and efficient architecture, the amplifier delivers excellent results in terms of gain, power-added efficiency, and linearity, particularly within the sub-6 GHz frequency range. This makes it highly suitable for 5G base station applications, where operating stability, harmonic suppression, and energy efficiency are critical requirements. Furthermore, the adopted design approach significantly reduces manufacturing costs while maintaining high electrical performance, providing an optimal trade-off between cost and functionality. Consequently, this amplifier represents a promising solution for modern communication infrastructures that demand high-performance, compact, reliable, and cost-effective RF systems.

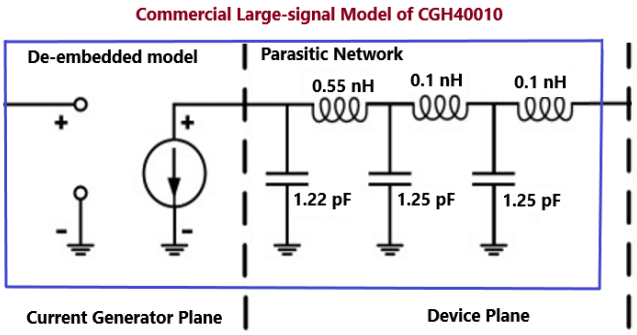

Figure 12. De-embedding of the commercial large-signal CGH40010 model, including the parasitic network between the intrinsic and extrinsic planes

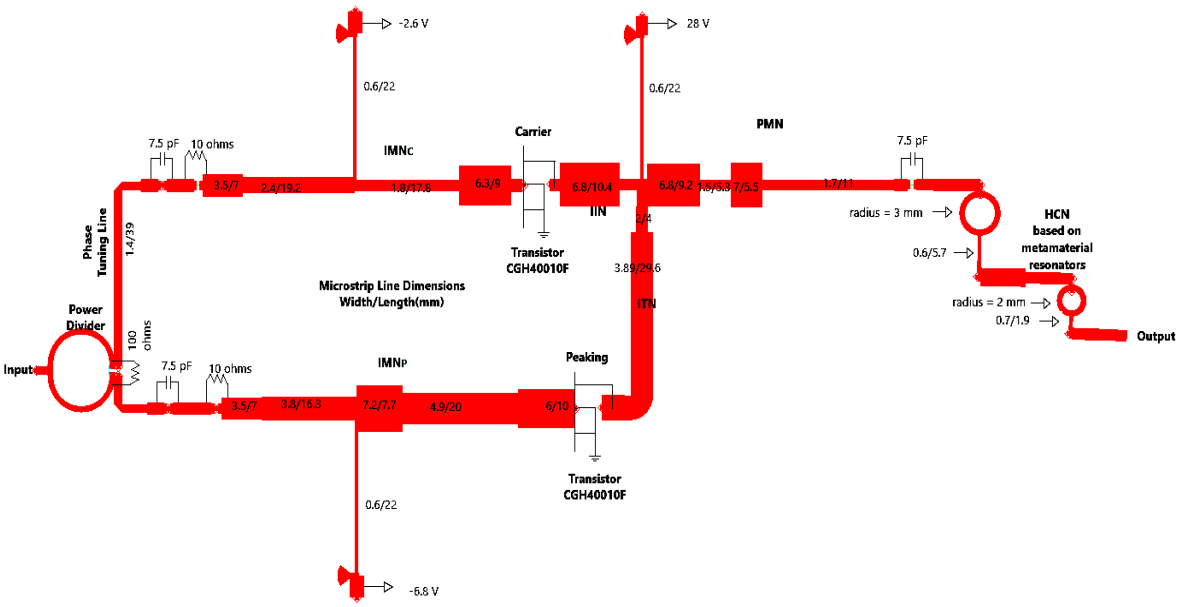

Figure 13. The layout of the designed DPA

3.2.2. Simulation results of the DPA

Based on the proposed design, the complete schematic of the designed DPA is presented in Figure 13. The simulation results, shown in Figures 14 to 16, were obtained through simulation. Figure 14 illustrates the simulated performance of the DPA in terms of drain efficiency and gain versus output power within the targeted

frequency band, with Figures 14(a) and 14(b) showing the simulated efficiency and gain, respectively. Figure 15 shows the variation of drain efficiency as a function of frequency at different OBO power levels, while Figure 16 depicts the average output power and drain efficiency across the [1.8–2.5] GHz range. These results provide a comprehensive assessment of the DPA's overall performance and help identify optimal operating conditions in terms of gain, efficiency, and output power.

The drain efficiency and gain characteristics of the designed DPA as a function of output power are illustrated in Figure 14, while Figure 15 depicts the DE at various output back-off levels relative to the saturation power. The simulations were conducted across a broad frequency range from 1.8 GHz to 2.5 GHz, with a fine resolution step size of 0.1 GHz to ensure accurate spectral analysis. The simulation outcomes confirm that the amplifier maintains excellent efficiency across the entire operational bandwidth. Specifically, the DE consistently exceeds 50% even at saturation, reaching a peak of 79.83%, highlighting highly efficient power utilization. Furthermore, the amplifier sustains strong efficiency under power back-off conditions—an essential feature for modern wireless systems that operate with high peak-to-average power ratios. At 3 dB and 6 dB OBO, the DE remains high, achieving 75.2% and 62.8%, respectively, demonstrating robust performance over a wide output power range.

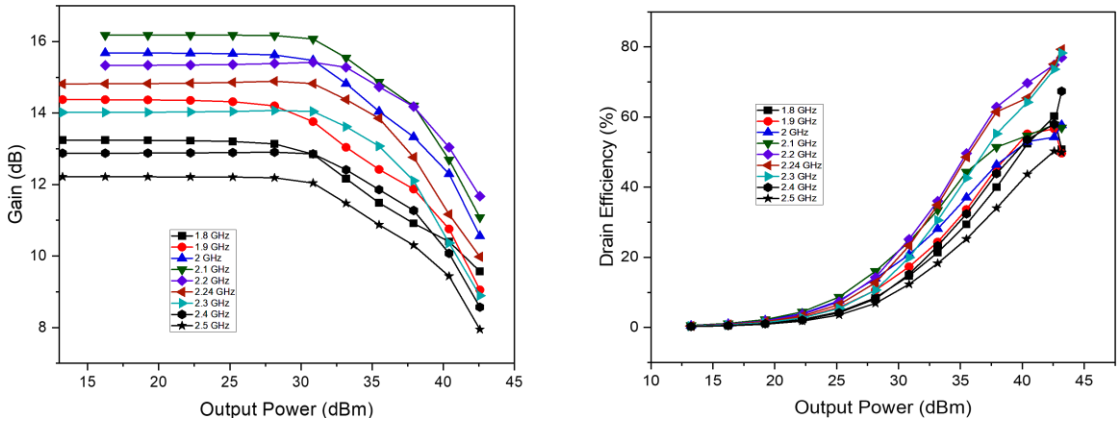

Figure 14. Simulated performance of the designed DPA in terms of efficiency and gain over the operating power range: (a) simulated drain efficiency, and (b) simulated gain of the designed DPA versus output power within the targeted frequency band

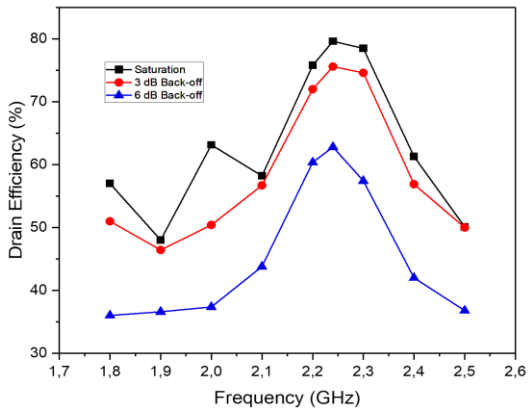

Figure 15. DPA drain efficiency as a function of frequency at different OBO power levels

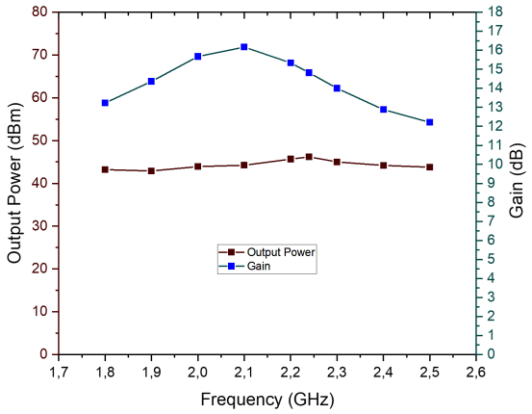

Figure 16. DPA average output power and drain efficiency over the 1.8 to 2.5 GHz range

In terms of gain, the DPA exhibits reliable amplification capabilities, as shown in Figure 15, with a saturation gain greater than 12.21 dB across the band and a maximum value of 16.18 dB observed at 2.1 GHz, confirming both the linearity and efficiency of the design. Additionally, Figure 14 shows that the output power

remains above 42.9 dBm throughout the operating frequency range, ensuring stable transmission levels suitable for advanced applications. These results underscore the effectiveness of the proposed DPA architecture, which combines high efficiency with strong gain performance, both at saturation and under backed-off conditions. Such behavior is particularly advantageous for 4G and sub-6 GHz 5G base stations, where efficiency across varying power levels is critical.

Figures 17 and 18 respectively illustrate the impact of the harmonic control circuit on the drain efficiency and gain of the Doherty amplifier. Incorporating this circuit leads to a significant improvement in power efficiency, indicating a more effective conversion of electrical power into useful output power, as well as an increase in gain, reflecting a stronger amplification of the input signal. These results highlight the crucial role of the harmonic control circuit in the overall optimization of amplifier performance, particularly in terms of efficiency and signal quality. By selectively suppressing second- and third-order harmonics, the circuit enhances spectral purity, which is essential to minimize interference and comply with the stringent requirements imposed by modern wireless communication standards such as 4G and 5G. Consequently, the harmonic control circuit proves to be indispensable for designing amplifiers that are both high-performing and fully compliant with current communication standards.

As shown in Figure 18, the DE reaches a maximum value of 79.83% at a frequency of 2.24 GHz when the resonators are integrated into the circuit. In contrast, without these resonators, the DE reaches only 73% at the same frequency. These results clearly highlight the significant impact of the resonators on improving the overall efficiency of the DPA. Figure 19 shows that the output third-order intercept point (OIP3), determined by the extrapolated intersection of the fundamental and IMD3 curves, is approximately 44 dBm, corresponding to an input power of around 35 dBm. This high OIP3 value indicates good linearity of the amplifier, while the rise of IMD3 from 25–30 dBm confirms the gradual onset of nonlinear distortions at high power levels.

Table 2 provides a performance summary of the designed amplifier in comparison with other recent works in the literature. The proposed design clearly stands out by achieving a peak drain efficiency of 79.83% at 2.24 GHz, representing a significant advancement over several existing solutions. Moreover, it maintains high efficiency even under power back-off, with DE values of 75.2% and 62.8% at 3 dB and 6 dB OBO, respectively. These metrics indicate strong linear behavior and operational stability, which are crucial for modulated signal environments.

The amplifier also offers a notable saturation gain exceeding 12 dB, reaching up to 16.18 dB, providing substantial signal amplification without compromising efficiency. Overall, the proposed design demonstrates a well-balanced performance across multiple key metrics, making it highly suitable for integration into next-generation wireless infrastructure. The obtained results fully validate the effectiveness of the adopted approach, which relies on the integration of a carefully optimized circuit topology combined with advanced harmonic control and suppression strategies. This synergy enables the realization of a DPA that is not only compact and energy-efficient but also capable of maintaining high performance across a broad output power range. Unlike conventional architectures, this design fully leverages the unique properties of metamaterial-based structures, significantly reducing signal losses, minimizing circuit footprint, and enhancing the spectral purity of the amplified signal.

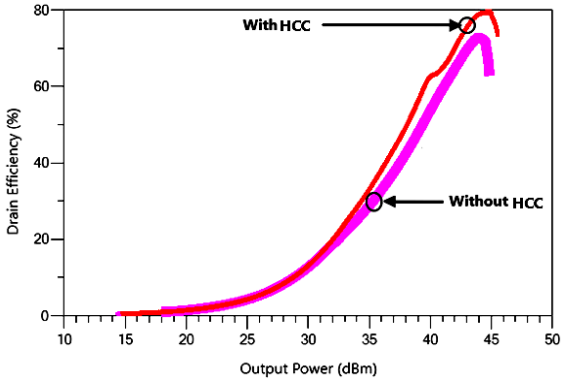

Figure 17. DPA drain efficiency with HCC and without HCC

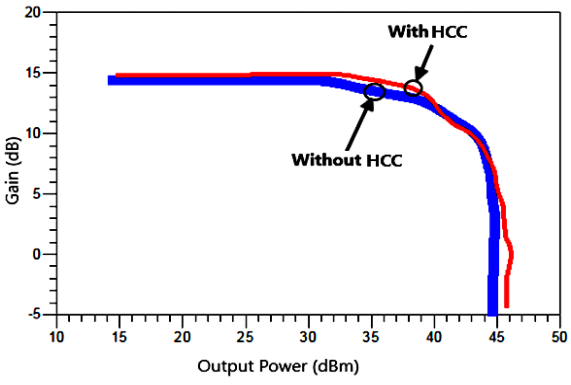

Figure 18. DPA gain with HCC and without HCC

Furthermore, by eliminating the need for lumped components and soldering through the use of planar microstrip-integrated resonators, this technique reduces insertion loss at high frequencies and simplifies the

manufacturing process. These combined advantages position the proposed amplifier as a highly suitable solution for the growing demands of next-generation communication systems such as 5G base stations, the IoT, and satellite communication platforms where compactness, energy efficiency, linearity, and reliability are all essential performance criteria.

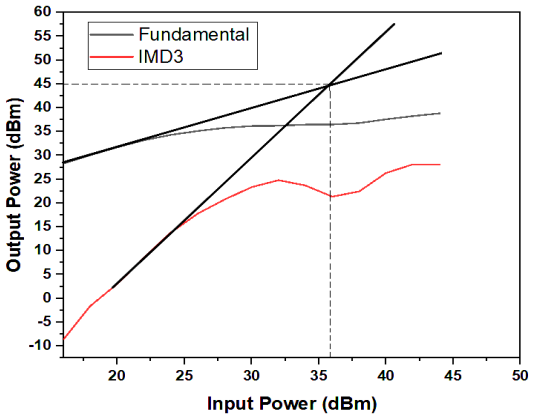

Figure 19. OIP3 extraction and IMD performance of the DPA during the two-tone test at 2.24 GHz

Table 2. State of the art of Doherty amplifiers

Ref. Year	Freq. (GHz)	BW. (GHz)	Pout (dBm)	DE@Sat (%)	DE@OBO(6dB) (%)	Gain@Sat (dB)
[26] 2023	1.0–2.5	1.5	43–44.2	62–76.5	44–56	8–13.5
[27] 2022	3.0–3.7	0.7	43.0–44.2	60.0–74.0	46.0–50.0	7.0–7.5
[19] 2024	1.45–2.45	1	42.7–44.9	62.4–74.1	40.5–59.8	9.4–13.9
	1.5–2.45	0.95	42.7–44.9	63.6–74.1	49.1–59.8	10.2–13.9
[28] 2024	1.7-2.6	2.15	43.2–45.2	58.4–69.1	46.3–57.7	9.1–11.2
[29] 2022	3.4-3.8	0.4	43.6–44.4	62–70	46-60	10-12
[30] 2024	5.1-7.2	2.1	37.2-39	51.6-58	38.4-50.5	10-12.3
This Work	1.8-2.5	2.15	42.9-46.2	50.4-79.83	36-62.8	12.2-16.18

Pout : Output power. DE@Sat : Saturation DE. DE@OBO : 6 dB back-off DE. Gain@Sat : Saturation gain

4. CONCLUSION

This paper presents a design approach for a broadband DPA targeting modern wireless communication systems such as 4G and 5G. The integration of a harmonic control circuit based on composite right/left-handed transmission lines enhances the amplifier's performance by improving drain efficiency and suppressing 2nd and 3rd order harmonics. Simulation results show that the drain efficiency reaches a maximum of 79.83 % at 2.24 GHz with the resonators, compared to 73 % without them, demonstrating the clear impact of the resonators on overall efficiency. The amplifier exhibits a gain ranging from 12.2 to 16.18 dB, with drain efficiency ranging from 50.8 % to 75.6 % at 3 dB OBO and from 36 % to 62.8 % at 6 dB OBO. Simulated linearity metrics indicate an OIP3 of approximately 44 dBm at an input power of 35 dBm, confirming good linearity while highlighting the onset of nonlinear distortions at high power levels.

It should be noted that these results are based solely on simulations of the complete DPA, while only the resonators have been experimentally validated. Full DPA measurements and additional linearity tests remain to be performed. Despite these limitations, the proposed design demonstrates the potential of CRLH-based harmonic control to improve efficiency and maintain spectral purity in broadband applications. The simulated DPA operates over a wide frequency band of 1.8–2.5 GHz, which meets the requirements of modern wireless applications. From a design perspective, the metamaterial-based harmonic control simplifies the suppression of higher-order harmonics while enabling effective load modulation, which could facilitate future integration with DPD techniques or higher-order Doherty architectures. Future work will focus on full experimental validation, exploring multiband operation for massive MIMO systems, and optimizing the integration of advanced linearization and broadband control strategies to meet emerging 5G and beyond communication standards.

Finally, this design demonstrates a significant impact for sub-6 GHz 5G base stations. It combines high efficiency, good linearity, and compactness, facilitating integration into existing infrastructures. Moreover, the precision of harmonic suppression and the overall simulated performance of the DPA ensure high-quality transmission across the entire operating band, thereby demonstrating the practical relevance of this approach for next-generation wireless systems.

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AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Faycal El Hardouzi	✓	✓	✓	✓	✓		✓	✓	✓	✓				
Mohammed Lahsaini	✓	✓						✓	✓		✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study, in accordance with legal and ethical requirements for privacy protection.

ETHICAL APPROVAL

This research does not involve human subjects and therefore does not require approval from an ethics committee.

DATA AVAILABILITY

The data availability statement is a valuable link between a paper's results and the supporting Data availability is not applicable to this manuscript, as no new data were created or separately analyzed for this study. The results are available within the article and/or its figures.

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