TELKOMNIKA, Vol.14, No.2, June 2016, pp. 497~506
ISSN: 1693-6930, accredited A by DIKTI, Decree No: 58/DIKTI/Kep/2013
DOI: 10.12928/TELKOMNIKA.v14i1.3042

State-space Modelling and Digital Controller Design for DC-DC Converter

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Abstract

The recent development in digital technology offers better platform for easy implementation of advance control algorithm in power converter design making digital control a viable alternative to analogue counterpart. Controller design for power converters has been very challenging due to non-linear characteristics of power switches, the supply voltage variability, load current changes and circuit element variation. This paper presents dynamic averaged state-space modelling of non-ideal dc-dc boost converter with parasitic and digital controller design for boost converter using digital redesign and direct digital design methods. The system was simulated in Matlab/Simulink to investigate the dynamic performance of the two controllers' transient response, control bandwidth and response to variable supply voltage. The results demonstrated fast transient and wide control bandwidth for tight voltage regulation to variable input voltage.

Keywords: *dc-dc converter, state-space model, digital compensator, closed loop response, control bandwidth*

1. Introduction

Power converters found their applications in nearly all electrical gadgets by providing necessary power conversion and power quality improvement for smooth operations. Power converters also plays important role in renewable energy systems by providing necessary control in stabilizing the variable generated output [1]. The generations from renewable energy resources are characterized by changing dynamics with varying output voltage, current, frequency and power which demands advance control schemes to fully tap their potentials [2, 3]. Increasing electronics interface has contributed immensely to small and large scale renewable energy deployment by providing better conditioning with improve efficiency and diverse suitability for wide range of load application.

The switch mode converter topologies are widely used in energy conversion applications owing to the advantage high efficiency. The converter topology is an arrangement of power switching devices and the magnetic elements which forms the power module. In addition to the power circuit, there is a control unit responsible for power flow regulation to meet the output voltage requirement. The controller design has been very challenging due to non-linear nature of power switching elements, variation of supply voltage and load current [4-6]. The implementation the control unit is achievable via analogue or digital control integrated circuit. The analogue technique has been widely used till recent time due to its design simplicity and high control bandwidth [7-9]. The technique has disadvantages of large number parts, complex hardware configuration, and sensitivity to environment in terms of thermal and ageing [10, 11]. Recently, the interest in digital control of power converter is gaining popularity, credit to high speed microcontrollers and digital signal processor with less power consumption at low cost [12]. Digital control system are less sensitivity to parametric variation, monitoring and auto diagnosing in operation are possible, flexible as they can be reprogram to different function and complexity of control is moved from hardware to software [12, 13].

This paper presents design and analysis of digital controller for dc-dc boost converter using both digital redesign and direct digital design approaches. A non-ideal boost converter was modelled using averaged state-space techniques which are prerequisite to effective controller design. The model took in to consideration the parasitic parameters of circuit elements

Received November 15, 2015; Revised April 22, 2016; Accepted May 3, 2016

in order to obtain improved dynamic model for effective controller design. The digital controllers are designed using the direct digital design and digital redesign approach using the Matlab-SISO_tool control design tools. The effectiveness of the controllers on the boost converter demonstrated fast transient response with improves dynamic performance necessary for eliminating voltage fluctuations associated to highly variable voltage source like solar photovoltaic system.

2. Design and Modelling of Boost Converter

A DC-DC boost converter is a non-isolation power converter that produces output voltage larger than the input voltage. Figure 1 shows the power circuit module and the controller unit which can be implemented using digital signal controller (DSC). The two basic control methods are the voltage and current control mode. The voltage mode control is a single loop control system with only output voltage used as control signal, while current control mode is a multi-loop control with inner current feedback loop in addition to the outer voltage feedback [5, 14]. The schematic of the boost converter shown in Figure 1 is a voltage mode control, the output voltage (V_0) which serves as feedback is sensed by opt-isolator (H) and transformed to discrete values via analogue to digital converter (ADC). The sensed voltage is compared with the desired reference voltage (V_{ref}) to generate error signal(e). The error is then processed by a compensator block to determine the duty cycle of pulse width modulation (PWM) which controls the converter switching *'on'* and *'off'* period.

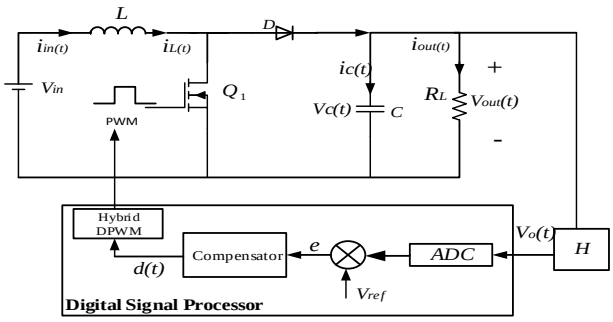

Figure 1. Boost converter with digital controller

2.1. Steady State Design

To study the dynamic behaviour of dc-dc boost converter with respect to the digital controllers, the steady state and dynamic modelling for continuous current mode (CCM) operation of non-ideal boost converter are presented in sub-section 2.1 and 2.2. Table 1 shows the summary of the steady state design example used as case study in the project.

Table 1. Steady state parameters

Parameters	Symbol	Value
Input voltage	V_{in}	12 [V]
Output voltage	V_{out}	48 [V]
Output voltage ripple	ΔV_o	500 [mV]
Rated power	P_o	500 [W]
Average output current	I_o	9.6 [A]
Switch on resistance	R_{on}	0.1 [Ω]
Parasitic inductor resistance	r_L	0.01 [Ω]
Parasitic capacitor resistance	r_C	0.01 [Ω]
Load resistance	R_L	5 [Ω]
Duty cycle	d	0.75
Inductor	L	90 [μH]
Output capacitor	C	100 [μF]
Switching frequency	f_s	100 [kHz]

The details of the steady state design equations for dc-dc boost converters have been presented in [4-6]. A 500W, 48V boost converter was design with 12V nominal input and ± 50% input variation. The switching frequency of pulse width switching control is 100 kHz to ensure high power density by reducing filter component size and the load was modelled as resistance. The *on* resistance of the power switch, the internal resistance of filter inductor and capacitor equivalent resistance were all considered for improved modelling and analysis of the boost converter.

2.2. Dynamic State Model

Switching converter is a periodic time-variant system that can be modelled using circuit averaging or state space averaging technique [6]. The dynamic models of converters are useful for controller design, predicting the system stability margin, and for studying transient response to supply/load perturbation [6]. It helps to predict dynamic behaviour of the converter prior to system prototyping to reduce design cycle time and cost. The state space average model method is used to model the non-ideal boost converter considering components parasitic parameters [15, 16]. This modelling technique gives a complete converter model with both steady state (DC) and dynamic (AC) quantities and the transfer functions of the converter are readily obtainable for dynamic analysis of the system.

Based on block diagram in Figure 1, the switching period for complete cycle is denoted is $T = 1/f_s$ and d is the duty cycle. The switch total *on*-time is $t_{on} = dT$ and *off*-time is $t_{off} = (1-d)T$. When switch Q_1 is *on* at time interval dT, by applying KVL and KCL, the differential state variables for boost the converter are derived as follows:

$$\frac{di_L(t)}{dt} = \frac{V_{in}(t)}{L} - i_L(t)\frac{(R_{on} + r_L)}{L} \tag{1}$$

$$V_{out}(t) = V_c(t)\frac{R_L}{R_L + r_c} \tag{2}$$

$$\frac{dVc(t)}{dt} = -\frac{Vc(t)}{C(R_L + r_c)} \tag{3}$$

The state space representation for the *on*-state is:

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dV_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_{on}+r_L)}{L} & 0 \\ 0 & -\frac{1}{C(R_L+r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in}(t) \tag{4}$$

$$\left[V_{out}(t)\right] = \begin{bmatrix} 0 & \frac{R_L}{(R_L + r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ V_c(t) \end{bmatrix} \tag{5}$$

Similarly, when switch Q_1 is in *of*-state at time interval $(1-D)T$, applying KVL and KCL, the differential state variables for boost the converter are derived as follows:

$$L\frac{di_L(t)}{dt} = V_{in}(t) - i_L(t)r_L - V_{out}(t) \tag{6}$$

$$V_{out}(t) = V_c(t)\frac{R_L}{R_L + r_c} + i_L(t)R_L//\mathrm{r_c} \tag{7}$$

$$\frac{di_L(t)}{dt} = \frac{V_{in}(t)}{L} - i_L(t)\frac{(r_L + R_L//r_c)}{L} - V_c(t)\frac{R_L}{(R_L + r_c)L} \quad (8)$$

$$i_c(t) = i_L(t) - i_{out}(t) \quad (9)$$

$$\frac{dVc(t)}{dt} = -\frac{R_L)}{C(R_L + r_c)}i_L(t) - \frac{V_c(t)}{C(R_L + r_c)} \quad (10)$$

The state space representation for the *off* state is:

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dVc(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L + R_L//r_c}{L} & \frac{-R_L}{L(R_L + r_c)} \\ \frac{R_L}{C(R_L + r_c)} & -\frac{1}{C(R_L + r_C)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ \\ V_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in}(t) \quad (11)$$

$$\left[V_{out}(t)\right] = \begin{bmatrix} R_L // r_c & \frac{R_L}{(R_L + r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ \\ V_c(t) \end{bmatrix} \quad (12)$$

For dynamic state analysis and controller design for the boost converter, the converter continuous-time transfer function $G(s)$ is obtained by performing state averaging on the state equations using the duty cycle d as weighting factor. The averaged state space equations for a converter are given by (13) and (14) [3], [17-18].

$$\dot{x}(t) = \overline{A}x(t) + \overline{B}u(t) \quad (13)$$

$$y(t) = \overline{C}x(t) \quad (14)$$

Where, the state averaged matrix are defined as $\overline{A} = A_1 d + A_2(1-d)$, $\overline{B} = B_1 d + B_2(1-d)$ and $\overline{C} = C_1 d + C_2(1-d)$. The term $x(t)$ is the converter DC state vector defined as inductors currents and capacitors voltages, $u(t)$ is converter DC input vector and $y(t)$ is the converter DC output vector.

The averaged matrix based on steady state parameters in Table 1 is derived as:

$$\overline{A} = A_1 d + A_2(1-d) \quad (15)$$

$$\overline{A} = \begin{bmatrix} -972.17 & -2772.23 \\ \\ 2495.01 & -1996.23 \end{bmatrix} \quad (16)$$

$$\overline{B} = B_1 d + B_2(1-d) \quad (17)$$

$$\overline{B} = \begin{bmatrix} 11111.1 \\ \\ 0 \end{bmatrix} \quad (18)$$

$$\overline{C} = C_1 d + C_2 (1-d) \tag{19}$$

$$\overline{C} = \begin{bmatrix} 0.002495 & 0.9985 \end{bmatrix} \tag{20}$$

Using the Matlab state-space (*ss*) to transfer-function (*tf*), the converter control to output continuous-time transfer function is obtained as (21):

$$G(s) = \frac{27.72s + 2.774e^{07}}{s^2 + 2968s + 8.857e^{06}} \tag{21}$$

3. Digital Compensator Design

The two approaches for designing digital controller are the digital redesign approach known as design by emulation and direct digital design approach [6, 17]. Design by emulation employs control design in the continuous time *s*-domain and then transformed to discrete/digital *z*-domain using any of the discretization methods such as backward Euler, bilinear and pole/zero matching (Equation 22-25) [3, 6]. Digital redesign method provides good response using well known continuous-time analogue design method but suffers from discretization delay effects.

The alternative approach is the direct digital design where digital controller design is done directly in *z*-domain. A switching action of a converter is considered and treated as a sampled-data system leading to a discrete-time model [6]. This approach provides good transient response with better phase margin and control bandwidth [18].

$$BackEuler: s = \frac{1-z^1}{T_{samp}} \tag{22}$$

$$Bilinear: s = \frac{2}{T_{samp}} \frac{1-z^{-1}}{1+z^{-1}} \tag{23}$$

$$Polezero\,Matching: \quad s + a = 1 - z^{-1} e^{-aT_{samp}} \tag{24}$$

$$s \pm ja = 1 - 2z^{-1} e^{-aT_{samp}} \cos bT_{samp} + z^{-2} e^{-2aT_{samp}} \tag{25}$$

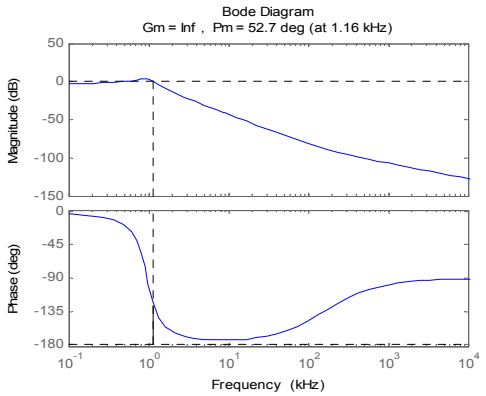

Figure 4. Converter bode-plot with unity feedback

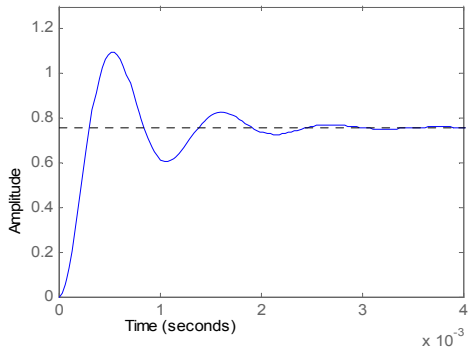

Figure 5. Converter step response with unity feedback

In order to predict the closed-loop stability of the converter, the closed-loop frequency and step response with unity feedback is presented in Figure 4 and Figure 5 respectively. The bode-plot has infinite gain margin (GM), 52.7º phase margin (PM) at 1.16 kHz crossover frequency. The closed loop step response shows that the system is under damped with some oscillations. It has steady state error with settling time of 3ms and about 44% overshoot.

3.1. Digital Redesign Controller

A proportional-derivative (PD) controller is first design in continuous time domain using the system Ziegler Nichol frequency response approach as detailed in [19, 20]. The controller design specification is set at 10% overshoot, 23 kHz gain cross-over frequency and phase margin of greater than 60º. The designed controller is further fine-tuned in the Matlab_SISO tool environment via frequency bode plot and then discretized using bilinear (Tustin) discretization method. The Tustin approximation method has the advantage of good matching between the continuous and discrete time models in the frequency domain [18].

The continuous-time transfer functions of the designed controller $C(s)$:

$$C(s) = 79.733 \times \frac{1 + 6.6e^{-05}s}{1 + 1e^{-06}s} \tag{26}$$

The equivalent digital controller in discrete-time domain $C(z)$ is obtained at sampling time of 5μ seconds.

$$C(z) = \frac{U(z)}{e(z)} = \frac{1560z - 1447}{z + 0.4286} \tag{27}$$

The equivalent difference equation of the controller can be written as:

$$U(k) = -0.4286U(k-1) + 1560e(k) - 1447e(k-1) \tag{28}$$

3.2. Direct Digital Design Controller

The plant (boost converter) is first discretized to *z*-domain using zero hold order (ZHO) at sampling period of 5μ second. The digital controller is then designed in (pseudo-continuous) *w-plane* using the same Ziegler Nichol frequency response approach as in digital redesign approach which is later transform back equivalent *z*-domain [18, 21].

The discrete-time transfer function of the plant is obtained as:

$$G(z) = \frac{0.0004826\ z + 0.0002058}{z^2 - 1.985\,z + 0.9853} \tag{29}$$

With trapezoidal rule, the plant transfer function is transformed to pseudo-continuous domain, *w-plane* as presented in (38).

$$G(w) = \frac{-6.973\,e^{-5}w^2 - 41.46\,w + 2.774\,e^{7}}{w^2 + 2968\ w + 8.857\,e^{6}} \tag{30}$$

The controller is then designed in *w-plan* which results in (39):

$$C(w) = \frac{0.004955\ \ w + 75.07}{1e^{-6}w + 1} \tag{31}$$

The digital equivalent of the controller transfer function in *z-plane* is obtained as:

$$C(z) = \frac{U(z)}{e(z)} = \frac{1469\ z - 1362}{z + 0.4286} \tag{32}$$

The difference equation of the controller can be written as:

$$U(k) = -0.4286U(k-1) + 1469e(k) - 1362e(k-1) \quad (33)$$

4. Results and Discussions

4.1. Digital Redesign Controller (DRC) Response

The step and frequency response of the closed loop performance of digital redesign controller (DRC) on the boost converter are presented in Figure 6 and Figure 7. The step response plots of the system shows that the system is able to achieve rise time of 15μs and settling time of 200μs with 6% overshoot. The closed loop phase margin is 157º with and control bandwidth of 9.49 kHz.

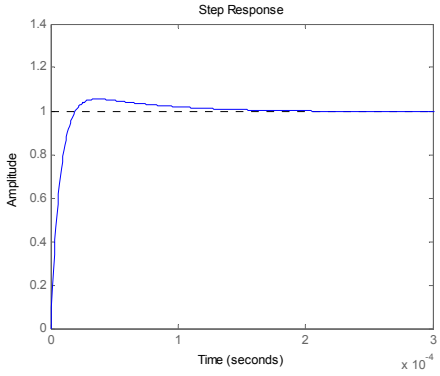

Figure 6. Closed loop step response with DRC

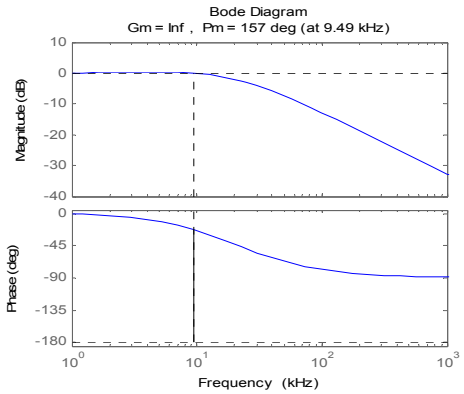

Figure 7. Closed loop bode-plot with DRC

4.2. Direct Digital Controller (DDC) Response

From the closed loop step and bode-plot of the boost converter with direct digital controller (DDC) in Figure 8 and Figure 9 respectively. This controller has an improved rise time of 10μs with settling time of 160μs and 7% overshoot. The phase margin of the frequency response is 138º with an improved control bandwidth of 16.5 kHz frequency and a gain margin of 5.55dB.

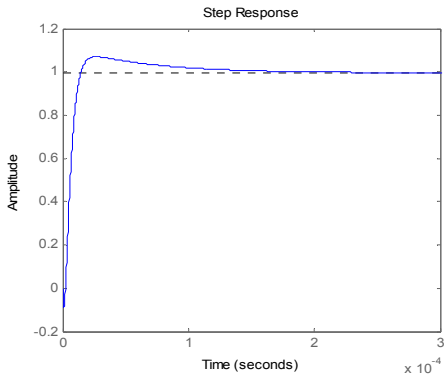

Figure 8. Closed loop step response with DDC

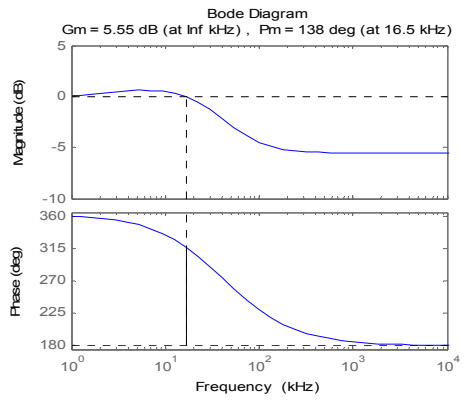

Figure 9. Closed loop bode-plot with DDC

Presented in Table 2 is the summary of the time and frequency response of the two controllers, digital redesign and direct digital controller. The controller's response shows that there were improvements in the converter start up transient by reducing settling time and

response overshoot. The settling time of the digital redesign and direct digital controllers are 200μs and 160 μs respectively as against that converter response with unity feedback having 13ms settling time. The direct digital controller has a faster transient as compared with that of digital redesign controller though with slightly higher overshoot which satisfied the design requirement of 10% maximum overshoot. Direct digital controller control bandwidth of 16.5 kHz against 9.5 kHz of digital redesign controller and also a phase margin of 157º as compared to 138º of digital redesign controller. The comparison of the two digital controller parametric response shows that the direct digital controller produced a better control action with faster transient and higher control bandwidth for tighter output voltage regulation in converter control as compared with digital redesign approach.

Table 2. Summary on closed loop frequency and time response

Design approach	Digital redesign (DRC)	Direct digital design (DDC)
Time response		
Rise time	15μs	10μs
Settling time	200μs	160μs
Over shoot	6%	7%
Frequency response		
Control bandwidth	9.49kHz	16.5kHz
Gain margin	Infinite	5.55 dB
Phase margin	157º	138º

4.3. Matlab-Simulink Implementation

The open loop simulation of the converter is implemented in Simulink environment based on the converter designed example with steady state parameters presented in Table 1. The converter response to variable input voltage varied from 12V nominal to 18V is shown in Figure 10.

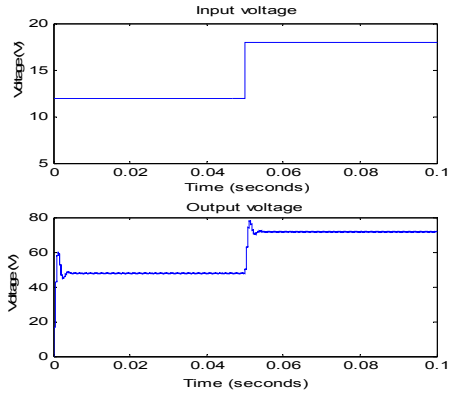

Figure 10. Converter open loop input-output voltage

To verify the system closed loop performance, the designed controllers with the boost converter was implemented in Simulink as presented in the Figure 11 and Figure 12 for both digital redesign controller (DRC) and direct digital controller (DDC) respectively.

The output response presented in Figure 13 and Figure 14 shows that the output voltage of the converter is 48V with nominal 12V supply and remains constant and bumpless after 50ms when the input voltage is increased by 50% from 12V to 18V. This shows the robustness of the two designed controllers to supply voltage variability.

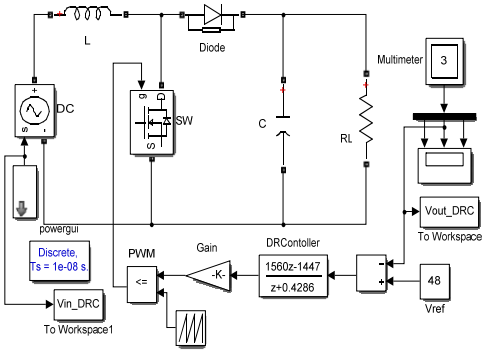

Figure 11. Converter closed loop with DRC

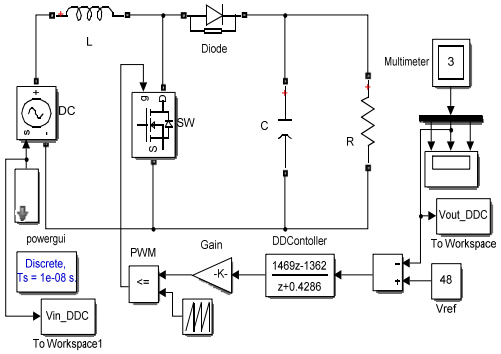

Figure 12. Converter closed loop with DDC

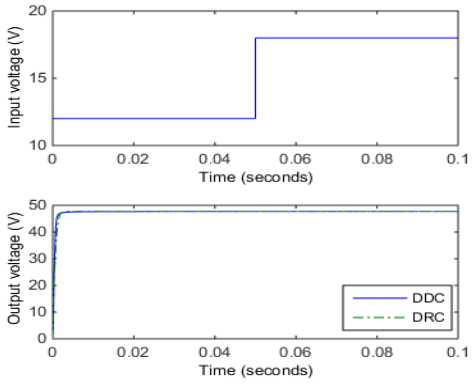

Figure 13. Converter response to variable supply voltage

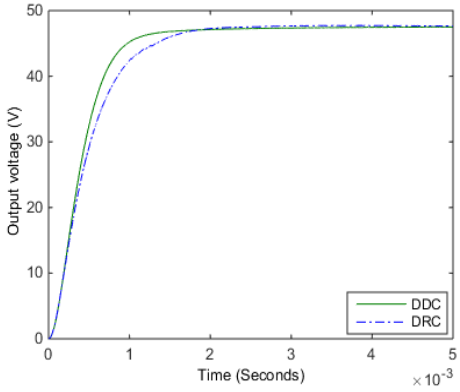

Figure 14. Converter transient response with DRC & DDC

5. Conclusion

A non-ideal DC-DC boost converter has been modelled and digital controller was designed using digital redesign and direct digital design approaches. The system step response of the controllers shows that the direct digital design controller has fastest transient and higher control bandwidth as compared with the digital redesign approach. The direct digital controller exhibited better dynamic performance with fastest transient with higher control bandwidth of 16.5 kHz against 9.5 kHz of digital redesign controller. The closed loop implementation of the controllers were able to give constant output voltage to variable input voltage even when the input voltage was increased by 50% from the 12V nominal to 18V.

References

[1] S Chakraborty, MG Simões, WE Kramer. *Power Electronics for Renewable and Distributed Energy Systems*. Springer. 2013.
[2] JM Carrasco, LG Franquelo, JT Bialasiewicz, E Galván, RP Guisado, MA Prats, et al. Power-electronic systems for the grid integration of renewable energy sources: A survey. *Industrial Electronics, IEEE Transactions on.* 2006; 53: 1002-1016.
[3] O Ibrahim, N Yahaya, N Saad, K Ahmed. *Design and Analysis of a Digital Controller for Boost Converter with Renewable Energy Sources for Domestic DC Load.* In Applied Mechanics and Materials. 2015: 141-145.
[4] M Rashid, C Press. Power Electronics Handbook. *Devices, Circuits, and Applications*. 2010.
[5] N Kularatna. *Power electronics design handbook: low-power components and applications*. Newnes. 1998.
[6] S Ang, A Oliva. Power-switching converters. CRC press. 2005.

[7] HH Park, GH Cho. A DC–DC Converter for a Fully Integrated PID Compensator With a Single Capacitor. *Circuits and Systems II: Express Briefs, IEEE Transactions on.* 2014; 61: 629-633.
[8] S Kapat, PT Krein. Formulation of pid control for dc–dc converters based on capacitor current: A geometric context. *Power Electronics, IEEE Transactions on.* 2012; 27: 1424-1432.
[9] YI Son, IH Kim. Complementary PID controller to passivity-based nonlinear control of boost converters with inductor resistance. *Control Systems Technology, IEEE Transactions on.* 2012; 20: 826-834.
[10] L Balogh. A practical introduction to digital power supply control. *Texas Instruments Incorporated.* 2005: 6-1.
[11] C Buccella, C Cecati, H Latafat. Digital control of power converters-A survey. *Industrial Informatics, IEEE Transactions on.* 2012; 8: 437-447.
[12] YF Liu, P Sen. *Digital control of switching power converters.* In Control Applications, 2005. CCA 2005. Proceedings of 2005 IEEE Conference on. 2005: 635-640.
[13] A Prodic, D Maksimovic. *Design of a digital PID regulator based on look-up tables for control of high-frequency DC-DC converters.* In Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on, 2002: 18-22.
[14] S Saggini, E Orietti, P Mattavelli, A Pizzutelli, A Bianco. *Fully-digital hysteretic voltage-mode control for dc-dc converters based on asynchronous sampling*. In Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE. 2008: 503-509.
[15] C Nwosu, M Eng. State-Space Averaged Modeling of a Nonideal Boost Converter. *The pacific journal of science and Technology.* 2008; 9: 302.
[16] V Jha, P Rai. State Space Averaged Modeling of Basic Converter Topologies. *VSRD International Journal of Electrical, Electronics & Communication Engineering.* 2012; 2: 566-575.
[17] A Prodic, D Maksimovic, RW Erickson. *Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter.* In Industrial Electronics Society, 2001. IECON'01. The 27th Annual Conference of the IEEE. 2001: 893-898.
[18] Y Duan, K Jin. *Digital controller design for switchmode power converters.* In Applied Power Electronics Conference and Exposition, 1999. APEC'99. Fourteenth Annual. 1999: 967-973.
[19] KJ Aström, T Hägglund. PID controllers: theory, design and tuning. 1995.
[20] KJ Åström, T Hägglund. *Advanced PID control*: *ISA-The Instrumentatio*n. *Systems, and Automation Society*. Research Triangle Park, NC. 2006.
[21] GF Franklin, JD Powell, A Emami-Naeini. Feedback control of dynamics systems. MA: Addison-Wesley, Reading. 1994.