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Editorial

High-Speed Computation using FPGA for Excellent Performance of Direct Torque Control of Induction Machines

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Abstract

The major problems in hysteresis-based DTC are high torque ripple and variable switching frequency. In order to minimize the torque ripple, high sampling time and fast digital realization should be applied. The high sampling and fast digital realization time can be achieved by utilizing high-speed processor where the operation of the discrete hysteresis regulator is becoming similar to the operation of analog-based comparator. This can be achieved by utilizing field programmable gate array (FPGA) which can perform a sampling at a very high speed, compared to the fact that developing an ASIC chip is expensive and laborious.

Keywords: ASIC, direct torque control, FPGA, torque ripple, variable switching frequency

The significances of having a high control bandwidth with high sampling frequency in algorithm computation are to provide a quick instantaneous response, improved linearity and accuracy of control systems. In the case of the hysteresis torque controller for the Direct Torque Control (DTC) drive system, the sufficient number of sampling is needed for controlling the torque in a hysteresis band. This is to ensure proper restriction and regulation of torque with the hysteresis bandwidth [1]. Ideally, the output torque ripple can be minimized by reducing the width of the hysteresis band of the comparator. However, in practice with the use of Digital Signal Processor (DSP), this cannot be accomplished due to insufficient sampling frequency. One way to overcome this problem is to apply a Field Programmable Gate Array (FPGA) which can perform the computation of control algorithm at high rate [2-4].

The potential of poor linearity and accuracy, particularly in complex calculations can be minimized using a high-speed digital signal processor (DSP) or field programmable gate array (FPGA). DSP and FPGA are two common controller boards used in executing control algorithms of electrical and power electronic drives. DSP is preferable to be employed for executing control algorithm which involves trigonometric functions, complex numbers and vectors. FPGA is known as lower cost controller board, however the execution of control algorithm which is written using a machine code (i.e. VHDL and Verilog) is highly complex. FPGA is also known as an integrated circuit which is electronically field-programmed hardware to execute any function. Unlike DSP, FPGA supports parallel computing, so different task operations do not have to compete for the same resources. Each operation is assigned to a devoted section and can function independently, without any influence from other logic blocks. Thus, the performance of one part of the application is not affected when other task operation is added. In contrast, DSP follows the paradigm of sequential execution, share the resource and hence the performance of one task operation affects other operation too [5-6].

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In such operation, FPGA provides some advantages such as flexibility in arranging components and additional functions. The current FPGA technologies allow for the integration of soft-core processors, as well as realization of several processors simultaneously. Furthermore, the designer can apply many ready-to-use components which are well-known as intellectual properties (IP). The usage of IP-cores reduces the development works and thus may contribute for reducing costs [5-7].

Figure 1 illustrates the occurrence of undershoots for two different sampling periods T_{s1} and T_{s2} (where $T_{s1} < T_{s2}$). If the sampling is too large the torque error may touch the lower band and causing the reverse voltage vectors to be selected [8-12]. Selection of these reverse voltage vectors causes the unnecessary increment in the torque ripple. Torque hysteresis comparator switching usually governs the VSI switching frequency. This can be illustrated by the discretized electromagnetic torque waveforms that operate under different steady-state conditions as shown in Figure 2.

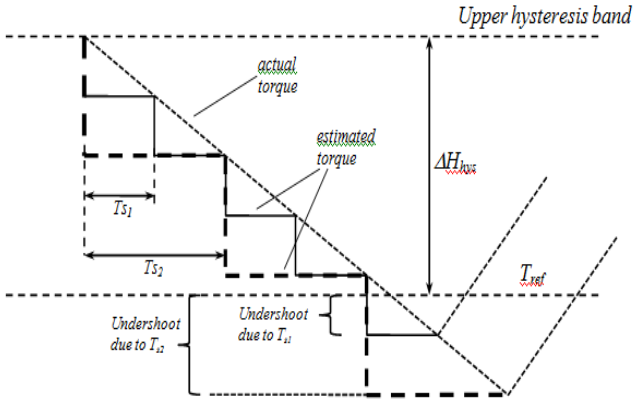

Figure 1. The occurrence of undershoots for two different sampling periods T_{s1} and T_{s2} (where $T_{s1} < T_{s2}$).

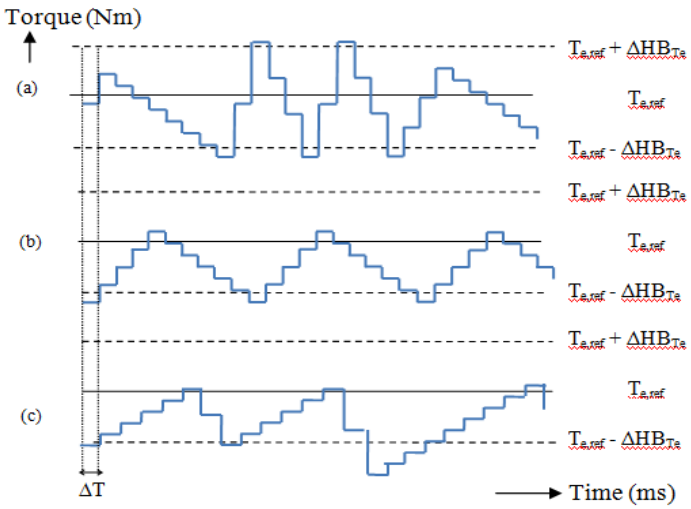

Figure 2. An illustration of processor with variable speed, that is, (a) low, (b) middle and (c) high speed

This figure shows the torque waveforms with the sampling time, ΔT, at three different operating speeds, i.e. low-, middle- and high-speed. The voltage vectors are selected at every sampling period ΔT based on the comparison between the reference and calculated torque,

which is also calculated for every sampling period. If the sampling period is too large, the torque waveform exceeds the band and thus causes the selections of inappropriate voltage vectors. Since the positive slope of the torque is too steep, the sampling period is not small enough to avoid the torque waveform from touching the upper hysteresis band. This incident can be avoided by reducing the sampling period.

The small sampling period can be achieved by utilizing high-speed processor where the operation of the discrete hysteresis regulator is becoming similar to the operation of analog-based comparator. The high-speed processor is always referred to the use of FPGA, in which the computation of control algorithm can be performed at very minimum sampling time, i.e. in nano-second. From Figure 2, it is clear that the rapid torque reduction due to the selection of reverse voltage vector can be avoided if the sampling time is greatly reduced using FPGA.

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