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FPGA-based Digital Baseband Transmission System Performance Tester Research and Design

Huimin Duan* , Juanjuan Gu , Guohua Hu , and Qian Zhang
Hefei University
No.99 jinxiu Avenue, Hefei, Anhui Province, China. +86-551-62158571
*Corresponding author, email: 123667426@qq.com, duan@hfuu.edu.cn

Abstract

Communication System Transmission Performance Tester, as a digital communication system design and testing equipment, plays an important role in the construction and daily maintenance of the communication system. The paper presents a kind of tester, which is designed using Cyclone IV FPGA (Field Programmable Gata Array) and VHDL (Very High Speed Integrated Circuits Hardware Description Language). According to the features in the eye diagram, the system performance can intuitively and qualitatively evaluated. The results prove that the system accurately displayed the eye diagram, thereby reflected the performance of the baseband transmission system truthfully.

Keyword: *communication system,transmission performance,FPGA, bit synchronization,eye diagram*

1. Introduction

With the development of communication technology, communication systems are becoming increasingly complicated. Accurate quantitative analysis of the performance of an actual baseband transmission system is tedious and complicated or even impossible[1]. Especially in the debugging and maintenance procedures, system performance may be varied in any time, a simple method to qualitatively monitoring the system performance is then more needed [2, 3]. Communication system transmission performance tester plays an important role in this field.

FPGA (Field Programmable Gata Array) technology has features such as the flexible architecture and logic unit, high integration and a wide scope of applicability[4, 5, 6]. Apply it to the traditional tester, we can achieve the following benefits: improving the accuracy of the testing eye diagram., expanding the analytical bandwidth of the system, increasing the anti-interference and improving the efficiency of real-time execution[7].

2. Overall Design

As shown in the Figure 1,the system mainly consists of four modules: the transmitter, the channel, the noise source, the receiver. Based on FPGA, the transmitter produces a level-four and a level-twelve pseudo-random sequences, which are then be transmitted used to be information source and channel noise. In the channel part, there are three kinds of LPF (Low Pass Filter) with three different cutoff frequencies which can be used to simulate the channel with different bandwidths[8]. At the receiving end, the received signal is applied as the input signal of the oscilloscope, while the bit synchronous clock is used as the scanning synchronizing signal, an eye diagram is then obtained[9].

The bit synchronous clock is a very important issue in digital communication systems. Only to extract the correct timing pulses, the receiver can obtain the steady eye diagrams, then makes accurately sampling decision and recovers the digital baseband signals. It directly affects the overall performance of the entire digital communications system[2, 3]. In this study, we use DPLL method to extract bit synchronous clock signal.

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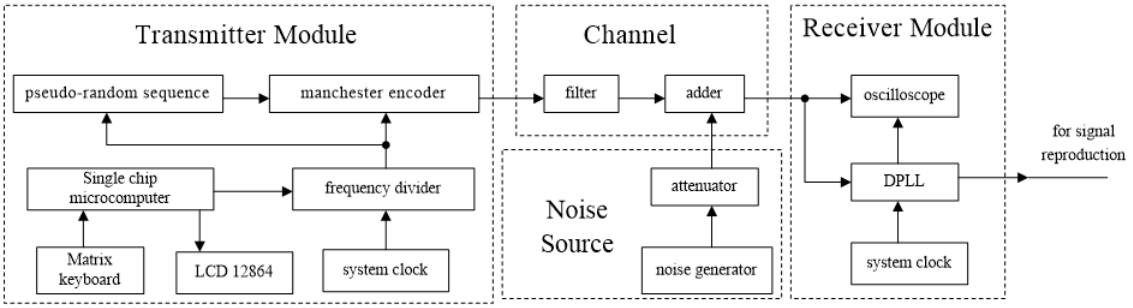


Figure 1. Diagram of system design

3. Research Method

3.1. Pseudo-random sequence and Manchester coding module

Based on FPGA, according to formula (1),the circuit of these two modules is designed using VHDL, and its simulation results are shown in Figure 2[10], [11].

$$f(x) = (1 + x^3 + x^4) \tag{1}$$

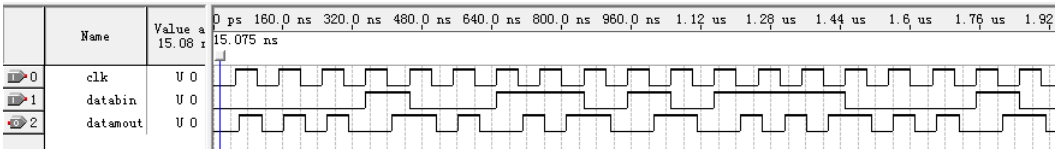


Figure 2. Results of pseudo-random sequence and Manchester coding module

In the picture: clk is the working clock; datain is the pseudo-random sequence output; datamout is the Manchester coding output.

3.2. Digital Phase-Locked Loop Module

This module is designed by using of VHDL and its top-level module is shown in Figure 3. It includes in total five sub-modules: a differential phase detector, an improved digital filter, bipolar clock source, controller, and frequency divider[9], [12]. Two of which are important and described below.

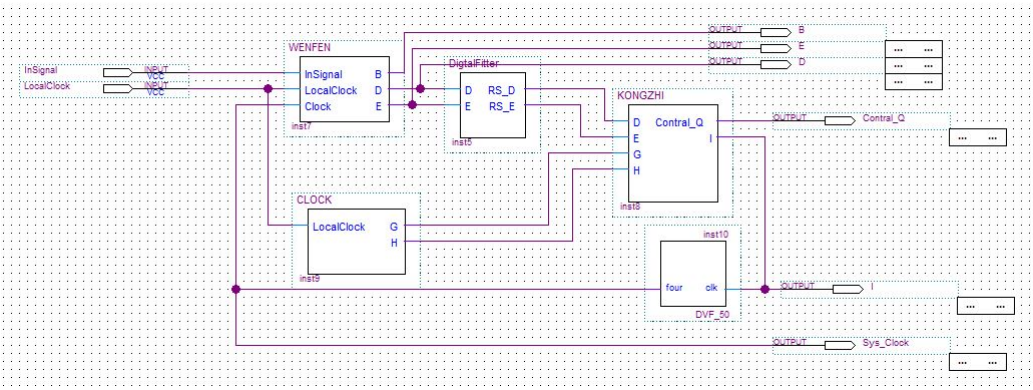


Figure 3. Scheme of digital PLL top-level module

3.2.1. Differential Phase Detector Module

Differential phase detector is composed of differential circui and a phase comparator circuit which consists of two AND gates, as shown in Figure 4.

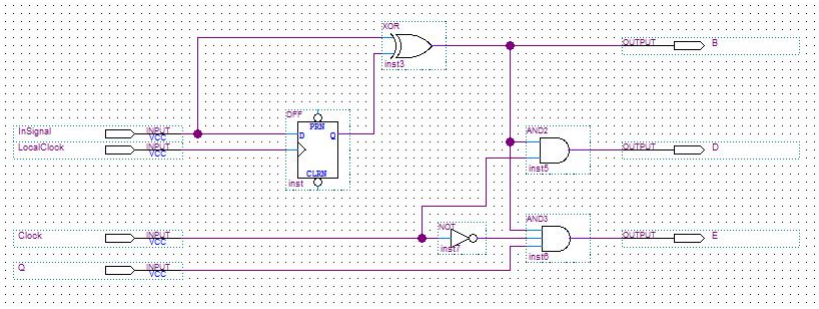


Figure 4. Scheme of differential phase detector

After the differential circuit, the input digital signal INSIGNAL (Manchester code) is output to B as the edge detection signal, corresponding to the input signal. Its simulation diagram is shown in Figure 5.

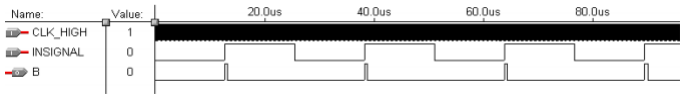


Figure 5. Simulation diagram of the edge detection signal

Edge detection signal B are respectively applied to two AND gates: the deduction gate AND2 and the addition gate AND3 (in Figure 4). If CLK is ahead of B, then AND3 is blocked, and AND2 sents a leading pulse D, as shown in Figure 6. If CLK lags behind B, deduction gate AND2 closed, addition gate AND3 then sents a lagging pulse E, as shown in Figure 7.

3.2.2. Controller Module

Implemented by CycloneIV FPGA, the controller module consists of deductions gate and addition gate. The opening and closing of the gates are controlled by Delay Flip-flops. The circuit diagram of the controller module is shown in Figure 8.

When comparing the local bit synchronous clock signal CLK to the edge detection signal B, the working status of the controller have four different situations:

(1) CLK ahead of B

As shown in Figure 9, G and H are bi-phase clock pulses. when the CLK is ahead of B, leading pulse D becomes positive pulse. At the rising edge of H, the level of the reverse control signal CONTRAL_Q changes from high to low, making that the deduction gate opens a trigger cycle and a pulse is deducted from G,thereby deducting a pulse to the bit synchronization signal I before the frequency dividing, and making that the phase of CLK is lagging by a period of H.

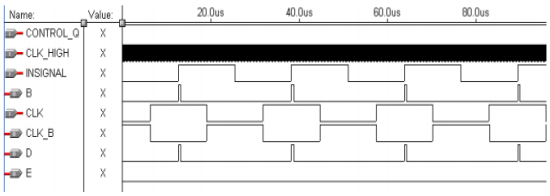


Figure 6. Simulation result of the leading pulse D

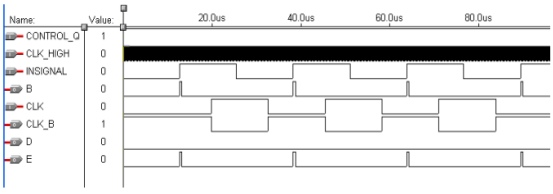


Figure 7. Simulation result of delaying pulse E

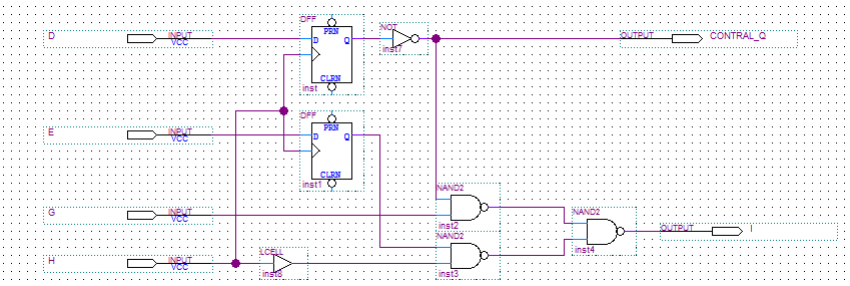


Figure 8. Simulation diagram of the control module

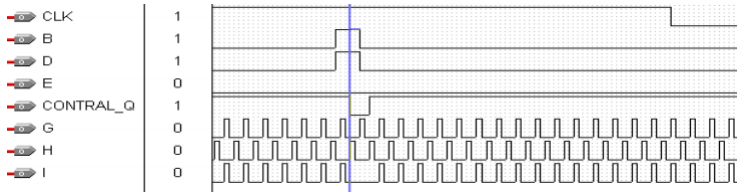


Figure 9. Simulation diagram when CLK ahead of B

(2) CLK lags behind B

As shown in Figure 10, when the CLK is lagging behind ”B, lagging pulse E becomes positive pulse. At the rising edge of ”H, the level of the reverse control signal CONTRAL_Q is unchanged, making that the addition gate opens a rigger cycle and a pulse is added to ”G, thereby adding a pulse to the bit synchronization signal I before the frequency dividing, and making that the phase of CLK is leading by a period of H.

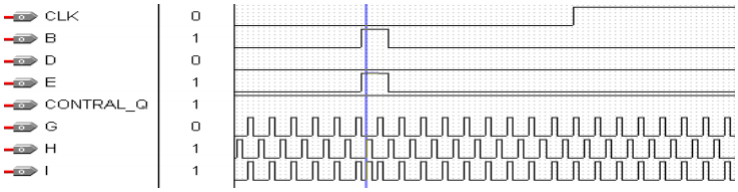


Figure 10. Simulation diagram when CLK lags behind B

(3) CLK synchronized with B

As shown in Figure 11, the lagging pulse SINNAL1 and the leading pulse SINGLA2 achieve dynamic equilibrium at the second half of the simulation diagram. As the edge detection pulse B has a fixed timewidth, when compared to the bit synchronization clock signal CLK, CLK’s jumping edge of lies in the middle of B”, therefore the leading pulse and the lagging pulse are observed alternatively. Deducting a pulse before the leading pulse is coming , adding a pulse before the lagging pulse is coming, the whole system is in a dynamic equilibrium status. This is the required bit synchronization status in this design.

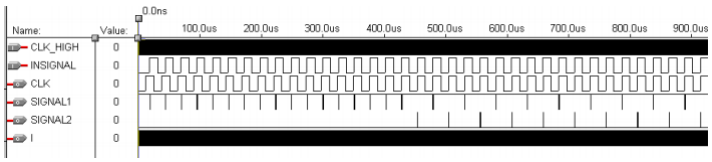


Figure 11. Simulation diagram when CLK synchronized with B

(4) CLK and B have reversed phase

When the descending edge of CLK is aligned to the rising edge of ”B, the input bit signal and the local synchronization clock have the reversed phase. At this time, the leading pulse D and the lagging pulse E are observed alternatively, making a false synchronization, the control module first deduct a pulse then add a pulse, making phase of CLK unchanged and not adjustable. To fix this, the control signal CONTRAL_Q is used here to avoid this situation, it functions as: turn off the addition gate if there is a ”D, so the control module is not able to generate addition pulse and the phase is able to be adjusted, therefore to solve the reversed phase problem of CLK and B.

3.3. Filter

The channel of baseband transmission system is equivalent to a LPF. In this design, we used four-order Butterworth LPF mode to design three filters with the upper cut-off frequencies of 100KHz, 200KHz, 500KHz, respectively[13], [14]. According to formula (2) and (3),the circuit diagram of a low-pass filter with cut-off frequency of 100KHz is shown in Figure 12.

$$A(j\omega) = \frac{A_0}{\sqrt{1+(\omega/\omega_c)^{2n}}} \tag{2}$$

$$\omega_c = \frac{1}{RC} \tag{3}$$

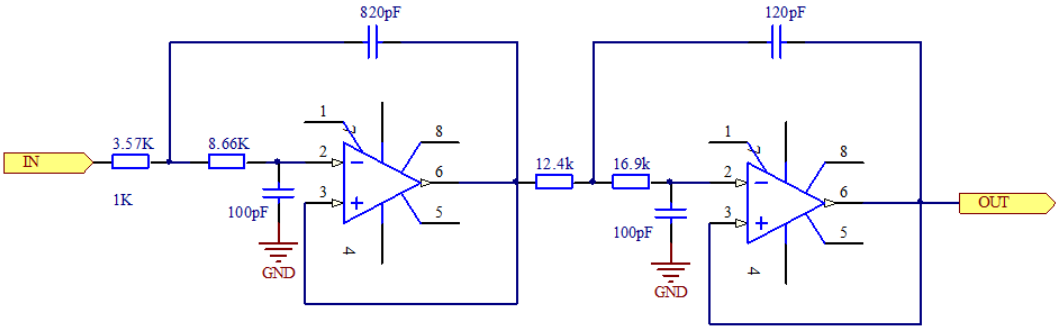


Figure 12. Scheme diagram of a low-pass filter with cut-off frequency of 100KHz

The filters with cut-off frequency of 200KHz and 500KHz are designed similarly as Figure 15, but only have difference in components parameters.

3.4. Addition module

A direct coupled amplifier is used in the addition circuit[15]. As the frequency of noise signal is 10MHz, so we used the THS3091 chip which has a gain-bandwidth product of 100MHz .The circuit as shown in Figure 13.

3.5. Attenuator

A -type attenuator network is used in this section. Adjustable resistance is used to change the input impedance to adjust the attenuation factor .Attenuator circuit as shown in Figure 14.

4. Result and Analysis

The received baseband signal is sent to Channel X of the oscilloscope,the bit synchronous clock is sent to Channel Y. Let the oscilloscope works in Channel Y trigger, then an eye diagram will appear on the screen of the oscilloscope[16]. Observation and analysis of the eye diagrams are as follows.

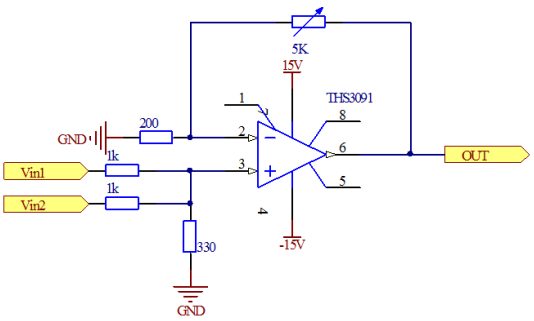


Figure 13. Circuit diagram of addition module

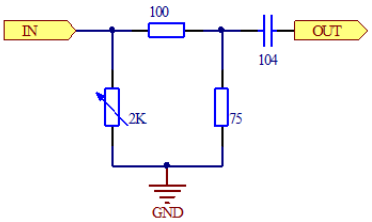


Figure 14. Circuit diagram of attenuator

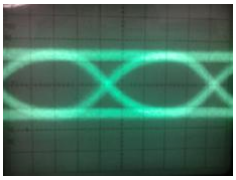
4.1. Same transmission system and different signal source

Testing condition : As shown in Table 1;Testing results : As shown in Table 2.

Table 1. Testing condition of same transmission system and different signal source

Name	condition
The signal source	f1=100Kbps, Vp-p=3.44V
Noise signal	f2=10Mbps, Vp-p=100mv
LPF cut-off frequency	Fo=100KHz

Table 2. Eye diagram with same transmission system and different signal source

Cut-off frequency	Before interference	After interference
100KHz		

According to the waveforms shown in Table 2, when the noise is introduced, the eye diagram becomes blurred. This result indicates that the eye diagram accurately reflects the problem during the signal transmission.

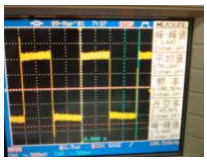
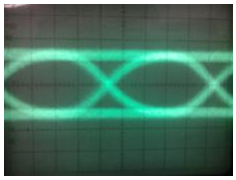
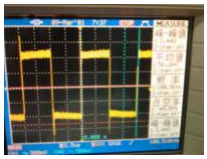
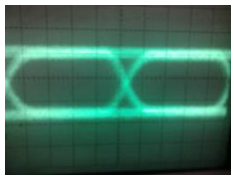
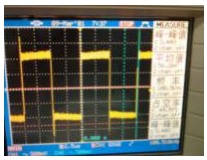
4.2. Different transmission system and same signal source

Testing condition : As shown in Table 3; Testing results : As shown in Table 4.

Table 3. Testing condition of different transmission system and same signal sourcel

Name	condition
The signal source	f1=100Kbps, Vp-p=3.44V
Noise signal	f2=10Mbps, Vp-p=100mv
LPF cut-off frequency	Fo=100KHz/200KHz/500KHz

Table 4. Eye diagram with different transmission system and same signal sourcel

Cut-off frequency	Signals from receiver (including noises)	Eye diagram
100KHz		
200KHz		
500KHz		

By comparing each eye diagram, it can be seen that: the eye diagram obtained with the 500KHz LPF has the widest opening and the largest slope of its hypotenuse; the eye diagram obtained with the 200KHz LPF has the median opening and the median slope of its hypotenuse; while the eye diagram obtained with the 100KHz LPF has the smallest opening and the smallest slope of its hypotenuse. Therefore when the optimal sampling time is selected in the moment that the eye diagram show a largest height of aperture, when a 500KHz transmission system is used, the SNR is maximum and is most sensitive to the timing error; while when a 100KHz transmission system is used, the SNR is minimum and is least sensitive to the sampling timing error.

Above test results show that, the eye diagrams obtained through the designed system, not only can truthfully reflect the noise caused interference to the signals, but also can accurately reflect the performance difference of different transmission systems[14]. Overall, the transmission performance tester can reflect the performance of the transmission system objectively.

5. Conclusion

In the research, the digital baseband transmission system performance tester makes use of the Cyclone IV FPGA and its built-in DPLL to generate and analyze the signals. The design improves the tester lock speed, the stability, reliability and flexibility, facilitating its maintenance and upgrades. The tests prove that the eye diagram can be displayed accurately, thereby truthfully reflected the performance of the baseband communication system.

In addition, through the eye diagram, we can easily obtain the amplitude distortion, zero distortion, noise tolerance, time sensitivity and other performance indicators[1,14].They can not only contribute to recovery of the baseband signal, but also can provide guidance for improve the transmission performance of the communication system.

6. Acknowledgement

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