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A Novel Multifunction Digital Chip Design Based on CMOS Technology

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Abstract

The realization of an analog-to-digital-conversion chip has great significance in the applications of electronic products. By considering mature time–number digitization, a new multifunction digital chip with a long time delay was designed in this study on the basis of the principle of analog-to-time conversion (ATC) and the realization of long time delay. With additional resistance, capacitance, and transistors, this chip can easily realize ATC, monostable triggers, Schmitt triggers, and multivibrators. The circuit composition of this chip was analyzed, and every module design was introduced. According to the simulation result of Hspice and CSMC 2P2M CMOS (Complementary Metal Oxide Semiconductor) process database, the chip layout (1mm^2) design was accomplished by using CSMC 2P2M CMOS technology. Finally, the designed chip was applied in multiproject wafer flow. The flow test demonstrated that this new chip can meet design goal and is applicable to various digital integrated chip designs as an IP (intellectual property) core.

Keywords: *CMOS technology, multifunction digital chip, layout design, MPW*

1. Introduction

The 555 timer is a chip with a monostable trigger, Schmitt trigger, and multivibrator. Given its flexible and convenient operation, the 555 timer is widely used in many fields, such as waveform generation and transformation, measurement and control, household appliances, and electronic toys. At present, the 555 timer chips available in the market are bipolar and CMOS (Complementary Metal Oxide Semiconductor) types. Both types of 555 timer chips apply a digital–analog hybrid integrated circuit, which is expensive. A cheap digital chip that can realize a long time delay is unavailable in the market. This study used CSMC 2P2M CMOS technology and designed a multifunction digital chip that can realize analog-to-time conversion (ATC), monostable trigger, Schmitt trigger, and multivibrator with additional resistance, capacitance, and transistors.

2. State of the Art

Analog-to-digital conversion (ADC) is a common interface chip in electronic products. Existing commercial ADC designs all involve analog–digital-mixed chips. Analog devices, including operational amplifiers, comparators, capacitors, and resistors, are used in existing ADC designs. The accuracy of reference voltage is important to comparator performance. Therefore, calibrations are difficult to conduct during the massive use of comparators. ADC development under single- and low-power consumptions should consider not only circuit structure and technological problems but also different analog designs, such as peripheral circuit and signal conditioning. Therefore, research on ADC has great significance. Corresponding research has been conducted successively in China and foreign countries. However, the direct designs of ADC remain restricted by digital–analog hybrids. In Reference [1], a hardware description language (HDL) was used to describe digital–analog hybrid circuits and realize an ADC design. However, the nature of the digital–analog hybrid technology of the chip remains unchanged, and the HDL for analog circuit still has no uniform standard and has not entered the commercial stage. The designed ADC in Reference [2] employed the random

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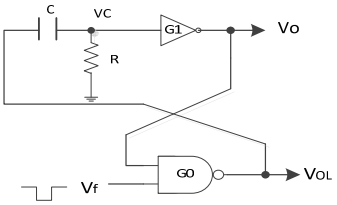
number and smoothing method, which involve simple circuits and has a long conversion time. An analog filter composed of RC was used in the design. The chip and RC filter performances were closely related [2]. The ADC for 0.8 μm CMOS technology was developed in foreign countries by the moving average filter technique. In this design, the converting signal was used directly as the supply voltage of CMOS delay gate and conducts measurements by utilizing the linear relationship between time delay size and the supply voltage on the CMOS gate. However, the applicable converting-voltage range for the design is limited, i.e., it is applicable to a low-voltage (1.8 V to 2.0 V) CMOS sensor. No report is available yet on whether a linear relationship exists between the delay time of the gate and the supply voltage beyond this voltage range. Given that the digitization of time-to-digital conversion is mature, an ADC chip can be designed indirectly by first converting voltage (current) into the ATC of the time signal and then digitizing this ATC.

The remainder of this paper is organized as follows. Chapter III analyzes the principle of ATC and discusses the theoretical implementation of ATC. Chapter IV studies the circuit composition of a multifunction digital chip and designs core, level-switching, electro static discharge (ESD) protective, and output buffer circuits. Chapter V presents the performance simulation of a multifunction digital chip under different temperatures and technologies. Chapter VI provides the layout design of the designed chip and the on-wafer test result. Chapter VII concludes. Chapter VIII provides the acknowledgment.

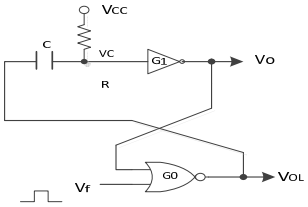
3. Implementation of ATC

The RC differential function can constitute constant 0 and 1 differential monostable trigger circuits. The differential monostable circuits and their waveform are shown in Figure 1. In the constant 1 differential monostable trigger circuit, the output voltage V_{OL} becomes high when the input end Vf has a negative triggering pulse. At the same time, VC becomes high by the coupling effect of supply voltage C. By contrast, the output V0 becomes low because V0 is the feedback to the input end.

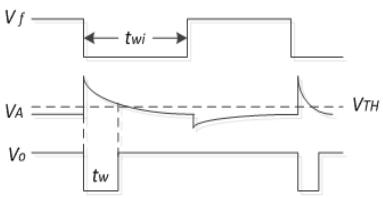
V_{OL} can still maintain a high level for a short time even if the negative triggering pulse of V_f disappears, thus resulting in the transient steady state of circuit. However, the VC in the RC circuit decreases with the charging of supply voltage C. When VC = V_{TH}(V_{TH}:threshold voltage), Vo returns to a high level, and the circuit returns to a steady state. In the constant 0 differential monostable trigger circuit, the low level of V_{OL} can be maintained for some time because of the feedback effect of Vo. With the charging of C, VC increases to V_{TH} gradually, Vo returns to a low level, and the circuit returns to the steady state.



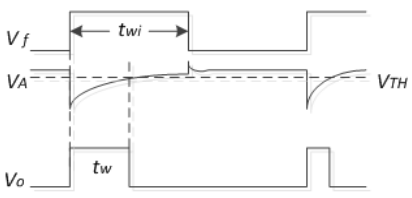
(a) Constant 1 differential monostable circuit



(b) Constant 0 differential monostable circuit



(c) Waveform of Figure 1(a)



(d) Waveform of Figure 1(b)

Figure 1. Differential monostable circuits and their waveforms

According to the above analysis on differential monostable circuits, these circuits have no specific requirements on input-triggering pulse and are applicable to this new multifunction digital chip. The constant 1 differential circuit can be used to measure the unknown voltage within the range of 0 to VTH, whereas the constant 0 differential circuit can be used to measure the unknown voltage within the range of V_{TH} to V_{DD}.

In Figure 1, the output pulse width T_W of the constant 1 differential monostable trigger circuit is only determined by the time for VC on R to decrease from the transition to V_{TH} during the charging process of C in the RC circuit. The delay time of the constant 0 differential monostable trigger circuit is determined by the charging time of C until VC increases to V_{TH}. It can be used to calculate the T_W approximately, and T_W can be calculated by the following equation:

$$T_w = RC\frac{V_{C(\infty)} - V_{C(0)}}{V_{C(\infty)} - V_{TH}} \quad (1)$$

Where $V_{C(0)}$ is the initial value of capacitor voltage, $V_{C(\infty)}$ is the end value of the capacitor voltage, and V_{TH} is the threshold voltage of the post-gate circuit. For a specific circuit, V_{TH} is fixed. When RC is determined, a corresponding relationship exists between T_W and $V_{C(\infty)}$ (Equation (2)). This relationship is the basic reference of ATC implementation:

$$T = f(V) \quad (2)$$

A numerical conversion circuit is then used to convert it into the corresponding numerical value of $V_{C(\infty)}$, thus accomplishing the numerical conversion from digital count N to $V_{C(\infty)}$ (Equation (3)).

$$V_{C(\infty)} = F(N) \quad (3)$$

4. Multifunction Digital Chip Design

The multifunction digital chip based on CMOS technology is shown in Figure 2. This chip mainly includes a core circuit, level switching circuit, output buffer circuit, and ESD(Electro-Static Discharge) protective circuit.

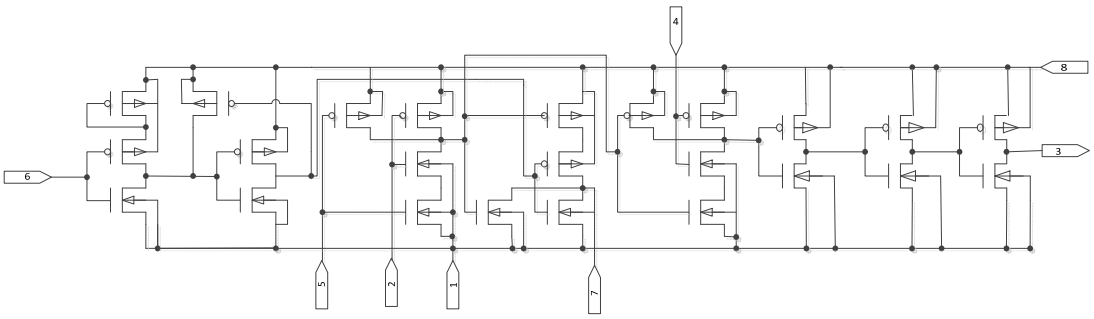


Figure 2. Multifunction digital chip

4.1. Core Circuit

The core circuit is the main component of the integrated circuit and is responsible for the main functions of the circuit. The core circuit can accomplish ATC through the external port of the integrated circuit together with R and C. The core circuit can also easily realize monostable triggers, multivibrators, and Schmitt triggers [1]. An ESD protective circuit is mainly used to avoid the CMOS-integrated circuit damages and latch-up caused by ESD. The level-switching circuit is mainly used to make the designed chip compatible with transistor–transistor

logic (TTL). The output buffer circuit is mainly used to increase the drive capability of the chip by increasing the output inverter chain.

4.2. Level-switching Circuit Composed of an Improved Inverted Buffer

Chip compatibility is a key problem that has to be considered in the design. A CMOS technical tape-out was employed in this design. In practical applications, the front end of the chip may be a TTL chip with the following logic level during operations: $VOL = 0.4V$ and $VOH = 2.4V$. Considering the influences of a service environment, when the supply voltage is 5 V, the general limits of the output-level range of the front-end TTL chip are $VOL_{\max} = 0.8V$ and $VOH_{mim} = 2.0V$. These limits are accessed to the input end of CMOS chip directly; the NMOS(N-Metal-Oxide-Semiconductor) and PMOS(positive channel Metal Oxide Semiconductor) tubes will be respectively broken down at $VOL_{\max}$ and VOH_{mim}, thus resulting in circuit breakdown. Therefore, a level-switching circuit at the input end is needed to convert the chip input level into the level range for CMOS chips to work normally. However, existing level-switching circuits composed of inverted buffers has width-to-length ratios of 11:1 for NMOS and PMOS tubes; this ratio denotes power and area consumption. The level-switching circuit composed of a CMOS Schmitt trigger is also disadvantageous for the large tube consumption and wide chip area [2]–[5]. The level-switching circuit used in the current chip is shown in Figure 3. M1 is a diode composed of PMOS tubes and is added to the PMOS source electrode of the first-stage input inverter. Owing to the effect of the substrate bias of M1, the additional PMOS tube increases the absolute value of the threshold voltage and reduces the effective supply voltage on the inverter. Therefore, adding M1 decreases the threshold logic level of the first-stage input level. The NMOS and PMOS tubes, which have small electric conduction, are optional as the inverter of the first-stage input level. However, another PMOS feedback tube (M4) is added to the circuit to maintain the high-level performance of the first-stage inverter after M1 is used. The simulation test result indicates that the level-switching circuit of the proposed chip design can convert the front-end TTL level into the operating level of the input end of this chip effectively. The circuit used occupies a small area during tape-out.

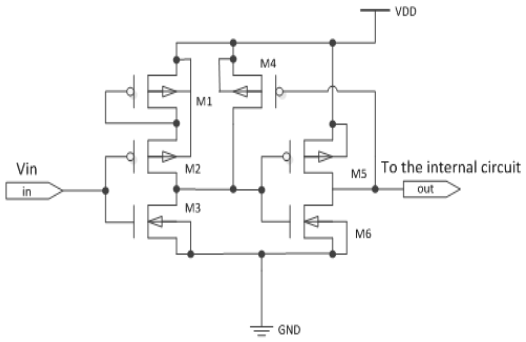


Figure 3. Level-switching circuit

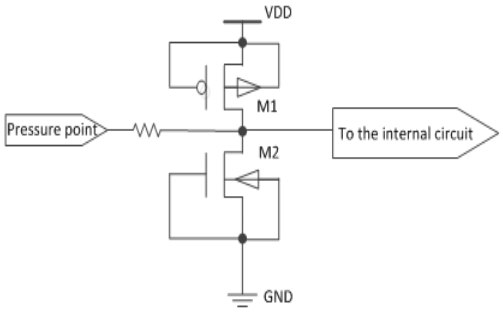


Figure 4. ESD protective circuit

4.3. ESD Protective Circuit

ESD has to be considered in MOS integrated chip design. ESD damage will cause gate breakdown inside the CMOS device and latch-up inside the chip. The device and circuit will also be damaged upon the local chip heating caused by the ESD-induced instantaneous high current. Particularly, the input and output ends are vulnerable to ESD [6]–[10]. On the basis of a comprehensive consideration on existing pair diode ESD protective circuit, this design uses a pair of PMOS and NMOS tubes to form the input ESD protective circuit. The NMOS tube gate is connected to the ground, whereas the PMOS tube gate is connected to VDD. Given that the MOS tube for designing ESD protective circuit is significantly large, a pectination MOS transistor is used for the layout design. The diode protection of PN structure in the leaking source region of the large MOS tube can also be used well. The ESD protective circuit is shown in Figure 4.

4.4. Output Buffer Circuit Composed of a Fix-tapered Buffer Chain

During chip design, attention should be focused on the output drive capability of the chip. The operating speed of the circuit can only be guaranteed when the drive current at the output level is large enough. The drive current is often increased by increasing the width-to-length ratio of the MOS (Metal Oxide Semiconductor) tube. However, the priori load capacitance and priori delay time will increase when the MOS tube expands. As a result, under the premise of a minimum total delay time of the buffer, an output buffer that can provide appropriate drive current is important to chip design. In CMOS chip design, an inverter chain composed of a multilevel inverter is commonly used as the output buffer [11-15]. In this chip design, a fix-tapered buffer chain composed of a three-level inverter with a progressive increase of 1.6 is used as the output buffer to increase the drive capability of the circuit. The output buffer circuit of the chip is shown in Figure 5.

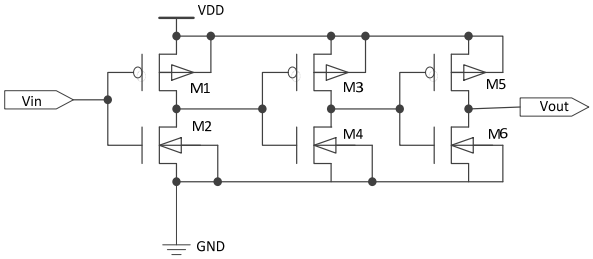


Figure 5. Output buffer circuit

5. Performance Simulation of the Multifunction Chip

A simulation test on the performances of the designed multifunction chip under different conditions was conducted using the Hspice software and the CSMC 2P2M 0.6 μm CMOS process database (06mixddct02v24).

5.1. Simulation Test under Different Process Feet

The simulation results of the multifunction chip under different process corners (FF, FS, SF, and SS) are presented in Figure 6.

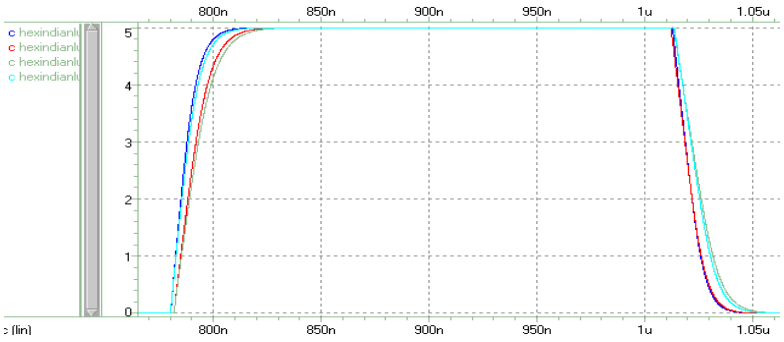


Figure 6. Simulation results of the chip under different process corners (FF, FS, SF, and SS).

Figure 6 indicates that the chip performances change considerably when the process corner varies within the acceptable range (the maximum change in the rise time delay of the circuit (from FF to SS) is 4.72 ns, and the fall time delay is 3.63 ns).

5.2. Simulation Test under Different Temperatures

The performance simulation of the chip under different temperatures (−25, 0, 25, 50, 80, and 120 °C) is shown in Figure 7.

In Figure 7, the chip performances under different temperatures (−25, 0, 25, 50, 80, and 120 °C) change insignificantly. The maximum rise time delay and fall time delay of the circuit were 0.836 and 3.79 ns, within the acceptable range, respectively.

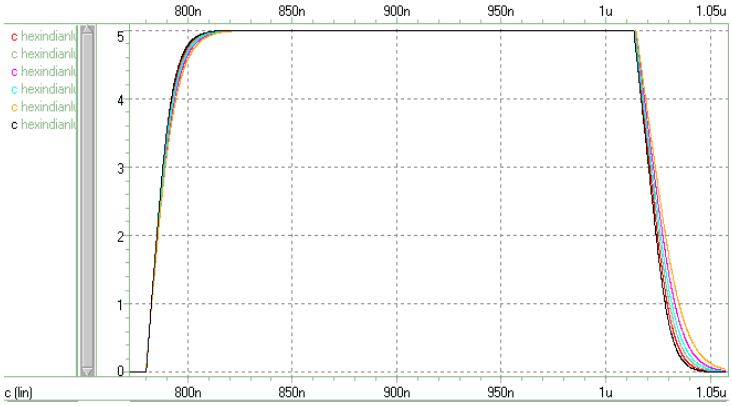
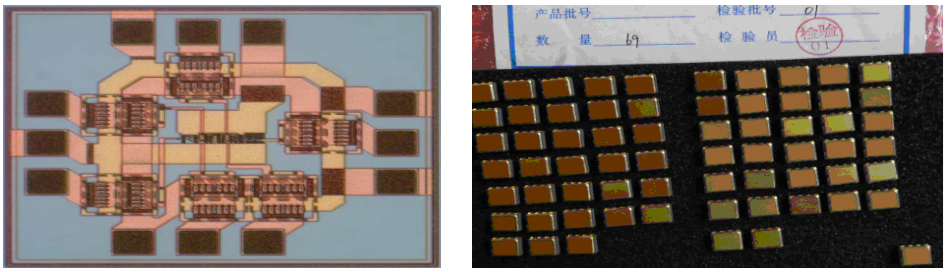


Figure 7. Performance simulation of the chip under different temperatures.

6. Chip Layout Design and Test Result Analysis

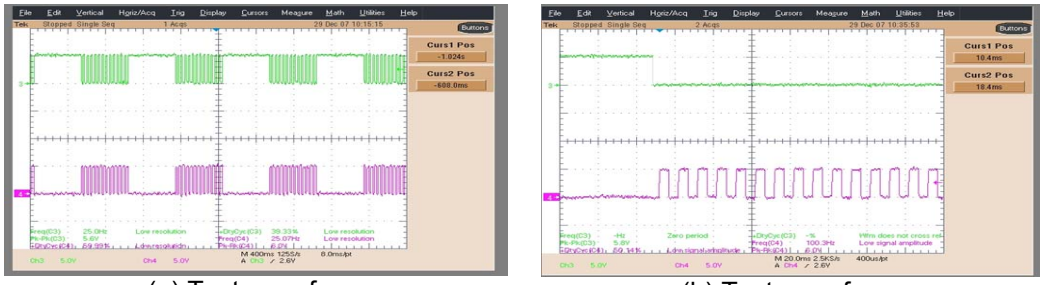
The entire system layout was designed and verified on the Jiutian layout editor and layout verification environment (ZeniPDT&ZeniVERI). The layout of the multifunction digital chip and the physical map of the encapsulated chip are shown in Figure 8.



(a) Layout (b) Physical map

Figure 8. Chip layout

Figures 9(a) and (b) show the tape-out test waveforms under different inputs. According to the test result, the proposed chip can realize various logic functions.



(a) Test waveform (b) Test waveform

Figure 9. Chip test results

7. Conclusion

This study proposes a new multifunction digital chip design based on CMOS technology. The chip layout design and verification are implemented on the basis of the CSMC 2P2M COMS technology. The proposed chip covers an area of 1 mm^2, has a simple circuit configuration, and is easy to be integrated. With additional devices, the chip can realize various functions, including ATC, monostable triggers, multivibrators, and Schmitt triggers. The chip can also change the transient state of the circuit by changing the control level connected to port 5 while realizing a monostable trigger, thus enabling a delay time five times higher than that of the traditional 555 timer. The on-wafer and encapsulated test results after tape-out show that the chip realizes preset functions and is widely used in various popular integrated circuit chip designs as an IP core.

Acknowledgements

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