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Optimal Modulation Algorithm for Hybrid Clamped Three-Level Inverter

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Abstract

The principle of a three phase hybrid clamped three-level inverter was presented. Taking sixty-four switch states into consideration, the operational states of hybrid clamped three-level inverter and different current circuits in different switch states were detailed derived. Optimal modulation algorithm was proposed based on the neutral small vectors by different combination, which can realize the automatic balancing of the neutral-point voltage with few switching cycles and did not need to measure the voltage of the clamped capacitors. The proposed modulation algorithm was also capable of restraining the turn-off over-voltage of the power switching devices effectively. Simulation results were given to verify the feasibility and correctness. Experimental results obtained by DSP-based implementation of the controller on 1 MW prototype show good performance in terms of DC-bus voltages regulation (small neutral point potential function and low DC ripple coefficient) and good sinusoidal current.

Keywords*: Optimization method, Hybrid clamped inverter, Pulse width modulation, DC-voltage balance*

1. Introduction

Nowadays, in order to meet the demands of the high-voltage grades and high-power inverter, an important trend in power electronic has been the replacement of the traditional two-level inverter by multilevel inverter [1-3]. With the development of power electronic technology, in [4-7], multilevel technology has been widely studied in the high-voltage and high-power system, grid-connected wind power system, active power filters, and many other fields. Currently, there is a large variety of such multilevel topologies available[8-9]. However, the three phase diode clamped three-level inverter is the most widely used topology. As an effective multilevel implementation, besides the characters of fewer power switching devices, lower input current harmonics, better sinusoidal and high adjustable power factor, diode clamped three-level inverter also has the advantages of bi-directional energy transfer, lower switching frequency and higher system efficiency, which can satisfy the requirements of higher voltage grades, higher power and lower harmonic pollution trend of inverter [10]. The operation and the control of three phase diode clamped three-level inverter have been researched during the last decade and both control and modulation methods have been presented in [11-12].

However, large-scale application of multilevel topology is subjected to the unbalance voltages of capacitors in DC-bus and the turn-off over-voltage for power switching devices [13-15], and diode clamped three-level inverter is no exception [16]. To solve the above problems, a variety of ideas have been put forward in many research papers [17-19]. Among these, the topology proposed by Korean scholar Young-Seok Kim in 1993, called the hybrid clamped three-level inverter (HCTLI) has the additional benefits of increased controlled switch states in addition to the general the benefits of diode clamped three-level inverter. Compared to three phased diode clamped three-level inverter, three clamped capacitors are added to three clamped legs. Thus, it can restrain the fluctuations of DC-bus neutral potential, realize the bidirectional current flow and restrain the over-voltages of the power switching devices by charging or discharging clamped capacitors and feasible modulation algorithms. Thereby, due to the opportunities of competitive advantages, HCTLI is generally considered attractive and applied as an inverter for the DC-AC converter. The research of HCTLI has focused so far on control schemes, fewer on the pulse width modulation (PWM) algorithms. Traditionally, in order to restrain the problem of DC-bus capacitor voltages unbalance, these modulation algorithms

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were proposed usually via the measure of DC-bus capacitor voltages and clamped capacitors.

The purpose of this paper is to analyze the operation of the HCTLI, based on an analytical analysis of current circuit and clamped capacitor states, and to determine if a suitable modulation algorithm can implemented. Concentrated on the three phased HCTLI, a new PWM control algorithm is proposed by different optimal combination of neutral small vectors without the use of three clamped capacitor voltages measured in this paper. It can reduce the fluctuations of DC bus neutral voltage and restrain the over-voltages of the power switching devices. These functionalities of the proposed PWM control algorithm are demonstrated by both simulations and experimental results from a DSP controlled, the 1 MW rated inverter prototype.

2. Control Principle of HCTLI

HCTLI using insulated gate bipolar transistor (IGBT) switches is presented in Figure 1. The main topology of the HCTLI consists of twelve power switches with anti-parallel diodes, each having voltage stress of U_d /2. There are six clamped diodes with three parallel clamped capacitors on phase legs and two DC-bus capacitors (C_1,C_2) in series on the DC side. The neutral point O of DC-bus is connected directly to three clamped midpoints.

To illustrate operation condition of HCTLI, phase A is set as an example to analyze. It is composed of clamped diodes (D_{1a}~D_{2a}), clamped capacitor C_a and four switches (S_{1a}~S_{4a}) with anti-paralleled diodes(D_{3a}~D_{6a}). Bidirectional current paths from load to the DC-bus potentials are achieved via switches (S_{1a}~S_{4a}) and diodes (D_{1a}~D_{6a}). Due to the clamped capacitor (C_a) of HCTLI, switches S_{2a} and S_{3a} can not work at the same time.

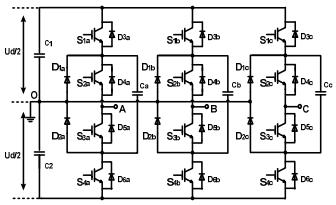
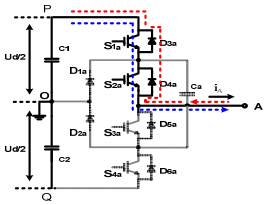
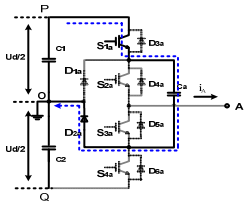


Figure 1. Main topology of the hybrid clamped three level inverter



(a) current flow paths



(b) charge/discharge paths of C_a

Figure 2. Diagrams of current circuit and clamped capacitor state when $S_A=1^+$

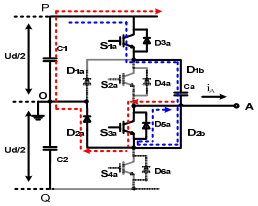
The power switches states of phase A could be represented by S_A. $S_A=1^+$ indicates the on state of power switches S_{1a},S_{2a} with S_{3a}, S_{4a} off. $S_A=0^+$ indicates the on state of power switches S_{1a}, S_{3a} with S_{2a}, S_{4a} off. $S_A=0^-$ indicates the on state of power switches S_{2a}, S_{4a} with S_{1a}, S_{3a} off. $S_A=1^-$ indicates the on state of power switches S_{3a}, S_{4a} with S_{1a}, S_{2a} off. Thus, the output voltage could be controlled by the switch states described above.

1) $S_A=1^+$ state

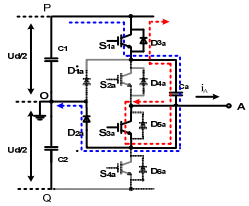
In $S_A=1^+$, the S_{1a}, S_{2a} are turned on and S_{3a}, S_{4a} off as shown in Figure 2(a). In steady-state conditions, if the phase current i_a is positive, the current flow along with the path: P→S_{1a}→S_{2a}→A. On the contrary, the current path will become A→D_{4a}→D_{3a}→P. Whatever the direction of ia, the pole A is connected to the positive point P of DC-bus, having the following equations: $U_{AO}=U_{PO}=0.5U_d$. On this occasion, the neutral point of the DC-bus should be remain clamped at one half of the complete DC-bus voltage. The possibility of influencing the neutral point potential is based on the clamped capacitor voltage U_{Ca}. If the voltage $U_{Ca}>U_{PO}$, the clamped capacitor voltage U_{Ca} remains constant, and the clamped capacitor C_a will be discharged in the next switch state. Otherwise the voltage $U_{Ca}<U_{PO}$, the capacitor C_a will be charged along with the path: P→S_{1a}→C_a→D_{2a}→O, as shown in Figure 2(b), until the two voltages meet the equation $U_{Ca}=U_{PO}$. The neutral point potential of DC-bus is thereby rising in $S_A=1^+$.

2) $S_A=0^+$ state

In Figure 3(a), if the phase current i_a is positive in steady-state condition, the current flow along with the path: P→S_{1a}→C_a→D_{5a}→A. On the contrary, the current path will become A→S_{3a}→D_{2a}→C_1→P. Whatever the direction of i_a, the pole A is connected to below point of C_a. Three-level inverter has a problem that excessive high voltages may be applied to the power switches, when the floating mid-potential varies from the neutral point potential. In this state, the neutral point potential is changed constantly along with clamped capacitor charged and discharged. If the voltage $U_{Ca}>U_{PO}$, the positive point P is connected to up point of the C_a at this moment. And the C_a would be discharged along with the path: A→S_{3a}→C_a→D_{3a}, while the phase current i_a is negative. On the other hand if the voltage $U_{Ca}<U_{PO}$, the C_a would be charged along with the path: P→S_{1a}→C_a→D_{2a}→O, until the two voltages meet the equation: $U_{Ca}=U_{PO}$. The path of clamped capacitor charged and discharged is illustrated in Figure 3(b). The output voltage U_{AO} is zero in $S_A=0^+$.

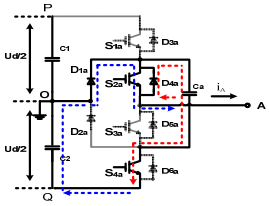


(a) current flow paths

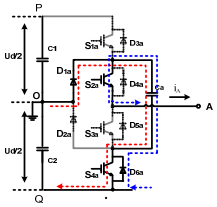


(b) charge/discharge paths of C_a

Figure 3. Diagrams of current circuit and clamped capacitor state when $S_A=0^+$



(a) current flow paths



(b) charge/discharge paths of C_a

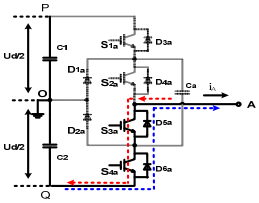
Figure 4. Diagrams of current circuit and clamped capacitor state when $S_A=0$

3) $S_A=0^-$ state

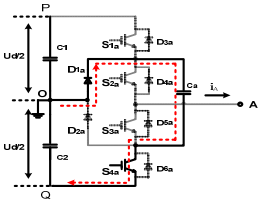
In contrast to the state of $S_A=0^+$, the power switches S_{1a}, S_{3a} are turned off with S_{2a}, S_{4a} on. When the phase current i_a is positive in steady-state condition, the current flow along with the path: Q→C_2→O→D_{1a}→S_{2a}→A. On the contrary, the current path will become A→D_{4a}→C_a→S_{4a}. The conduction path of current is illustrated in Figure 4(a). Similarly, the voltage across the clamped capacitor U_{Ca} is analyzed. As shown in Figure 4(b), if the voltage $U_{Ca}>U_{OQ}$, the C_a would be discharged along with the path: D_{6a}→C_a→S_{2a}→A. On the other hand, if the voltage $U_{Ca}<U_{OQ}$, the C_a will be charged along with the path: O→D_{1a}→C_a→S_{4a}→Q, until the voltage of the U_{Ca} has the same value as the voltage U_{OQ}. The output voltage U_{AO} between the inverter pole A and the neutral point O of DC-bus is also zero in $S_A=0^-$.

4) $S_A=1^-$ state

The conduction path of current is presented in Figure 5(a), and the switches S_{1a}, S_{2a} are turned off and S_{3a}, S_{4a} turned on. Under steady-state condition, if the phase current i_a is positive, the current flow along with the path: Q→D_{6a}→D_{5a}→A. Instead, the current flow path will become A→S_{3a}→S_{4a}→Q, when i_a is negative. Whatever the direction of i_a, the pole A is connected to negative point Q of the DC-bus, having the following equations: $U_{AO}=U_{QO}=-0.5U_d$. In the same way, if the voltage $U_{Ca}>U_{OQ}$, the U_{Ca} remains constant. And the C_a would be discharged in the next switch state. Otherwise, the voltage $U_{Ca}<U_{OQ}$, as shown in Figure 5(b), the C_a would be charged along with the path: O→D_{1a}→C_a→S_{4a}→Q, until the two voltages meet the equation: $U_{Ca}=U_{OQ}$. The neutral point potential of the DC-bus is dropped sequentially in $S_A=1^-$.



(a) current flow paths



(b) charge/discharge paths of C_a

Figure 5. Diagrams of current circuit and clamped capacitor state when $S_A=1^-$

Table 1. Switch states for phase A of HCTLI

S_A	S_{1a}	S_{2a}	S_{3a}	S_{4a}	U_{AO}
1^+	ON	ON	OFF	OFF	0.5Ud
0^+	ON	OFF	ON	OFF	0
0^-	OFF	ON	OFF	ON	0
1^-	OFF	OFF	ON	ON	-0.5Ud

To sum up, the switch states of phase A could be derived, and presented in Table 1. Similarly, this operating principle also applies to phase B and C. Because of four kinds of switch states for each phase, the HCTLI contains 4^3=64 kinds of switch state combinations. It makes control complicated, but the control accuracy will be improved with switch states increased.

3. DC-Bus Voltage Balance Analysis

HCTLI topology has been applied in medium and high voltage power applications due to the inherent advantages[20]. However, it also has the problem that the neutral point potential floated. It may lead to the issue that the power switches bear excessive high voltage. The HCTLI topology shows that stable neutral point potential determines whether the voltages of two DC-bus capacitors are balanced or not. In practical operation, the neutral point potential would fluctuate, leading to these two voltages of the DC-bus capacitors do not equal completely. Such voltage fluctuations may also result in distortion of the inverter output voltages, harmonic content increased and decrease in the output efficiency. Meanwhile, excessive high voltage that power switch devices withstood would cause the device itself breakdown and make the systematic reliability reduced greatly [16, 21]. And not only that, the life span of capacitance will also be greatly reduced because of severe capacitor voltages fluctuation, which would greatly damage AC drives. So it is important and significant to balance the DC-bus capacitor voltages.

It is generally known that HCTLI contains 64 kinds of switch states corresponding to 64 voltage space vectors, but among them are some redundant vectors. The neutral point potential is primarily influenced by these redundant vectors generated at the output of the inverter. The distribution of voltage space vectors is presented in Figure 6. It has 64 kinds of voltage space vectors, but there are only 19 kinds of valid and equivalent voltage space vectors after equivalent transformation, including one zero vector V_0, six small vectors V_1~V_6, six mid-vectors V_7~V_{12} and six large vectors V_{13}~V_{18}. Among of them, the vector V_0 contains 10 kinds of switch states and six switch states for each small vector, while each mid-vector corresponds to two switch states and each large vector corresponds to only one.

Different outputs of the inverter are generated by voltage space vectors based on the combination of 64 switch states in different ways. The analysis of these different output states of HCTLI shows that there are only seven output states associated with the DC-bus capacitors and the load. As Figure 7 shows, the direction of the arrows indicates the direction of loop-current.

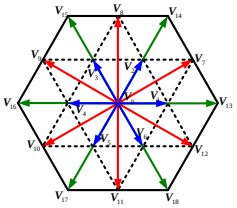


Figure 6. Diagram of voltage space vector distribution

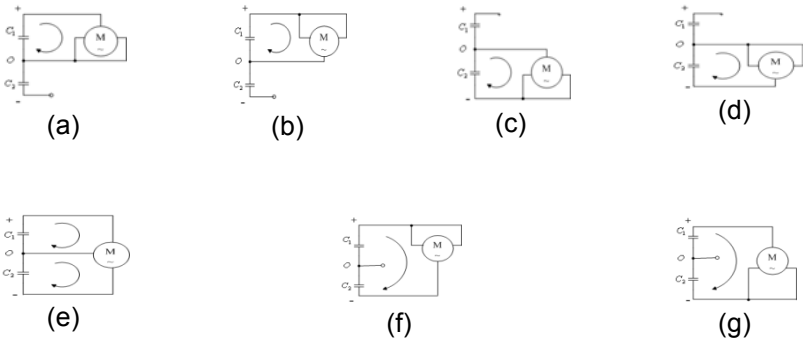


Figure 7. Current paths under seven output states

The switch states that correspond to output states mentioned above are shown respectively:

(1) Output state "a": $1^+0^+0^+$, $0^+1^+0^+$, $0^+0^+1^+$; (2) Output state "b": $1^+1^+0^+$, $1^+0^+1^+$, $0^+1^+1^+$;

(3) Output state "c": $0^-1^-1^-$, $1^-0^-1^-$, $1^-1^-0^-$; (4) Output state "d": $1^-0^-0^-$, $0^-1^-0^-$, $0^-0^-1^-$;

(5) Output state "e": There are thirty six combinations for switch states, of which small vectors $1^+0^+0^-$ and $1^-0^+0^-$ all have six kinds of combinations. However, small vectors $1^+0^-0^-$, $1^+1^+0^-$, $0^+1^-1^-$ and $1^-0^+0^+$ all have three kinds. Meanwhile, each of mid-vectors $1^+0^+1^-$ and $1^+0^-1^-$ also has six kinds of combinations;

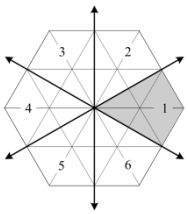
(6) Output state "f": $1^+1^+1^-$, $1^-1^+1^+$, $1^+1^-1^+$; (7) Output state "g": $1^+1^-1^-$, $1^-1^+1^-$, $1^-1^-1^+$.

Known from the analysis of the above: (i) In "a" and "b" output states, the neutral point potential rises, and the HCTLI outputs positive small vectors. The load is only connected to the capacitor C_1, which forms a discharge circuit. At this moment, the voltage of C_1 drops and the other rises. (ii) In "c" and "d", the neutral point potential drops, and the HCTLI outputs negative small vectors. The load is only connected to C_2, and it forms a discharge circuit. In these two states, the voltage of C_2 drops and the other rises. (iii) In "e", the HCTLI outputs neutral small vectors and mid-vectors. The two capacitors C_1 and C_2 are both connected to the load, which constituting two charge-discharge circuits. In theory, the small scale fluctuation of neutral potential can be achieved by some combinations of neutral small vectors and mid-vectors. (iv) In "f" and "g", the neutral point O has no connection and no current to the load. In this case, large vectors are generated. At the same time, the load connects the C_1 and C_2 directly, which have the same value in charge-discharge time and the average current of charge-discharge. In theory, as long as these two capacitors have the same parameters, the neutral point potential would keep constant. Accordingly, the neutral point potential is not affected by the large vectors.

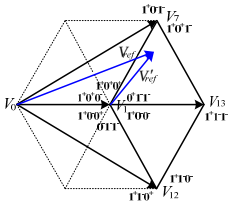
In summary, selecting different vectors to synthesize the reference voltage space vectors will cause different effects on the neutral point potential.

4. Optimized Modulation Algorithm

Select the appropriate voltage space vectors is the core issue of SVPWM for HCTLI. The hexagonal plane of three-level voltage space vector is divided into six small hexagons of the same shape in conventional modulation algorithm, and then solved by two-level SVPWM in two-level voltage space vector plane [22]. However, this conventional modulation algorithm needs to further divide the reference voltage vector regions, because of its intersection area for some vectors. Figure 8(a) shows a new irregular division method adopted in this paper.



(a) Vector plane division (S =1, 2, 3, 4, 5, 6)



(b) Composition for the reference voltage vector in small hexagonal section S=1, small triangle section N=1

Figure 8. Diagrams of vector plane division and vector composition

Table 2. Switch states for phase A

Num	Switch states
1	$1^+\,0^+\,0^+ \rightarrow 1^+\,0^+\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^-\,1^-\,1^-$
2	$1^+\,0^+\,0^+ \rightarrow 1^+\,0^+\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^+\,1^-\,1^-$
3	$1^+\,0^-\,0^- \rightarrow 1^+\,0^-\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^-\,1^-\,1^-$
4	$1^+\,0^-\,0^- \rightarrow 1^+\,0^-\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^+\,1^-\,1^-$
5	$1^+\,0^-\,0^+ \rightarrow 1^+\,0^-\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^-\,1^-\,1^-$
6	$1^+\,0^-\,0^+ \rightarrow 1^+\,0^-\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^+\,1^-\,1^-$
7	$1^+\,0^+\,0^- \rightarrow 1^+\,0^+\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^-\,1^-\,1^-$
8	$1^+\,0^+\,0^- \rightarrow 1^+\,0^+\,1^- \rightarrow 1^+\,1^-\,1^- \rightarrow 0^+\,1^-\,1^-$

The vector planes (S = 1, 2, 3, 4, 5, 6) are divided to ensure the reference vector can be assigned to a unique two-level voltage space vector plane. Take the vector plane divided (small hexagonal section S=1, small triangle section N=1) as an example to illustrate and calculate the switch operation time of voltage vectors selected. This triangle demarcates the valid and realizable location for the reference voltage vector. For HCTLI, SVPWM is implemented by synthesizing the reference vector using the three nearest vectors forming a triangle around it. As shown in Figure 8(b), when the reference voltage vector V_{ref} lies to the first region N=1, the V_{ref} can be jointly synthesized by three voltage vectors V_1, V_7 and V_{13}. According to the principle of Volt-second balance, the operation times of V_1, V_7 and V_{13} would be derived at a sampling period through the voltage vectors correction and two-level SVPWM algorithm.

In Figure 8(b), the vector V'_{ref} is corrected by V_{ref} and V_1 as the following function.

$$V'_{ref} = V_{ref} - V_1 \tag{1}$$

Then, the Volt-second balance for the correct reference voltage can be expressed as:

$$V'_{ref} \cdot T_s / 2 = V_1 \cdot T_0 + V_7 \cdot T_1 + V_{13} \cdot T_2 \tag{2}$$

HCTLI has 19 kinds of valid and equivalent states of the following type:

$$S_{ABC} = \begin{bmatrix} S_A & S_B & S_C \end{bmatrix}^T \tag{3}$$

Switch states S_X (x=A,B,C) take values in{1^+, 0^+ or 0^-, 1^-} presenting the per unit voltage of the phase with respect to the neutral point. Phase to neutral point voltages are given by:

$$\begin{bmatrix} U_{AO} & U_{BO} & U_{CO} \end{bmatrix}^T = 0.5U_d \begin{bmatrix} S_A & S_B & S_C \end{bmatrix}^T \tag{4}$$

Thus, these voltages could be converted into the α-β coordinate using the following transformation:

$$\begin{bmatrix} V_{ref\alpha} \\ V_{ref\beta} \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} U_{AO} \\ U_{BO} \\ U_{CO} \end{bmatrix} \tag{5}$$

The corresponding operation times (T_0, T_1 and T_2) of V_1, V_7 and V_{13} are derived by equations (1)~ (5) respectively as follows:

$$\begin{cases} T_0 = T_s - T_1 - T_2 \\ T_1 = 3\sqrt{3}V_{ref\alpha}T_s / U_d \\ T_2 = 4.5V_{ref\beta}T_s / U_d - 3T_s / 2 - 3\sqrt{3}V_{ref\alpha}T_s / 2U_d \end{cases} \tag{6}$$

Where: T_S is the sampling period, $V_{ref\alpha}$ and $V_{ref\beta}$ are the components of V_{ref} in α,β axis.

In order to adjust the neutral point potential fluctuations, the conventional modulation algorithm generally detects the voltages of DC-bus capacitors and the clamped capacitors, and then combines the positive and negative small vectors to make it come true. However, It may be equivalent to a hysteretic regulator, which applies only to the case of DC-bus voltage imbalance. The effects of the clamped capacitors and the neutral small vectors are ignored in conventional modulation. Thus, taking fully account of the clamped capacitors charging and discharging effects, a new voltage vector selection method to synthesize the reference vector of SVPWM algorithm is proposed in this paper. Furthermore, choosing different appropriate combinations of neutral small vectors makes voltage vector selection implement.

Take the reference voltage V_{ref} shown in Figure 8(b) for example to analyze. As mentioned above, the reference voltage vector V_{ref} can be jointly synthesized by three voltage vectors V_1, V_7 and V_{13} using the method of seven segment configuration. For SVPWM, the sequence of these three voltage vectors applied during a switching cycle is as follows:

$$V_1 \rightarrow V_7 \rightarrow V_{13} \rightarrow V_1 \rightarrow V_{13} \rightarrow V_7 \rightarrow V_1$$

In the corresponding six switch states of small vector V_1, both the positive small vector state $\{1^+0^+0^+\}$ and negative small vector state $\{0^-1^-1^-\}$ have a significant impact on the neutral point potential, and others are neutral small vector states$\{1^+0^+0^-$, $1^+0^-0^+$, $1^+0^-0^-$, $0^+1^-1^-\}$. Mid-vectors have two kinds of states$\{1^+0^-1^-$, $1^+0^+1^-\}$, while large vector has only one switch state. Therefore, eight kinds of vector states sequences to synthesize reference voltage vector could be obtained as shown in Table 2.

In order to ensure that each switch state change makes only one power switch turn on or off, appropriate switch state should be selected from the neutral small vector and mid-vector to meet the need. For the first of the switch state sequences, the same changes of three-phase switch states are between S_{1x} and S_{4x} (x = a, b, c). And the fourth of the switch states, the changes of three-phase power switch states are between S_{2x} and S_{3x} (x=a, b, c). Considering the power switch devices S_{2a} and S_{3a} can not turn on simultaneously because of the HCTLI topology, the AC load current flows through the primary channel of 1^+ and 1^-. In order to improve the quality of AC current waveform and reduce switch losses of power switch devices S_{2x} and S_{3x} (x = a, b, c), in the meantime, taking the fluctuations of the clamped capacitor into account, this paper chooses the first sequence to synthesize the reference voltage vector. The first sequence of switch states with corresponding operation times is shown as follow:

$$\begin{array}{ccccccccccccc} 1^+0^+0^- & \rightarrow & 1^+0^+1^- & \rightarrow & 1^+1^-1^- & \rightarrow & 0^-1^-1^- & \rightarrow & 1^+1^-1^- & \rightarrow & 1^+0^+1^- & \rightarrow & 1^+0^+0^+ \\ \vdots & & \vdots & & \vdots & & \vdots & & \vdots & & \vdots & & \vdots \\ T_0/4 & & T_1/2 & & T_2/2 & & T_0/2 & & T_2/2 & & T_1/2 & & T_0/4 \end{array}$$

Similarly, the other vector sequences would be got to synthesize the voltage space vectors in other different sections of the vector plane following the principle proposed. The sequences of corresponding switch states for SVPWM algorithm are shown in Table 3.

Table 3. Switch states sequences for SVPWM

Small Sections	Switch states sequences		
	S=1	S=2	S=3
N=1	$1^+ 0^+ 0^+ \rightarrow 1^+ 0^+ 1^- \rightarrow 1^+ 1^- 1^- \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 1^+ 1^+ 1^- \rightarrow 1^+ 0^- 1^- \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 0^+ 1^+ 1^- \rightarrow 0^+ 0^- 1^- \rightarrow 1^- 0^- 1^-$
N=2	$1^+ 0^+ 0^+ \rightarrow 1^+ 0^+ 1^- \rightarrow 0^- 0^+ 1^- \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 1^+ 1^+ 1^- \rightarrow 0^- 1^+ 1^- \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 0^+ 1^+ 1^- \rightarrow 1^- 1^+ 1^- \rightarrow 1^- 0^- 1^-$
N=3	$1^+ 0^+ 0^+ \rightarrow 0^- 0^+ 0^+ \rightarrow 0^- 0^+ 1^- \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 0^- 1^+ 0^+ \rightarrow 0^- 1^+ 1^- \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 1^- 1^+ 0^+ \rightarrow 1^- 1^+ 1^- \rightarrow 1^- 0^- 1^-$
N=4	$1^+ 0^+ 0^+ \rightarrow 0^- 0^+ 0^+ \rightarrow 0^- 1^- 0^+ \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 0^- 1^+ 0^+ \rightarrow 0^- 0^- 0^+ \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 1^- 1^+ 0^+ \rightarrow 1^- 0^- 0^+ \rightarrow 1^- 0^- 1^-$
N=5	$1^+ 0^+ 0^+ \rightarrow 1^+ 1^- 0^+ \rightarrow 0^- 1^- 0^+ \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 1^+ 0^- 0^+ \rightarrow 0^- 0^- 0^+ \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 0^+ 0^- 0^+ \rightarrow 1^- 0^- 0^+ \rightarrow 1^- 0^- 1^-$
N=6	$1^+ 0^+ 0^+ \rightarrow 1^+ 1^- 0^+ \rightarrow 1^+ 1^- 1^- \rightarrow 0^- 1^- 1^-$	$1^+ 1^+ 0^+ \rightarrow 1^+ 0^- 0^+ \rightarrow 1^+ 0^- 1^- \rightarrow 0^- 0^- 1^-$	$0^+ 1^+ 0^+ \rightarrow 0^+ 0^- 0^+ \rightarrow 0^+ 0^- 1^- \rightarrow 1^- 0^- 1^-$
	S=4	S=5	S=6
N=1	$0^+ 1^+ 1^+ \rightarrow 0^+ 1^+ 0^- \rightarrow 0^+ 0^- 0^- \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 0^+ 0^+ 0^- \rightarrow 0^+ 1^- 0^- \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 1^+ 0^+ 0^- \rightarrow 1^+ 1^- 0^- \rightarrow 0^- 1^- 0^-$
N=2	$0^+ 1^+ 1^+ \rightarrow 0^+ 1^+ 0^- \rightarrow 1^- 1^+ 0^- \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 0^+ 0^+ 0^- \rightarrow 1^- 0^+ 0^- \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 1^+ 0^+ 0^- \rightarrow 0^- 0^+ 0^- \rightarrow 0^- 1^- 0^-$
N=3	$0^+ 1^+ 1^+ \rightarrow 1^- 1^+ 1^+ \rightarrow 1^- 1^+ 0^- \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 1^- 0^+ 1^+ \rightarrow 1^- 0^+ 0^- \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 0^- 0^+ 1^+ \rightarrow 0^- 0^+ 0^- \rightarrow 0^- 1^- 0^-$
N=4	$0^+ 1^+ 1^+ \rightarrow 1^- 1^+ 1^+ \rightarrow 1^- 0^+ 1^+ \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 1^- 0^+ 1^+ \rightarrow 1^- 1^+ 1^+ \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 0^- 0^+ 1^+ \rightarrow 0^- 1^+ 1^+ \rightarrow 0^- 1^- 0^-$
N=5	$0^+ 1^+ 1^+ \rightarrow 0^+ 0^- 1^+ \rightarrow 1^- 0^+ 1^+ \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 0^+ 1^- 1^+ \rightarrow 1^- 1^+ 1^+ \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 1^+ 1^- 1^+ \rightarrow 0^- 1^+ 1^+ \rightarrow 0^- 1^- 0^-$
N=6	$0^+ 1^+ 1^+ \rightarrow 0^+ 0^- 1^+ \rightarrow 0^+ 0^- 0^- \rightarrow 1^- 0^- 0^-$	$0^+ 0^+ 1^+ \rightarrow 0^+ 1^- 1^+ \rightarrow 0^+ 1^- 0^- \rightarrow 1^- 1^- 0^-$	$1^+ 0^+ 1^+ \rightarrow 1^+ 1^- 1^+ \rightarrow 1^+ 1^- 0^- \rightarrow 0^- 1^- 0^-$

In the same way, operation times of corresponding vectors in above regions could be obtained by the method proposed. Then, the pulses to control the switch devices on-off could be acquired based on SVPWM principle. The optimized modulation not only can meet the need to synthesize the voltage space vectors as a precondition, but also can balance the neutral point potential automatically. In addition to, it has good features of reducing the switch losses, decreasing switch frequency of S_{2x} and S_{3x}.

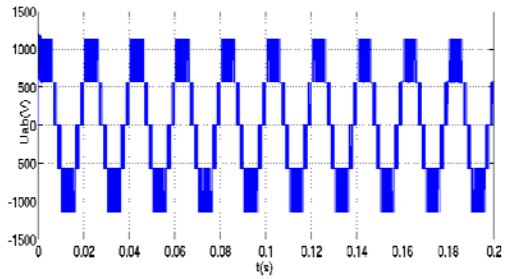
5. Simulation and Experiment

A detailed simulation for HCTLI has been built to verify the feasibility of the proposed algorithm based on Matlab/Simulink. The main parameters of simulation are listed in Table 4.

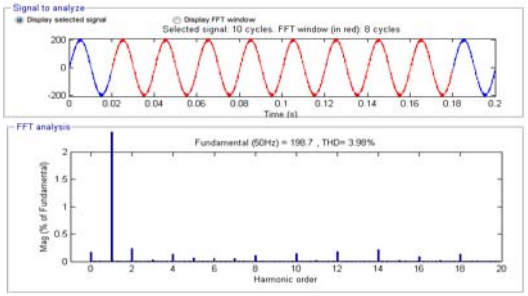
Figure 9 shows the simulation waveforms of HCTLI under steady-state operation. The modulated pole to pole voltage U_{AB} and the output current i_a are shown in Figure 9(a) and Figure 9(b) separately, and the total harmonic distortion of the measured current is 3.98%. DC-bus capacitors (C_1, C_2) voltages and the neutral point potential fluctuations are shown in Figure 9(c) and Figure 9(d). It is observed that the voltages of two DC-bus capacitors are almost balance. The fluctuation of the neutral point potential is very small, nearly ±5V.

Table 4. Main simulation parameters of HCTLI

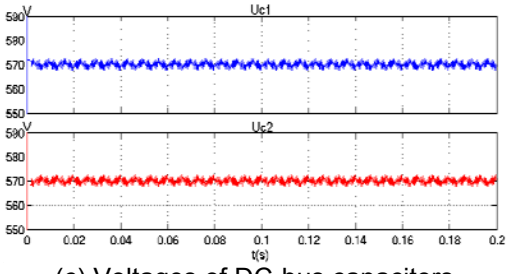
DC-bus voltage(V)	1140
Resistance load(Ω)	5
Inductance load(H)	$1e^{-3}$
DC-bus capacitors (μF)	4700*2
Clamped capacitors(μF)	1200*3
Switch frequency (Hz)	2000



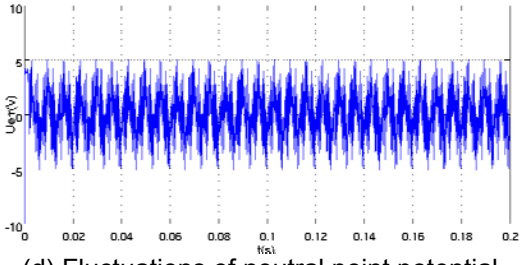
(a) The modulated voltage U_{AB}



(b) The output sinusoidal line current i_a



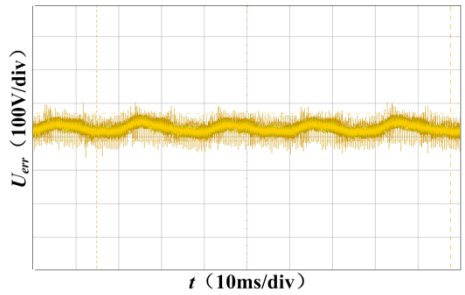
(c) Voltages of DC-bus capacitors



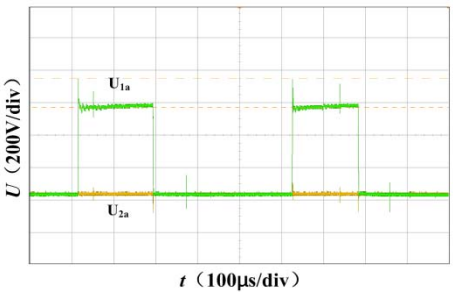
(d) Fluctuations of neutral point potential

Figure 9. Simulation of voltage and current, DC-bus voltages and neutral point voltage

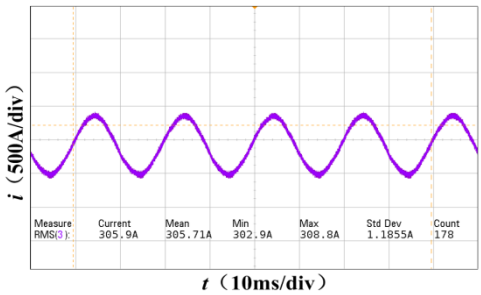
The proposed algorithm is also verified via experimental results of a 1MW prototype based upon DSP and CPLD/FPGA structure. Experimental measurements under steady state are recorded in Figure 10, which shows the waveforms of HCTLI neutral point potential fluctuations in Figure 10(a), power switch devices turn-off over-voltages in Figure 10(b) and output load current in Figure 10(c).



(a) Waveforms of the neutral point potential



(b) Turn-off over-voltage



(c) Output load current

Figure 10. Diagrams of neutral point voltage, over-voltage in cutting off and current curves

Similar to the simulation results, the DC-bus voltage is stable and the ratio of the neutral point potential fluctuation is very small. As shown in Figure 10(a), the neutral point potential fluctuation is ±42V, and the DC ripple coefficient is 3.75% measured in the experiment. The waveform display good load current sinusoidal, while controlling the power switch devices turn-off over-voltage effectively. The turn-off over-voltage of the power switch device S_{1a} is about 200V, when the load current is 305A. Experiment fully illustrated this optimized modulation strategy is able to meet the needs of DC-bus voltage balance, effectively reducing the neutral point potential volatility and turn-off over-voltage of power switch.

6. Conclusion

The hybrid clamped three-level inverter and the operating conditions corresponding to power switch states were presented in this paper. The basic of the DC-bus capacitor voltages balancing was analyzed. A new SVPWM control algorithm was proposed to ensure balancing the DC-bus capacitor voltages and outputting sinusoidal current are met based on different optimal combination of neutral small vectors without the use of three clamped capacitor voltages measured in this paper. The operated sequences of switch states for this optimal modulation algorithm has been detailed presented. The functionality of the optimal SVPWM algorithm was proven with simulations an experiments of a 1 MW laboratory prototype. The match between the simulation and experimental results validates the the optimal SVPWM algorithm. The hybrid clamped three-level inverter is able to maintain balanced DC-bus capacitor voltages and make lower turn-off over-voltage. Furthermore, it provides better sinusoidal output load current.

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