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Design of LDPC Decoder Based On FPGA in Digital Image Watermarking Technology

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Abstract

LDPC code and digital image watermarking technology, which is an effective method of digital copyright protection and information security, has been widely used. But this is a multi-disciplinary, multi technology application scheme. In order to realize FPGA design of LDPC decoder in the application scheme, an effective implementation method of digital watermarking application system must be found. In this paper, MATLAB software and Qt development environment are combined to achieve the digital watermarking application software design. It could get real-time input data for the LDPC decoder. Then the hardware of the LDPC decoder is primarily implemented by FPGA in the digital image watermarking system. And the serial port is used to make the output data of the decoder back to computer for verification. Through the simulation results, the Modelsim time simulation diagram is given, and the watermark image compared with the original image is got. The results show that the resource usage of our system is few, and the decoding rate is fast. It has a certain practical value.

Keywords*: LDPC code; FPGA; digital image watermark*

1. Introduction

Low Density Parity Check (LDPC) code, as a kind of channel coding, shows stronger error correction and control ability than the other code, such as Turbo code, BH code and so on. At present, the digital image watermarking technology has been used widely as an effective way for protection of digital copyright and information security. And many researchers had made LDPC code for the digital image watermarking system. Because the LDPC code has strong error correcting ability, its anti-interference ability is much better, compared with the traditional information hiding algorithm. Although the watermarking image suffered a strong attack consequently, it could keep up the lower error rate and get the secret information with lest distortion. In this paper, the digital image watermarking system is performed that the watermark information encoded by LDPC code is embedded into the original image, and could extract the watermark information at receiving end. Then the original watermark image is recovery with LDPC decoding on FPGA, and the embedded watermark image is extracted finally. At first, we use a method of mixed programming with Qt and MATLAB to realize the software of digital image watermarking system.

Qt is provided as a kind of application development framework of cross platform C++ graphical user interface by Trolltech in 1991[1]**.** It could support a variety of operation system platforms, such as Windows, Mac OS, Linux and so on. And it's "written once, compile anywhere", so there are wide adaptability and well portability. In addition, people can download and use freely, because Qt can be obtained by the open source license. Now Qt has evolved into an application development framework from a simple graphical toolkit, which has came into an integrated software development environment. Qt Creator is an integrated development environment of Qt, and it can be operated by cross platform. It includes project wizard, senior C/C++ code editor, compiler, debugger, graphic designer, tools of classes and so on. The development tasks can be completed more quickly and easily by the Qt Creator.

The Qt software has powerful development function. But it provides limited mathematical functions, and has a lack of ability to deal with the complex problems of algorithm. However, MATLAB, as a mathematical analysis tool, has strong ability to do numerical value,

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symbols, matrix calculation, and visualization of calculation results. So MATLAB is a powerful aided design tool of computer. We combine Qt with MATLAB to make up for programming deficiency of Qt singly. One project of the key point of national Th Five-Year Plan of China is used Qt and MATLAB for mixed programming to come true the software design [2]**.** So the mixed programming method with Qt and MATLAB is simple and effective.

The watermark image reduction in the digital image watermarking system is mainly based on the design and implementation of LDPC decoder on the FPGA hardware platform. The large iterative computation quantity is required by LDPC decoder in the decoding process. The speed of software simulation is very slow. However, the large amount of calculation can be quickly realized in the decoding process by FPGA simulation. And the decoding time is reduced greatly. It could reflect the better real communication process and enhance the reliability of system.

2. Design of Digital Image Watermarking System

In this paper, the principle of the digital image watermarking system is encoded the watermark image information by LDPC at first. Then the watermark image is embedded into the original carrier image, and extracted at the receiving end. The original watermark image could be recovered by the LDPC decoder based on FPGA hardware platform. Therefore, this digital image watermarking system is mainly made up of the LDPC code encoding, watermark embedding, watermark extraction and watermark image display. The design of system is divided in two parts, one is the software design of digital image watermarking system based on the mixed programming with Qt and MATLAB, the other is the hardware simulation design of LDPC decoder based on FPGA.

2.1. Realization of Digital Watermark Software

In this paper, the method of mixed programming with Qt and MATLAB is used to realize the software of digital image watermarking system. The main process is as follows.

1. Write M file.

Using MATLAB to generate M files of LDPC code, watermark embedding and extraction algorithm. M files will be saved as ldpcmark.m. And the simulation results demonstrate the program is correct [3]**.**

2. Generate DLL file.

The compiler of MATLAB environment is used to make M file convert into DLL files in order to make M file called by Qt directly. DLL file is a dynamic link library file. When programs are required to perform special tasks, it can allow programs to share the code and other resources. So the DLL profiles can reduce frequency of memory exchange and improve efficiency of code. In the command window of MATLAB, the DLL file is generated by the following command:

Mcc-W cpplib: ldpcmark-T link: lib ldpcmark.m.

Some files are generated, which include header file “ldpcmark.h”, import library file “ldpcmark.lib”, and dynamic link library file “ldpcmark.dll”.

a) The Original Carrier Image

b) The Watermarking Image

Figure 1. The Images Selected in Digital Image Watermarking System Software

3. Call DLL file in Qt to get the system software.

The ldpcmark.dll file can be copied to the output directory directly, and the header file “include” uses extern "C" in the calling program of Qt. The total program is divided into five parts: choose the original carrier image (as shown in Figure 1(a)), select the watermarking image (as shown in Figure 1 (b)), LDPC encoding, embed and extract the watermark. The corresponding procedure is shown in Figure 2.

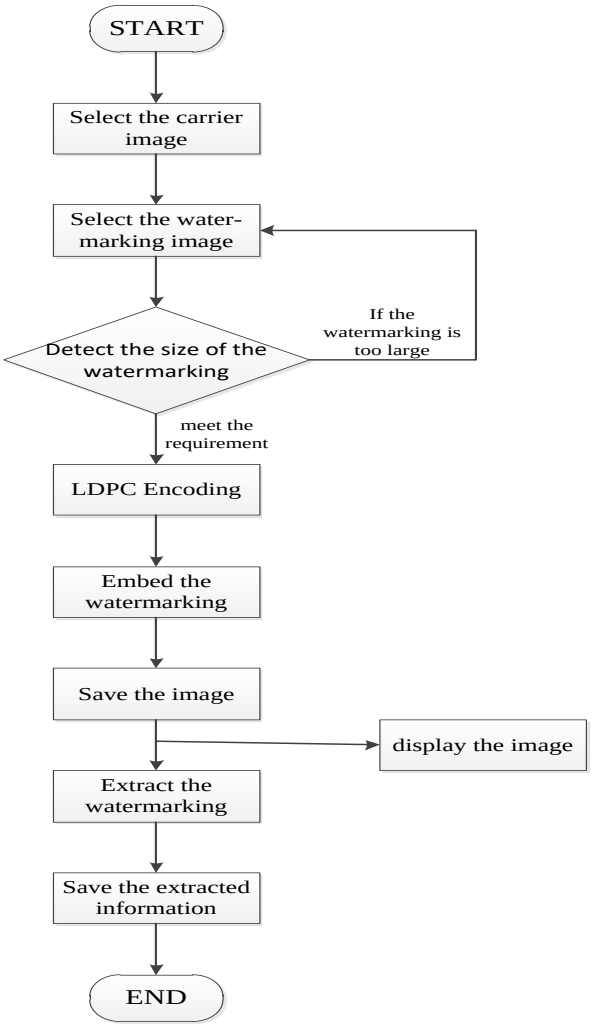

Figure 2. The Operation Flow Chart Of Digital Watermark Software

2.2. Design of LDPC decoder based on FPGA

The Qt software can save the extracted watermarking information. But this information is not decoded by LDPC decoder. The original watermarking image cannot be displayed. Therefore the information as the original data is input to the LDPC decoder implemented by FPGA design. The watermarking estimation value is output by the LDPC decoder, and then transported to computer by serial port. The original watermark image is displayed on the computer.

In the hardware design of FPGA [4-8], all structure of the LDPC decoder is made up of four modules, which are the information input module, variable node processing units (VNU) module, check node processing units (CNU) module, and the information output module [9-11]. Figure.3 is the structure diagram of LDPC decoder in the digital image watermarking system based on the hardware design of FPGA. The whole decoder is based on the hierarchical control implementation which is similar to the operation of assembly line [12]. The control unit is the key

part of decoder, which coordinate all the work of decoder as top-level control. The second layer control is controlled by the input cache, CNU, VNU and the output cache module, etc. And these modules do not interfere with each other. In order to implement the hardware of LLR-BP decoding algorithm in log domain, we choose the binary domain min-max decoding algorithm.

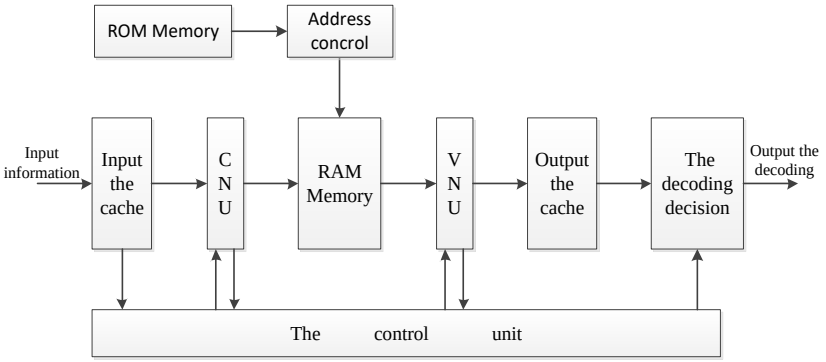

Figure 3. The Overall Design Diagram of LDPC Decoder

The work process of decoder is as shown in Figure 4. The watermarking information after extracted is needed to carry on quantitative analysis to obtained quantitative bit information. The quantitative bit information as the input information is transferred into the input cache module to complete the serial to parallel conversion. Then the information enters into the iteration process. The CNU and VNU module are used to complete the update calculation process of check nodes and variable nodes respectively. At the same time, the information exchange of the variable nodes and check nodes is performed by RAM memory. The output cache module is used to complete the parallel to serial conversion. Finally the information will be input to the decoding module to output the decoding information. The control unit is used for monitoring completion status of the CNU module and VNU module in each iteration process, and determined whether to reach the setting maximum number of iterations. It is also used to control each module startup simultaneously.

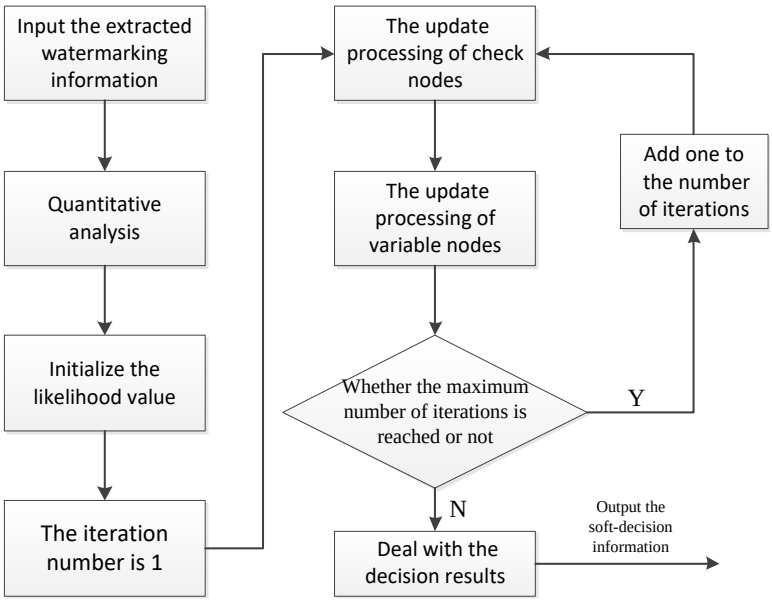

Figure 4 The Flow Chart of LDPC Decoder

2.2.1 The design of the CNU module

Check Node Unit module (CNU) is mainly used for calculating the information of check nodes and variable nodes in LDPC decoder. The data required by the update calculation in the CNU module is the information from the variable nodes to check nodes [13-16]. The degree of check node is set to 6, and 32 configuration sequences will be formed in the CNU module. The schematic diagram of the CNU module is as shown in Figure 5. The first information "0" from check node to variable node is as an example, the operation process of CNU module is as follows:

(1) The last 5 values of the top 16 allocation vectors are replaced with the corresponding variable information.

(2) Get the maximum value of vector information of each configuration, and there are totally 16 maximum values.

(3) Get the minimum value of the 16 maximum values, and the minimum value is parity information transferred the first variable node from the check node.

According to above process, the update calculation process of all check nodes is completed orderly.

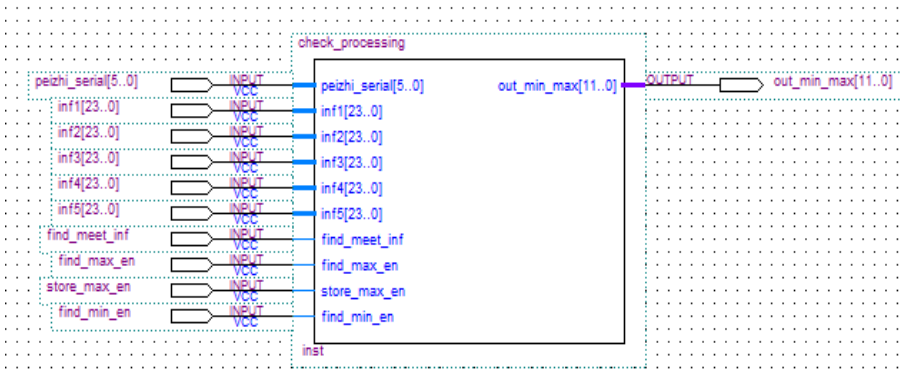

Figure 5. The Schematic Diagram of the CNU Module

2.2.2 The design of the VNU module

The information in Variable Node Unit module (VNU) is the initialization likelihood value and the returning information from check nodes to variable nodes[17-18]. The initial information value is only the value of $L(P_i)$, the remaining values are zero or do not participate in add operation. Figure 6 is the schematic diagram of VNU module which adopts the pipeline design. The degree of variable node is set to 3. The VNU module has three inputs, which are variablein_1, variablein_2, and variablein_3 respectively. The initialization likelihood value of the channel is In. The initialization phase would output the value of In directly. The soft-decision decoding will be updated in each iteration process. The role of Subtraction is to minus own information carried in the minimum values. The iteration number is set to10 in this design.

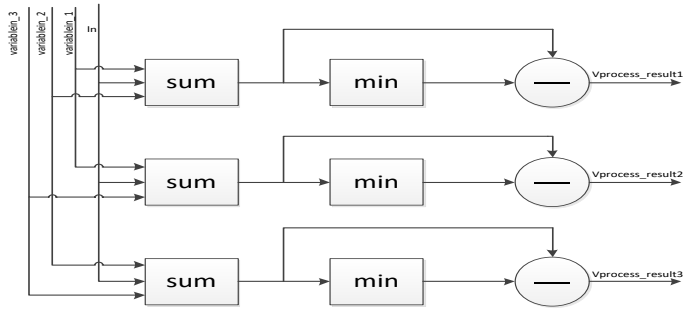

Figure 6. The Schematic Diagram of the VNU Module

3. Results and Discussion

3.1. The Output Information of LDPC Decoder

While the LDPC decoder [19-21] reaches a maximum number of iterations in the update calculation process of information, the read enable of main control of the decoder can decide to output the decoding information. After all the decoding information are read over, the order "code_out_over =1" would be executed by the decoder. Figure 7 is the decoding output information of the decoder.

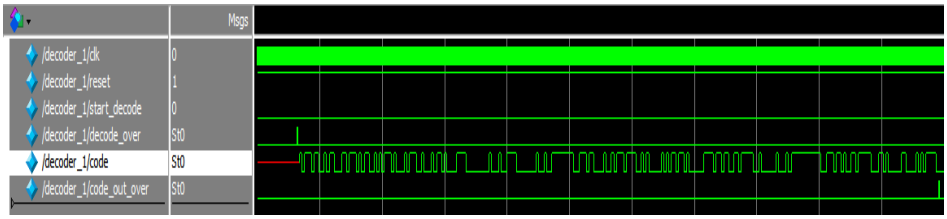

Figure 7. The Decoding Output Information of Decoder

3.2. The Results of Digital Image Watermarking System Test

The output data of the decoder is returned to the computer by the serial port, which can display the image. And the output image can be obtained as shown in Figure 8 (a). By the contrast of the original watermark image (as shown in Figure 8 (b)), the result shows that the hardware design of LDPC decoder based on FPGA is correct in the digital image watermarking system.

(a) (b)

Figure 8 The Test Chart of LDPC Decoder based on FPGA

4. Conclusion

A digital image watermarking system is researched in this paper. This system is made up of 4 parts: the LDPC code encoding, watermark embedding, watermark extraction and watermark image display. The system software is realized by the mixed programming with MATLAB and Qt at first. It could get real-time input data for the LDPC decoder. The hardware of the LDPC decoder is primarily implemented by FPGA in digital image watermarking system. And the serial port is used to make the output data of decoder back to computer for verification. Through the results of system test, the Modelsim time simulation diagram is given. And the watermark image compared with the original image is got. They are almost the same. This digital image watermarking system has a certain practical value.

In addition, the hardware resource consumption of LDPC decoder is larger and the throughput is not high enough. So it needs to further optimize the existing decoding algorithms, and the hardware design should realize the maximum module reuse in order to deal with the relationship between resources and the speed.

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