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The Performance of an Integrated Transformer in a DC/DC Converter

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Abstract

The separation between the low-voltage part and high-voltage part of the converter is formed by a transformer that transfers power while jamming the DC ring. The resonant mode power oscillator is utilized to allow elevated competence power transfer. The on-chip transformer is probable to have elevated value inductance, elevated quality factors and elevated coupling coefficient to decrease the loss in the oscillation. The performance of a transformer is extremely dependent on the structure, topology and other essential structures that create it compatible with the integrated circuits IC process such as patterned ground shield (PGS). Different types of transformers are modeled and simulated in MATLAB; the performances are compared to select the optimum design. The on-chip transformer model is simulated and the Results of MATLAB simulation are exposed, showing an excellent agreement in radio frequency RF.

Keywords*: On-Chip Transformer, Radio Frequency, Integrated Circuits*

1. Introduction

The on-chip transformers donate considerably in enhancing consistency, efficiency, and presentation of silicon-integrated radio-frequency (*RF*) circuits. Newly, much investigate has focused on the design and characterization of integrated transformers. Transformers are characteristically used for impedance matching and adaptation between differential and single-ended signals (balun process), power combining, and tuning networks. Many researchers have reported the integration of on-chip transformers in power amplifiers (*PAs*), voltage controlled oscillators (*VCOs*), and low-noise amplifiers (*LNAs*) [1-6].

The transformer separates the secondary face (output) from the primary face (input) electrically, modeling two DC voltage fields that can have varied supply rails. This broken ground loop will defend the low-voltage face circuits from the electrical upset and over-voltage hazards caused by the high-voltage face circuit's action. In addition, the noise conducted in the ground will be removed. The converter consists of *DC* supply, oscillator, rectifier and regulator. The oscillator converts the fixed *DC* voltage to alternating *AC* voltage and therefore the *AC* current pouring from side to side the primary winding of the transformer. The diverging current produces diverging magnetic flux in the center (comprising air center) which persuades a varying electromotive power or voltage athwart the secondary face winding. For this cause, the primary face *DC* constituent cannot pass from side to side the transformer and have an impact on the secondary winding, and neither the secondary winding to the primary winding. After transitory from side to side the transformer, the *AC* voltage is corrected by the rectifier and then a not obligatory controller to the *DC* voltage over. For RF transformers, there are some models now obtainable in the literature. Rotella et al., [7] present an electrical model that takes into explanation the transformer and its parasitics, and Biondi et al., [8] and Wang et al., [9] also comprise analytical expressions to calculate some of its components. Likewise, El-Gharniti et al., [10] present an even more comprehensive model containing the equations to calculate each one of its elements. This model is shown to be scalable to geometric dimensions and different technologies.

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In the on-chip transformer, the main intent is the remove of power from primary to secondary windings. Thus the transformer efficiency can be cleared as the ratio of the output power (distributed to the load) to the input power. In vision of the confidence of this ratio on the extinction impedances, an extra useful choice of figure (topology and structure) of merit for RF transformers is the lowest insertion loss, which is defined as the opposite of the most coupling coefficient and quality factor. Therefore, information to optimize high performance on-chip transformer with desired inductance, quality factor and coupling coefficient *K* is very significant. In the past a few decades, great labors have been loyal to the modeling, optimization and design of the on-chip transformer on silicon substrates [11-13]. The approaches, such as using diverse structures planar type or stack type [14], and diverse geometry octagonal type or square type [15], and patterned ground shields between metal conductors and the silicon substrate [16, 17], have been reported. However, to the author's best knowledge, less effort has been found to systematic studies on the performance trends of transformer varying with different structure and topology.

In this paper, we present design of integrated on-chip transformers for power *ICs* application and analytical model for on-chip transformers that is suitable for circuit simulation. We also provide simple expressions for calculating the inductance value, quality factor value and coupling coefficient and these topology and structures transformer of merit. Finally, simulation results will be compared with measured results.

2. Presentation of the Transformer

Figure 1 shows an ideal transformer circuit model. The transformer can be treated as an electromagnetic power converter [18] which consists of two or extra magnetically joined windings. A time-varying voltage practical at the primary face causes a time-varying current to run, thus reasoning a varying magnetic flux in the center. The varying magnetic flux will stimulate a voltage at the secondary face. The center, for most of the small frequency applications, is made of ferromagnetic metals which have superior permeability that augment the magnetic field. Though, for elevated frequency applications like our case, the ferromagnetic center is not well-matched with the course and will have magnetic saturation and core losses which debase the quality factor of the transformer.

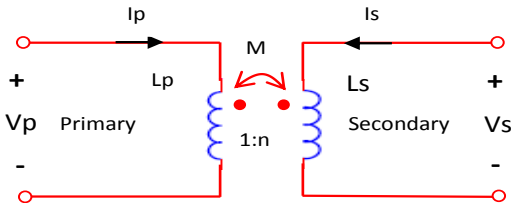

Figure 1. Ideal Transformer Circuit Model

The ideal transformer model can be treated as a two port network with the nexting terminal voltages and currents liaison:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} jwL_p & jwM \\ jwM & jwL_s \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (1)$$

Where *Lp* and *Ls* are the self-inductance of the primary and secondary face winding. *M* is the mutual inductance among the two windings. For ideal transformer, the power transmits will be lossless and magnetic flux is restricted in the magnetic center [18, 19], thus the nexting identity holds:

$$\frac{I_s}{I_p} = \frac{V_p}{V_s} = \frac{N_p}{N_s} = n = \sqrt{\frac{L_p}{L_s}} \quad (2)$$

Where *Ip* and *Is* are the current flowing through the primary and secondary winding, *Vp* and *Vs* are the primary and secondary voltage, *Np* and *Ns* are the primary and secondary number of turns, *n* is for the turns ratio of transformer. An additional important parameter to characterize a transformer is the coupling coefficient *K* which is defined by:

$$K = \frac{M}{\sqrt{L_P . L_S}} \tag{3}$$

If the two windings are completely joined, *K*=1. Due to the leakage of magnetic flux reasoned by a lack of high permeability magnetic center in practical, the *K* for most on chip transformers is in the range of 0.3~0.9 [20-25].

3. Transformer Modeling and Simulation

According to the metal losses and substrate losses, we build a practical transformer model that mimics the performance of on-chip transformer at high frequencies shown in Figure 2(a). The model has resistance in series to mimic the metal loss of the inductor (*Rp* and *Rs*). Other than mutual inductance *M*, the model also illustrates the mutual capacitance effect by *C* since the two windings are isolated by silicon-dioxide and the capacitor can be formed. *Cp* and *Cs* illustrate the terminal-to-terminal capacitance which may short the inductor at high frequencies. To emulate the substrate loss, the block consisting C_{OX}, C_{SUB} and R_{SUB} is used which shows the substrate current loss and capacitive coupling between the windings and the substrate [26-31].

Although we can build circuit model consisting of resistors, capacitors and inductors to emulate the on-chip transformer for a certain frequency variety, it is motionless hard for employ the model and relying on the simulation results of this model since the values for the resistance, capacitance and inductance are not easily.

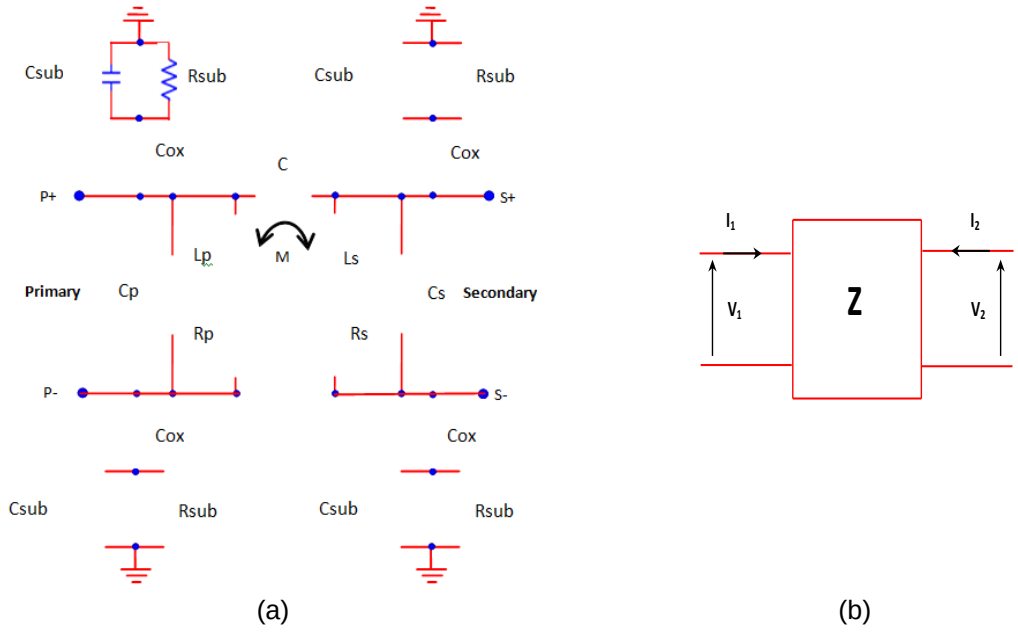

Figure 2. (a) A Practical Transformer Model. (b) Simplified model for transformer

The specifications of the transformer can be calculated by the Z-parameters matrix shown in Figure 2(b). Between which we heart on the winding inductance *L*, quality factor *Q* and coupling coefficient *K*. In the simulation, we set the primary face port to be port 1 and the secondary face port to be port 2. Thus the specifications can be calculated by:

$$L_p = \frac{\mathrm{Im}(Z_{11})}{2.\pi.f} \quad (4)$$

$$L_s = \frac{\mathrm{Im}(Z_{22})}{2.\pi.f} \quad (5)$$

$$Q_p = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \quad (6)$$

$$Q_s = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})} \quad (7)$$

$$k = \sqrt{\frac{\mathrm{Im}(Z_{12}).\mathrm{Im}(Z_{21})}{\mathrm{Im}(Z_{11}).\mathrm{Im}(Z_{22})}} \quad (8)$$

Where *Lp*, *Ls*, *Qp*, *Qs* and *K* are respectively for the primary inductance, secondary inductance, primary quality factor, secondary quality factor and coupling coefficient between the two windings.

3.1. Structure Comparison: Planar Transformer and Stacked Transformer

The on-chip transformers can be classifying into two types agreement to the structure: planar transformer and stacked transformer. To evaluate the performance in our frequency range, we build one stacked transformer and one planar transformer.

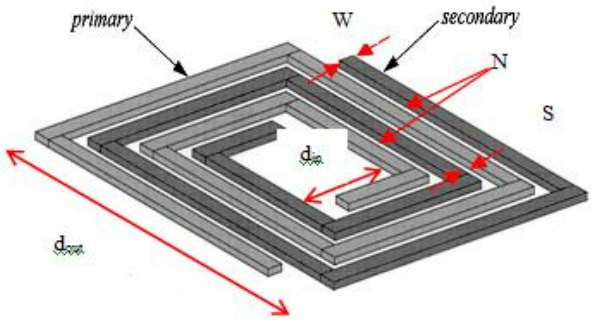

Figure 3. Horizontal Geometry of the Planar Transformer

For the flat geometry, we introduce the parameters: number of turns *N*, outer dimension d_{out}, and inner dimension d_{in}, trace width *W* and adjacent trace separation *S* to describe the geometry of the spiral winding, the definitions of these parameters are shown in Figure 3.

The simulation results (1 at 8 GHz) are shown in (Figure 4(a), (b), (c), (d), (e)). The simulation results illustrate that the stacked transformer gives upper primary winding inductance with a lesser covering region comparing to the planar transformer. However, the quality factor for primary winding is quite low comparing to the planar transformer. This is because the primary winding is fabricated using metal layer thick making the series resistance quite large. Besides, the coupling coefficient of stacked transformer is lesser than planar transformer, which is caused by the increased separation between the two windings due to the sandwiched layer for underpasses and the thick oxide layer. As a result, we should use planar transformer for better quality factor and better coupling coefficient.

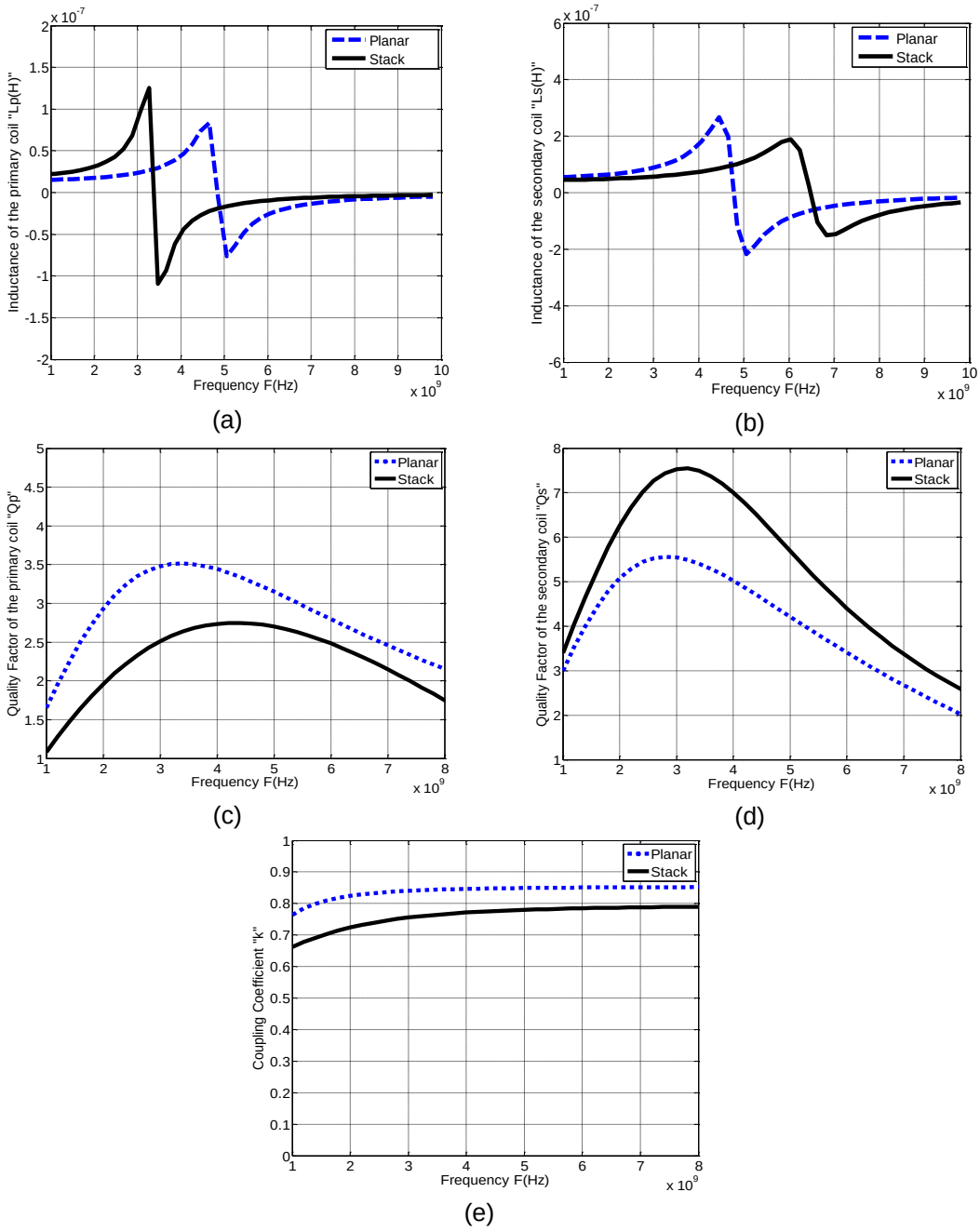

Figure 4. Simulation Results: Stacked and Planar Transformers: (a) Primary inductance *Lp*, (b) Secondary inductance *Ls*, (c) Primary quality factor *Qp*, (d) Secondary quality factor *Qs*, (e) coupling coefficient *K* as a function of frequency and structure transformer.

3.2. Topology Comparison: Octagonal Transformer and Square Transformer

We simulated these two models in the frequency variety that two topology transformer (octagonal and square). For both of the transformers, *Np*:*Ns*=4:3, d_{out}=1850µm, d_{in}=842µm, *Wp*=51µm, *Ws*=50µm,S_{Pri}=45µm, S_{Sec}=42 µm.

The simulation results (1 at 10 GHz) are exposed in (Figure 5.(a),(b),(c),(d),(e)) as under. The simulation results illustrate that the coupling coefficient of the two type transformers (Octagonal, Square) is shut to every other. The square topologie has a primary inductance 2,5nH and secondary 5.2nH higher than the octagonal topologie. The involvement of the mutual inductance between the segments in the square topologie is important comparing to the longer

trace length and larger casing region of the octagonal topologie. For quality factors comparison, square topologie is superior to the octagonal topologie. Therefore, we prefer the square topologie to get superior inductance and inferior losses.

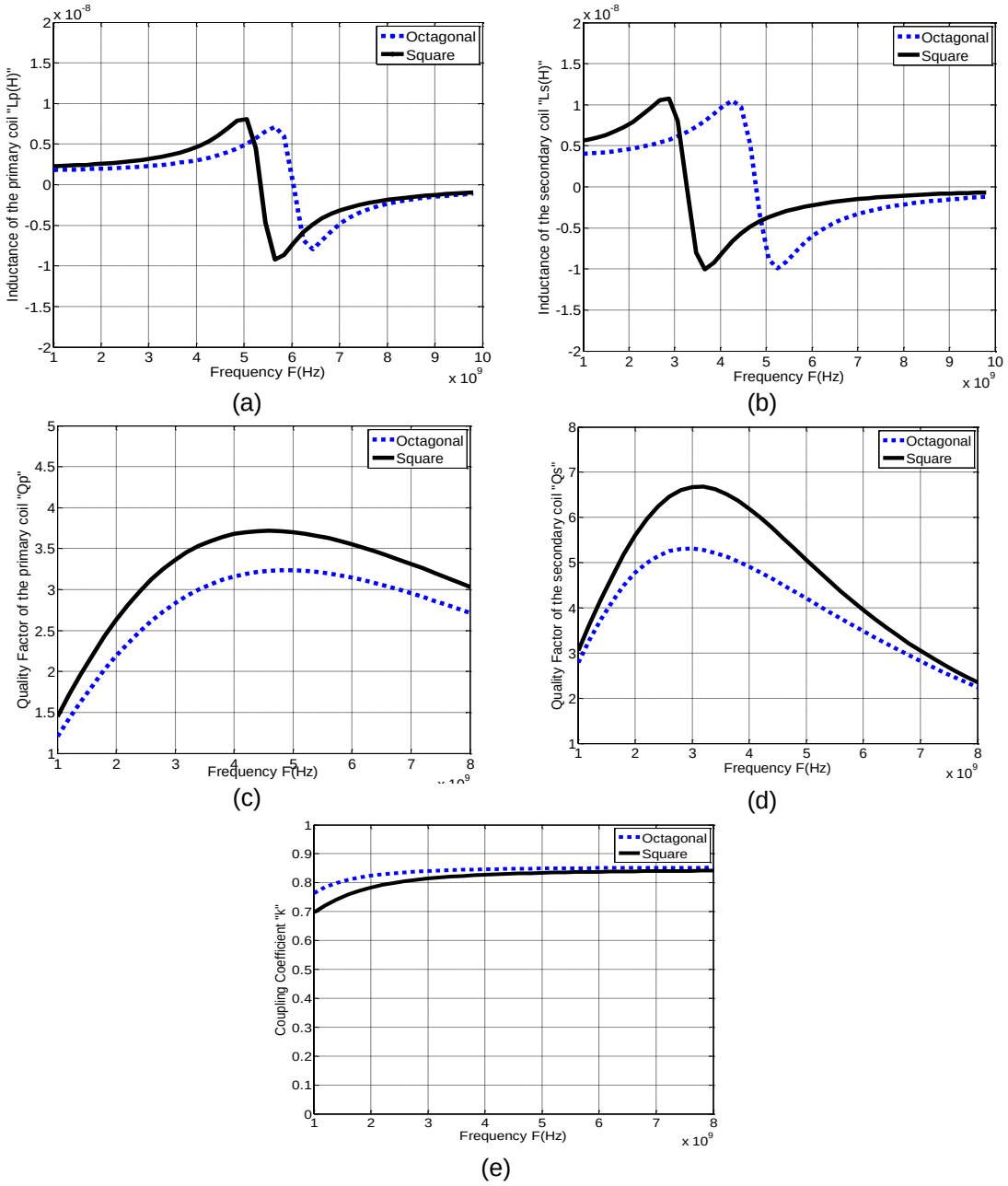

Figure 5. Simulation Results: Octagonal and Square Transformers: (a) Primary inductance *Lp*, (b) Secondary inductance *Ls*, (c) Primary quality factor *Qp*, (d) Secondary quality factor *Qs*, (e): coupling coefficient *K* as a function of frequency and topology transformer.

3.3. Patterned Ground Shield (PGS)

At superior frequencies, the magnetic field created by the transformer will make eddy current on the failure substrate. To diminish the failure, we require a ground shield to decrease the eddy current and supply a ground correlation. Thus, a *PGS* is frequently built beneath transformers for elevated frequency functions. To notice the influence of the *PGS* in our

transformer, we built 3 models for simulation: (1) transformer not including a *PGS*; (2) transformer with a metal *PGS* and (3) transformer with poly-silicon *PGS*.

The simulation results (1 at 10 GHz) are exposed in (Figure 6). From the simulation results we view that the transformers with *PGS* have a superior inductance value comparing to the not including a *PGS*; for transformers with metal *PGS*, the quality factor will be degraded comparing to the one with poly-silicon *PGS* and the not including a *PGS*. The explanation for this degradation is that the metal layer sits faster to the winding layer than the poly-silicon, creating a superior capacitance with the winding. The parasitic capacitance will debase quality factor. As a result, we employ a poly-silicon *PGS* in our design.

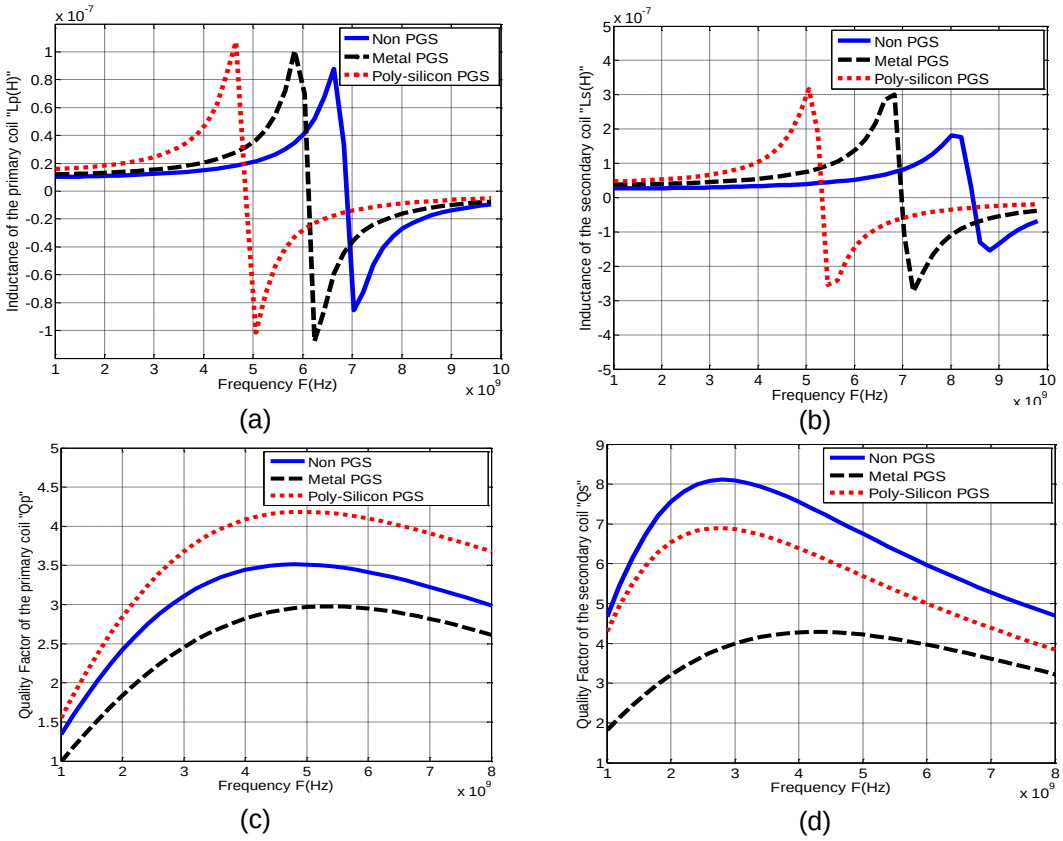

Figure 6. Simulation Results: without *PGS*, with Poly-Silicon *PGS* and with Metal PGS: (a) Primary inductance *Lp*, (b) Secondary inductance *Ls*, (c) Primary quality factor *Qp*, (d) Secondary quality factor *Qs* as a function of frequency and *PGS* effect

4. Comparison of the Simulation Results and the Measurement Results

The dimension of the transformer is 0.2cm by 0.23cm. The group analyzer sweeps the frequency from 1GHz to 10GHz to measure the Z-parameters [32]. The writing converts the Z-parameters to S-parameters and calculates the *K*, *Q* and value inductance.

The simulation extensive frequency variety is from 1GHz to 10GHz to make it comparable with the measurements.

The data at 2 GHz is shown in (Table 1). We can observe that the difference between the measurement and simulation results.

Table 1. Measurement and Simulation Results Comparison

	K	*Lp*	*Ls*	*Qp*	*Qs*
Measurement	0.52	21.5nH	52.2nH	4.5	4.1
Simulation	0.71	28.2nH	71.0nH	4.1	4.9

We can observe that the coupling coefficient decreases to 0.52 at around 2GHz, which is much inferior to the simulation results. The motive for this disagreement is the additional inductance involvement of the converter and the transformer routing traces.

5. Conclusion

An on-chip transformer for a *DC*/*DC* Converter is enlarged. To obtain a precise model, the MATLAB simulation is used to design and simulate the transformer model. The simulation results on coupling coefficient, inductance value and quality factors value of different structures, topology formes are compared to choose the best design that is compatible with the integrated transformer in a converter. The planar structure with square topologie is chosen for superior quality factor and inductance value. Further influence such as *PGS* is also simulated. *PGS* prepared by poly silicon layer shows an in good health result in the sense of elevated quality factor and inductance. The measurement is presented by network analyzer and the result is compared with the simulation result of the model that has on-chip transformer. The simulation results show a good consistency with the measurement.

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