TELKOMNIKA, Vol.12, No.4, December 2014, pp. 779~786
ISSN: 1693-6930, accredited **A** by DIKTI, Decree No: 58/DIKTI/Kep/2013
DOI: 10.12928/TELKOMNIKA.v12i4.506

Non-Planar MOSFET Modeling with Analytical Approach

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Abstract

Non-planar structures have been identified as promising structure for next device generation in the nanoelectronic era. However, the continuous device dimension scaling into nano regime eventually requires more sophisticated model due to the limitation of the existing models. A model for non-planar MOSFET structure was elaborated in this paper, especially for device with pillar structure, using analytical approach. The concern of channel shape and structure were discussed as well. The result shows the shift in subthreshold characteristic in the channel with recessed channel model. The charge sharing is suspected as one of the key parameter in the shift of performance in the recessed region.

Keywords*: non-planar MOSFET, nanoscale, analytical model, surface potential, short channel effect*

1. Introduction

The rapid development of MOSFET have shown a tremendous progress in downscaling the dimension and structure as well into nanoscale. The continuous scaling of the device dimension has now reached tens of nanometer size especially for the channel length of transistors. With the smaller device dimension, it is getting impossible to maintain the conventional bulk structure legacy, as shown by International Technology Roadmap for Semiconductor (ITRS) [1]. Several future devices with non-conventional structure have been proposed to overcome the conventional MOSFET structure limitations, as example in [2]-[8]. The non-planar MOSFET is expected to expand the Moore’s law. Several structures could shift the downsizing off the lithography and obtain self-aligned multi gate which is hard to produce with conventional one.

On the other hand, several fabrication methods produces various channel shapes, Some methods result in straight channel between source and drain, while some others create such a bending channel, a combination of vertical and recessed horizontal direction of current. For example, several geometries may be found in non-planar double gate MOSFET. Figure 1(a) reveals the recessed channel with L-shaped geometry due to the presence of corner that diverts the direction of current from drain to source. The second geometry, shown in Figure 1(b), offers the possibility of direct flux. This body-tied geometry have its channel connected to the substrate potential. The floating body channel (Figure 1(c)) reveals simple double gate structure but with its channel potential isolated electrically from the substrate.

Several models that simulate the physics of the vertical devices have been published recently. However, many authors focused on the ideal non-doped double-gate/surround gate MOSFET structure [9]-[11]. Others modeled the highly doped MOSFET with the help of regional model [12],[13] or depletion charge [14] as well as with conformal mapping [15]. However, the analytical model for non-ideal junction structure, as well as recessed channel, has not been well articulated in previous publications. In the conventional MOSFET, the recessed gate is known for its ability to prevent short channel effect, but in the vertical geometry, the recessed channel is somewhat different with that of conventional. The simulation of recessed gate in vertical MOSFET geometry has been presented in [16], but it is mainly concentrated for vertical surround gate, and no analytical model was offered.

Received September 22, 2014; Revised November 10, 2014; Accepted November 22, 2014

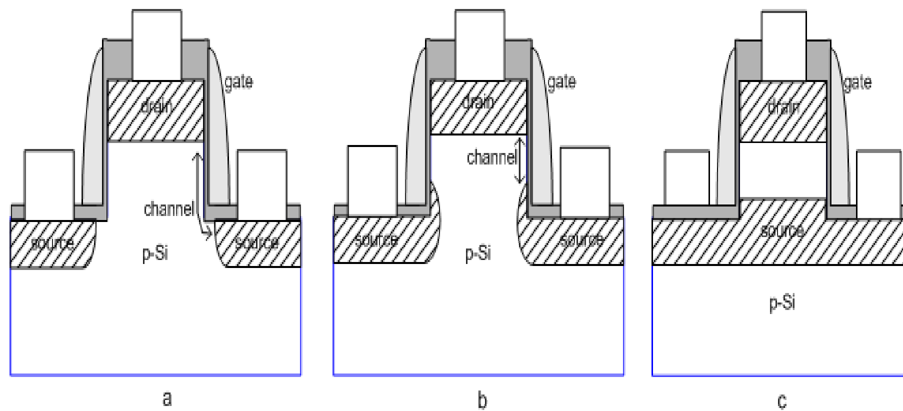

Figure 1. The variation of channel geometry in non-planar DG MOSFET: (a) recessed, L-shape channel, (b) body-tied channel, and (c) floating-body channel

Therefore, in order to explain the behaviour of channel with different shape and potential profile, it is important to derive the appropriate model. In addition, the continuous scaling of device requires applicable model in nanoscale. This paper elaborates the analytical model of non-planar MOSFET which employ the recessed channel geometry in the bottom part. The corner effect is elaborated extensively, with the help of approach that has been provided for conventional model [17]. In addition, the preceeding reports on this model have also been reported in [18]. This extended report provides more evaluation on the short channel effects which are crucial in the nano regime.

2. Analytical Model

The structure of recessed channel in non-planar MOSFET can be seen in Figure 2. This typical structure is an ideal form of the fabricated devices. The straight channel potential model is derived from Poisson equation using generic approach as noted in several references, e.g. [10],[19]-[22]:

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \quad (1)$$

Moreover, the presence of corner region in the bottom is arguably difficult to solve using two-dimensional Poisson equation in Cartesian system. Therefore, we divide the channel into two regions: first is the straight and latter is the corner region. We simplify the corner region as a quarter circle, an approach adopted from Zhang et al [17] for grooved gate in conventional MOSFET. However, Zhang's model used trapezium-shape approach, while our model employs quarter-circle approach which is more realistic.

The uniformed depletion width x_d is calculated using the following formula:

$$x_d = \frac{D_A}{L} \quad (2)$$

D_A is the total depletion region area as in [23], as simplification of depletion width towards all area mainly due to the gate influence.

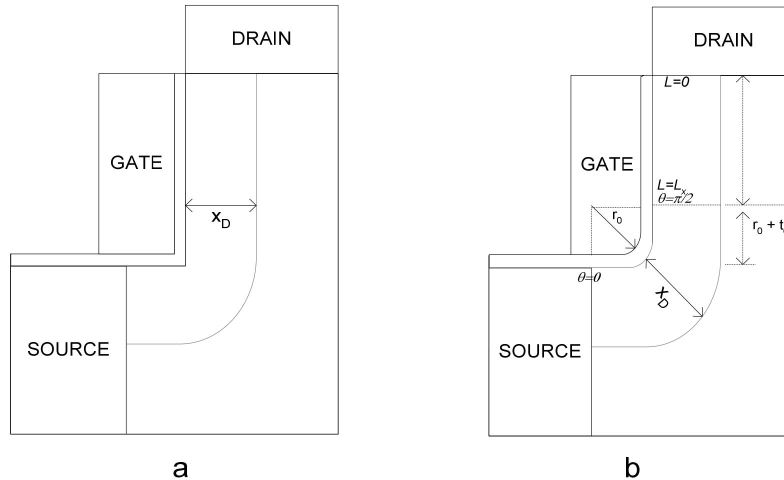

Figure 2. The structure of recessed channel in vertical geometry (a), and its approach using two-region solution (b)

The potential of channel for each region is following the two dimensional second-order parabolic approach of graded channel approximation (GCA) that originally proposed by Young [24]. However, for corner area, the parabolic approximation is adopted to the cylindrical coordinate system as was used in [17]. The potential for both cartesian and polar coordinate systems are:

$$\Psi_{st}(x,y) = \phi_s(x) + C_{11}(x)y + C_{12}(x)y^2 \quad (3)$$

$$\Psi_{cr}(r,\theta) = C_{20}(\theta) + C_{21}r + C_{22}r^2 \quad (4)$$

The notation "*st*" stands for "straight", to differentiate with "*cr*" for "corner". In solving the differential Poisson equation using general parabolic approach, several boundary conditions are set, which are applied to both regions (for polar coordinate, x and y should be replaced with θ and r, respectively):

The electric field in the silicon-oxide interface is according to Gauss' law [23]:

$$-\frac{\partial\psi_s}{\partial y}\bigg|_{y=0} = \frac{C_{ox}}{\epsilon_{si}}(V_{gn} - \phi_s(x)) \quad (5)$$

(i) The potential at depletion layer is equal to the substrate potential, for body-tied channel to the V_{sub} :

$$\psi_s(x, x_d) = V_{sub} \quad (6)$$

(ii) The electric field in the depletion layer is:

$$\frac{\partial\psi}{\partial y}\bigg|_{y=x_d} = 0 \quad (7)$$

All parameters are put and later the potential equation is rewritten as:

$$\psi_{st}(x,y) = \frac{V_{sub}y^2}{x_d{}^2} - \frac{V_{g1}y\epsilon_{ox}}{t_{ox}\epsilon_{si}} + \frac{V_{g1}y^2\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}} + \left(1 - \frac{y^2}{x_d{}^2} + \frac{y\epsilon_{ox}}{t_{ox}\epsilon_{si}} - \frac{y^2\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}}\right)\phi_{s1}(x) \quad (8)$$

Similarly for the corner area, with inner radius $r_0 = L_{lateral} - t_{ox}$, depletion depth $r_d = r_0 + t_{ox} + x_d$ and capacitance of cylindrical tube $C_{ox} = \epsilon_{ox}/(r_0 \ln[1 + t_{ox}/r_0])$ as derived in

[25], by borrowing quarter circle approach of grooved channel, solving all boundary conditions for corner area's potential result in [17]:

$$\Psi_{\mathrm{cr}}(r,\theta) = \mathrm{V_{sub}} - M\left(\frac{r^2-2r(r_0+t_{ox}+x_d)+(r_0+t_{ox}+x_d)^2}{2r_0x_d}\right) * \left(V_{g1} - \varphi_{s2}(\theta)\right) \quad (9)$$

where:

$$M = \frac{\epsilon_{ox}}{\epsilon_{si}}\ (1/\mathrm{Ln}[1 + t_{ox}/r_0]) \quad (10)$$

Eq. 9 shows that the potential equation throughout the corner are dependent of r_0, which represent the length of recessive part of the channel. By substituting potential equation $\psi_{st}(x,y)$ of Eq. 8 back into Poisson's equation, a differential equation of potential in straight channel is obtained:

$$\frac{qN_A}{\epsilon_{si}} = \frac{2V_{sub}}{{x_d}^2} + \frac{2V_{g1}\epsilon_{ox}}{t_{ox}x_d\epsilon_{si}} - \frac{2(x_d\epsilon_{ox}+t_{ox}\epsilon_{si})}{t_{ox}{x_d}^2\epsilon_{si}}\phi_{s1}(x) + \frac{(x_d-y)(x_dy\epsilon_{ox}+t_{ox}(x_d+y)\epsilon_{si})}{t_{ox}{x_d}^2\epsilon_{si}}\phi_{s1}^{''}(x) \quad (11)$$

Similarly for corner area, the surface potential $\varphi_{s2}(\theta)$ of Eq. 9 is substituted into Poisson's equation for polar coordinate [17]:

$$\frac{d^2\Psi}{dr^2} + \frac{1}{r}\frac{d\psi}{dr} + \frac{1}{r^2}\frac{d^2\Psi}{d\theta^2} = \frac{qN_A}{\epsilon_{Si}} \quad (12)$$

which result in [17]

$$\frac{V_{g1}-\varphi_{s2}(\theta)}{{\lambda_2}^2} + {\varphi_{s2}}^{''}(\theta) = \frac{qN_A}{\epsilon_{si}}\frac{(r_0+t_{ox})x_d}{{\lambda_2}^2M(r_0+t_{ox}-x_d)} \quad (13)$$

It is noteworthy that Poisson equation of both regions as expressed in Eqs. 10 and 12 can be rearranged in the generic second-order differential equation formula [26] which has the common form of:

$$\phi_{s1}^{''}(x) - \frac{\phi_{s1}(x)}{{\lambda_1}^2} = \beta_1, \text{for straight} \quad (14)$$

$$\varphi_{s2}{}^{''}(\theta) - \frac{\varphi_{s2}(\theta)}{{\lambda_2}^2} = \beta_2, \text{for corner} \quad (15)$$

The respective boundary conditions for both regions can be defined as:

(i) $\Psi_{\mathrm{st}}(0,0) = \phi_{s1}(0) = V_{bi} + V_{ds}$

(ii) $\Psi_{\mathrm{st}}(L_x,0) = \phi_{s1}(L_x) = V_p = \varphi_{s2}(0)$

(iii) $\varphi_{s2}\left(\frac{\pi}{2}\right) = V_{bi} + V_{sub}$

(iv) $\left.\frac{\partial\phi_{s1}}{\partial x}\right|_{x=L_x} = \left.\frac{\partial\varphi_{s2}}{r\partial\theta}\right|_{\theta=0}$ (16)

Threshold voltage V_T is determined when the value of minimum surface potential is twice the Fermi potential $\varphi_{s,min} = 2\phi_F$. Thus, the location of the minimum potential along the surface in the channel obeys the expression:

$$\left.\frac{\partial\phi_s}{\partial x}\right|_{x=x_{min}} = 0 \quad (17)$$

By solving the boundary conditions and calculating the location of minimum potential in each regions, the threshold voltage can be determined from the minima of both regions.

3. Results and Analysis

The structure of straight channel with no corner effect was simulated as well as the recessed structure. The surface potential of recessed and non-recessed channel are shown in Figure 3 as a function of channel length for a fixed recessed length, L_{rec}=10 nm. For the body-tied structure, the body of channel outside the depletion region is assumed to have the potential of substrate, V_{sub}. Meanwhile, Figure 4 shows the surface potential with the recessed channel is limited to around 15% of the total channel length *L*. It is notable that the minimum surface potential is located in the straight region for L_{rec} < 40% *L*.

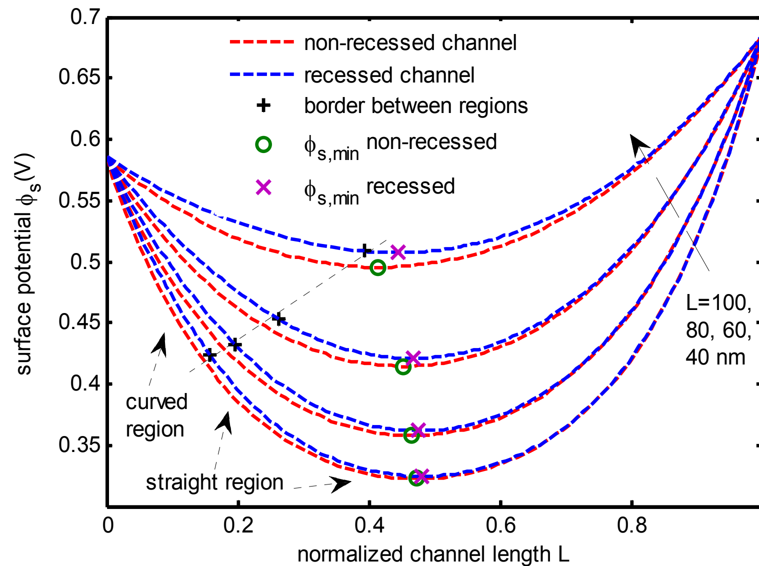

Figure 3. The surface potential for recessed and non-recessed channel. the length recessed part are constant (10 nm), V_{ds}=0.1 V. t_{ox} = 3 nm, V_{gs}=0.1V

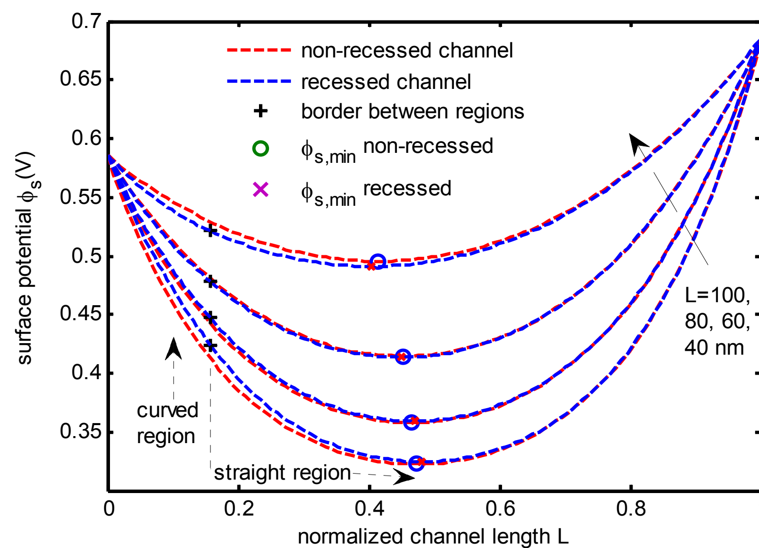

Figure 4. The surface potential as a function of normalized channel length, with the recessed region length are 15% of L. V_{ds}=0.1 V. t_{ox} = 3 nm, V_{gs}=0.1V

Figure 5 reveals the extracted threshold voltage for both structures with L_{rec} = 15% L, V_{ds}=0.1 V, N_A= 10^{18} cm^{-3}, t_{ox}=2 nm. The threshold voltage shows the tendency of decreasing in shorter channel, as is expected due to short channel effect. In addition, the straight channel obtains lower V_T than the recessed channel. In any application with the usage of low V_{DD} which is commonly found in low-power nano IC, lower threshold voltage is required for a better switching operation, which can maintain the lower drain voltage as well. Furthermore, lower V_T may produce higher current drive for operations with high power.

Physically, the curved channel structure lacked the gate control in the corner region. The similar phenomenon is also found in grooved channel in planar MOSFET, as in [27],[28]. The lack of gate control produces decreased potential in the corner area compared to the straight channel. It also prevents the quick conversion into inversion in the channel beneath the oxide layer, with the charge slowly respond to the gate voltage. As a result, higher threshold voltage is needed in the recessed channel.

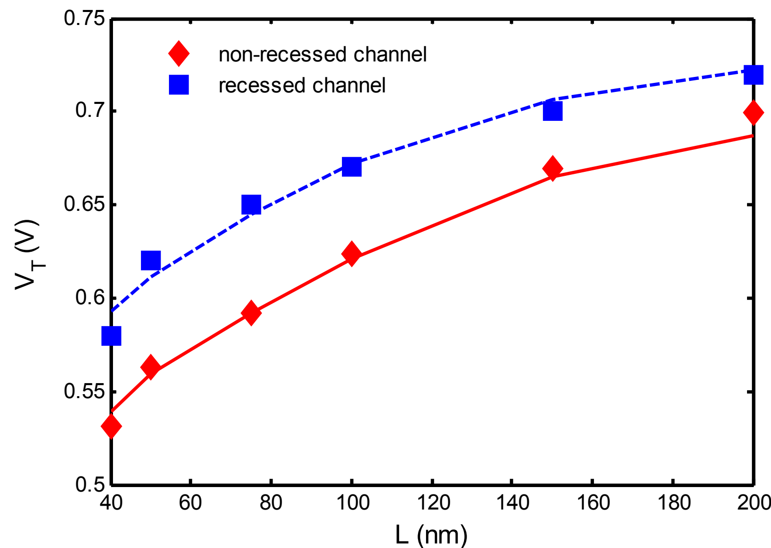

Figure 5. The threshold voltage due to short channel effect

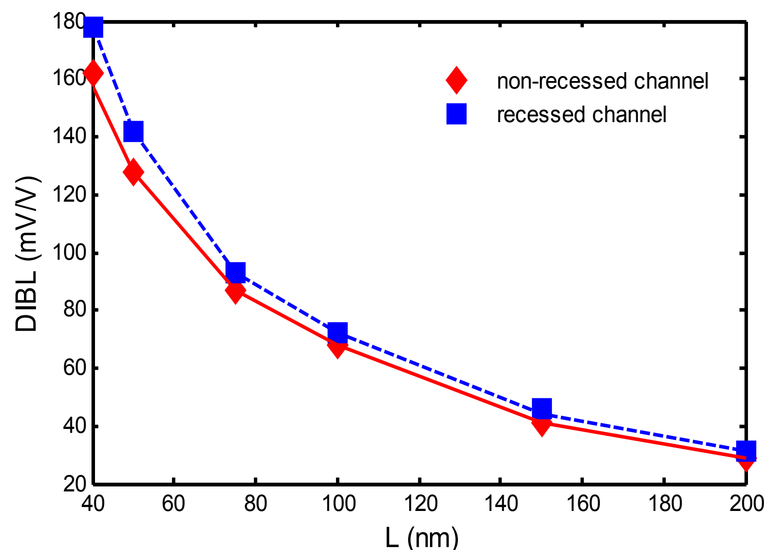

Figure 6. The drain-induced barrier lowering for recessed and non-recessed channel, at V_{ds}=0.1 and 1.0 V

In the presence of higher drain voltage, the control of charge inversion is affected. The value of DIBL is shown at Figure 6, calculated for at V_{ds}=0.1 and 1.0 V. The curved channel suffers from higher DIBL in short channel compared to the straight one. The curved channel has a higher potential barrier at the drain end, but the increase of drain potential suppresses this barrier height more than in the straight counterpart. With the benefit of lower DIBL at short channel, and more acceptable threshold value in nanoscale device operation, the option of straight channel is more preferable than that suppressed channel counterpart. Therefore, the ORI-based vertical MOSFET offers advantages in the short channel regime.

4. Conclusion

The non-planar MOSFET structure with recessed channel has been modeled analytically using parabolic approach. Two distict region representing different channel shape were applied for the ease of model. The simulation based on the developed model shows the shift of threshold voltage due to the presence of the recessed part in the corner. In addition, the DIBL reveals the tendency of increasing in the lower channel length, as a manifestation of the short channel effect. While the straight channel offers lower threshold voltage, the higher DIBL is found for recessed channel. The result reveals the implication of the usage of pillar for non-planar structure, which requires more careful design in the future for threshold-sensitive application .

References

[1] ITRS. *International Technology Roadmap for Semiconductors (ITRS).* 2013. Available: http://www.itrs.net/reports.html

[2] T. Endoh, et al. Sub-10 nm Multi-Nano-Pillar Type Vertical MOSFET. *IEICE Transactions on Electronics.* 2010; E93-C: 557-562.

[3] A. Sugimura, et al. Proposal of Vertical-Channel Metal Oxide Semiconductor Field-Effect Transistor with Entirely Oxidized Silicon Beam Isolation. *Japanese Journal of Applied Physics.* 2009; 48.

[4] MA. Riyadi, et al. *Vertical Double Gate MOSFET For Nanoscale Device With Fully Depleted Feature.* AIP Conference Proceedings. 2009;1136: 248-252.

[5] J. Pan. The Gate-Controlled Diode, High-Frequency, and Quasi-Static C-V Techniques for Characterizing Advanced Vertical Trenched Power MOSFETs. *IEEE Transactions on Electron Devices.* 2009; 56: 1351-1354.

[6] M. Masahara, et al. Vertical Ultrathin-channel Multi-gate MOSFETs (MuGFETs): Technological Challenges and Future Developments. *IEEJ Transactions on Electrical and Electronic Engineering.* 2009; 4: 386-391.

[7] L. Tan, et al. The influence of junction depth on short channel effects in vertical sidewall MOSFETs. *Solid-State Electronics.* 2008; 52: 1002-1007.

[8] J. Moers. Turning the world vertical: MOSFETs with current flow perpendicular to the wafer surface. *Applied Physics A: Materials Science & Processing.* 2007; 87: 531-537.

[9] Y. Taur, et al. "A continuous, analytic drain-current model for DG MOSFETs. *IEEE Electron Device Letters.* 2004; 25: 107-109.

[10] Y. Taur. An analytical solution to a double-gate MOSFET with undoped body. *IEEE Electron Device Letters.* 2000; 21: 245-247.

[11] XP. Liang, Y. Taur. A 2-D analytical solution for SCEs in DG MOSFETs. *IEEE Transactions on Electron Devices.* 2004; 51: 1385-1391.

[12] J. He, et al. A continuous analytic channel potential solution to doped symmetric double-gate MOSFETs from the accumulation to the strong-inversion region. *Chinese Physics B,* 2011; 20.

[13] K. Chandrasekaran, et al. *Compact modeling of doped symmetric DG MOSFETs with regional approach.* in Workshop on Compact Modeling, NSTI-Nanotech, MA, USA. 2006: 792 - 795.

[14] D. Munteanu, et al. Compact model of the quantum short-channel threshold voltage in symmetric Double-Gate MOSFET. *Molecular Simulation.* 2005; 31: 831-837.

[15] S. Kolberg, TA. Fjeldly. 2D Modeling of nanoscale DG SOI MOSFETs in and near the subthreshold regime. *Journal of Computational Electronics,* 2006; 5: 217-222.

[16] B. Subrahmanyam, MJ. Kumar. Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects. *Physica E-Low-Dimensional Systems & Nanostructures.* 2009; 41: 671-676.

[17] XJ. Zhang, et al. Analytical analysis of surface potential for grooved-gate MOSFET. *Chinese Physics.* 2006; 15: 631-635.

[18] MA. Riyadi, et al. *Study on the Analytical Model of non-planar MOSFET.* in Proceeding of the 2014 International Conference on Electrical Engineering Computer Science and Informatics (EECSI2014). Yogyakarta, Indonesia. 2014: 245-248.
[19] Z. Ghoggali, F. Djeffal. Analytical analysis of nanoscale fully depleted Double-Gate MOSFETs including the hot-carrier degradation effects. *International Journal of Electronics.* 2010; 97: 119-127.
[20] F. Djeffal, et al. Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges. *Microelectronics Reliability.* 2009; 49: 377-381.
[21] H. Lu, Y. Taur. An analytic potential model for symmetric and asymmetric DG MOSFETs. *IEEE Transactions on Electron Devices.* 2006; 53: 1161-1168.
[22] B. Yu, et al. Explicit Continuous Models for Double-Gate and Surrounding-Gate MOSFETs. *IEEE Transactions on Electron Devices.* 2007; 54: 2715-2722.
[23] V. Venkataraman, S. Nawal. Modeling and Simulation of Strained Silicon MOSFETs for Nanoscale Applications. *Bachelor of Technology dissertation.* Department of Electrical Engineering, Indian Institute of Technology Delhi, Delhi. 2006.
[24] KK. Young. Short-channel effect in fully depleted SOI MOSFETs. *IEEE Transactions on Electron Devices.* 1989; 36: 399-402.
[25] X. Zhang, et al. An Analytical Model for Threshold Voltage of Grooved-Gate MOSFET's [in Chinese]. *Chinese Journal of Semiconductors.* 2004; 4: 441-445.
[26] E. Kreyszig. *Advanced engineering mathematics*, 9th ed. Wiley. 2006.
[27] B. Doris, et al. *Extreme scaling with ultra-thin Si channel MOSFETs*. Electron Devices Meeting,2002 IEDM'02. Digest. International. 2002: 267-270.
[28] J. Tanaka, et al. *A sub-0.1mm grooved gate MOSFET with high immunity to short-channel effects.* in Electron Devices Meeting, 1993. IEDM '93. Technical Digest., International. 1993: 537-540.