

IMPROVED VOLTAGE OF CASCADED INVERTERS USING SINE QUANTIZATION PROGRESSION

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Abstrak

Metode-metode inverter multi level kaskoda (CMLI) yang ada hanya meningkatkan kualitas daya tetapi memiliki tegangan keluaran yang rendah, jika tegangan DC dibatasi oleh rating tegangan semikonduktor daya. Untuk meningkatkan amplituda tegangan keluaran CMLI, makalah ini mengusulkan pola urutan penyaklaran tegangan DC yang baru. Pola urutan tersebut didasarkan pada metode kuantisasi atau sine quantization method (SQM), yang penentuan urutan tegangan DC-nya diperoleh dari pen-diskret-an amplitudo fungsi gelombang sinus. Metode tersebut juga dikolaborasi dengan metode sisa luas sama (SERAM) untuk meminimalkan distorsi harmonisa total atau total harmonics distortions (THD). Suatu inverter kaskoda fase tunggal yang didalamnya berisi inverter sejumlah jembatan H disimulasikan dan diimplementasikan untuk memverifikasi metode yang diajukan. Amplitudo tegangan keluaran dan THD hasil simulasi dan eksperimen menunjukkan bahwa urutan pola kuantisasi sinus menghasilkan tegangan keluaran yang lebih tinggi bila dibanding dengan pola urutan DC lain, dengan kualitas daya atau THD berada pada batasan yang masih bisa diterima. Amplitudo tegangan keluaran memiliki fungsi yang linier dengan gradien 0,6665 untuk tiap kenaikan satu inverter jembatan H yang ditambahkan, dan memiliki penurunan THD dengan fungsi eksponensial dengan nilai yang kurang dari 5%.

Kata kunci: CMLI, inverter multilevel, SERAM, THD

Abstract

The previous methods of cascaded multilevel inverter (CMLI) can improve power quality but the methods have low voltage output if the DC voltages limited by the voltage rating of power semiconductor. To improve the amplitude of CMLI output voltage, this paper proposes a new DC voltage progression. The progression based on sine quantization method (SQM), which determines a sequence of DC voltages from discrete amplitudes of sine wave function. The method also collaborates with step equal residual area method (SERAM) to minimized total harmonics distortions (THD). A single-phase CMLI that consist four H-Bridges simulated and implemented to verify the methods. Amplitude output voltage and THD results of simulations and experiments indicate that the sine quantization progression produce the highest output voltage than other DC voltage progressions, with power quality or THD in the accepted region. The amplitude of output voltage have linier function with amplitude equal 0.6665 times of H-Bridges numbers and have exponential function of THD with value below 5%.

Keywords: CMLI, multilevel inverter, SERAM, THD

1. INTRODUCTION

Recently the multilevel inverter (MLI) is the most popular dc to ac converters for high voltage and high power in the power industry. The general structure of this MLI is to synthesize a sinusoidal voltage from several levels of voltages [1]-[4]. There are three well-known topologies; diode-clamps, flying capacitor, and cascaded multilevel inverter (CMLI) [4]-[8]. Diode clamp and flying capacitor are MLI with common dc sources. These inverters use capacitors in series to divide the dc bus voltage in to a set of voltage levels. While, the CMLI consists several H-bridge inverter units, and separated DC sources.

The CMLI topology eliminates the excessively large number of bulky transformers required by conventional multi pulse inverters, clamping diodes required by multilevel diode clamped inverters, and flying capacitors required by multilevel flying capacitor inverters [5]. A CMLI is simply consists a series connection of multiple H-bridge inverters [5]-[9]. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. The CMLI introduces the idea of using separate DC sources to produce a stepped voltage (similar to sine AC voltage waveform) by cascading the output voltage of H-bridges.

In the first developmeent, this inverter use equal DC voltage, but in order to improve power quality the unequal DC voltages also used [5], [9]. In the equal DC voltages, all of H-Bridge inverters have same voltage amplitude, but in unequal DC voltages each H-Bridge inverters have different voltages. The voltages depend on its function progression [9]. The popular unequal DC voltages CMLI are binary and trinary progressions of DC voltages. In the binary progression the amplitude of DC voltage have ratio $1: 2: 4: 8 \dots : 2^N$, while in the trinary progression the amplitude of DC voltage have ratio $1: 3: 9: 27 \dots : 3^N$.

The binary and trinary voltage progression can improve power quality but the methods have low voltage output if the DC voltages limited by the voltage rating of power semiconductor. To improve the CMLI within high amplitude output voltage this paper proposes a new DC voltage progression. The progression based on sine wave quantization. To improve the power quality usually this inverter collaborate within eliminate or minimize the THD [3-4],[9]. In this paper we use a new THD minimized based on area was called Step Equal Residual Area Method (SERAM). The computer-aided simulation using Matlab Simulink and experiments using a single phase CMLI prototype within computer controller based and PCI interfacing will be implement to verify the proposed scheme.

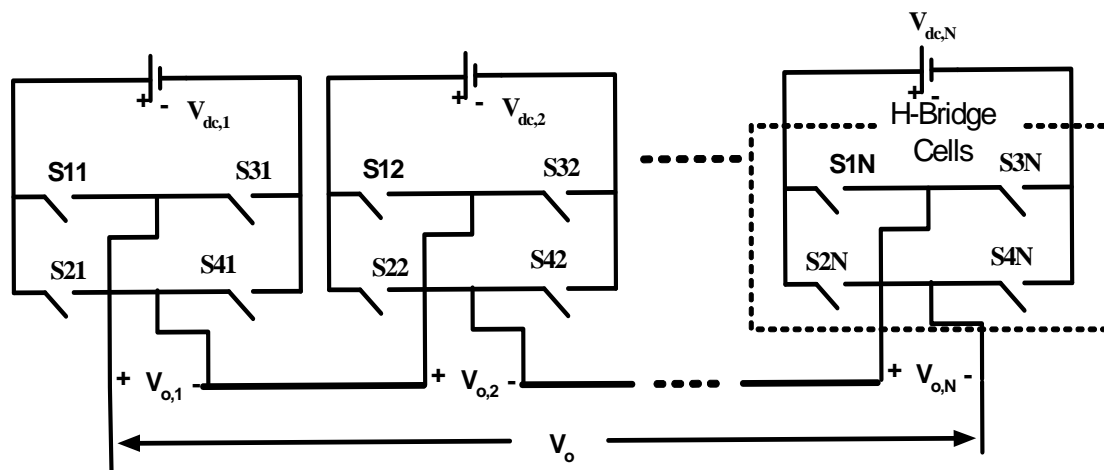


Figure 1. Single-phase cascaded multilevel inverter

Table 1. Switches combination and output voltage of each H-Bridge

Switches condition				Output
S_{1j}	S_{2j}	S_{3j}	S_{4j}	0
OFF	OFF	ON	ON	
ON	ON	OFF	OFF	V_{dcj}
ON	OFF	OFF	ON	
OFF	ON	ON	OFF	$-V_{dcj}$

Figure 1 shows a single-phase CMLI schematic that consist of several H-Bridges. If in each H-Bridge the switches are S_{1j} , S_{2j} , S_{3j} , S_{4j} , where j is sequence of H-Bridges, so there are four switching combinations in each H-Bridge, but only three possibilities of output voltage that occurred that is 0, V_{dcj} and $-V_{dcj}$ as shown in Table 1. The switching condition for 0 must be choice from two conditions occurred. So, Only three output voltages and three switches in

each H-Bridges. Figure1 also shows that if sequence of H-Bridges (j) until N, the voltage output of CMLI is obtained by summing of the output voltages of H-bridge as equation (1).

$$V_o(t) = V_{o,1}(t) + V_{o,2}(t) + \dots + V_{o,N}(t) \quad (1)$$

Based on equation (1) and three output voltages, the maximum number of switches of CMLI (s) is shown as equation (2). But not all of switches are the effective switching. The effective switches only produced if the output voltages have different amplitudes. These effective of output voltages usually called voltage levels (n).

$$s = 3^N \quad (2)$$

2. RESEARCH METHOD

Quantization is conversion of a continuous range of values into a number of discrete levels [10]. So, in the CMLI context, sine quantization progression is a sequence of DC voltages that amplitudes follow sine wave function value on discrete times. Figure2 shows sine quantization process. If the voltage of sine wave reference is V, the frequency is f and the number of H-Bridge is N, so each DC voltage can determine by equation (3). While, the output maximum voltage can be calculated by using equation (4).

$$\begin{aligned} V_{dc,j} &= V_m \sin(\omega t_j) \\ &= \sqrt{2}V \sin(2\pi f \frac{1}{4N} j) \\ &= \sqrt{2}V \sin(\pi j \frac{1}{2N}) \quad j=1,2,3,\dots,N \end{aligned} \quad (3)$$

$$V_{\max} = \sum_1^N \sqrt{2}V \sin(\pi j \frac{1}{2N}) \quad j=1,2,3,\dots,N \quad (4)$$

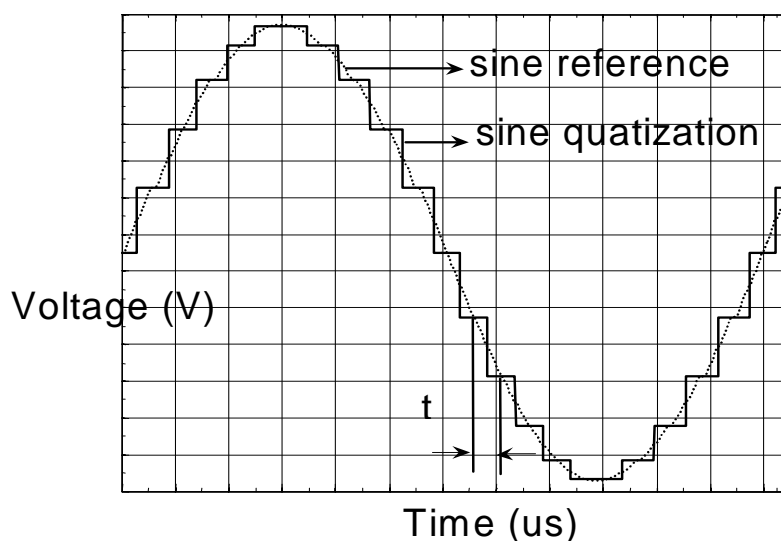


Figure2. Sine quantization process

Table 2 shows DC voltages of CMLI using sine quantization in the number of H-Bridges 2 to 5. The using of these voltages in to circuit of CMLI is shown in Figure1, the CMLI using sine quantization find.

To improve the power quality, usually the CMLI collaborate with eliminate or minimize the THD [3-4], [9]. One of these methods is area base method. In this paper we use Step Equal Residual Area Method (SERAM). The basic of the method within 7 levels output voltage of CMLI shown in Figure 3. Obviously, area in the upper and lower of sine reference is composed of harmonic components. Ideally, this area should be zero, i.e. the stepping wave and the sine wave overlap each other. In other words, the stepping wave has no harmonics but the fundamental.

Assume V_j and V_k are voltage amplitudes adjacent and the area between the sine wave and the stepping wave are equal, so the difference is zero. In the condition, the firing angle of power electronic devices can calculate using equation (5), while the other angles using equation (6).

$$d_i = \sin^{-1}\left(\frac{V_j + V_k}{2}\right) \quad (5)$$

$$d_j = \sin^{-1}(V_j) \quad \text{and} \quad d_k = \sin^{-1}(V_k) \quad (6)$$

A single-phase CMLI as describe above then simulated and implement to find amplitude, waveform and THD of output voltage. The simulation circuits using Matlab Simulink show at Figure 4, while photograph of experiment using a single-phase CMLI within four H-Bridges and variable DC is shown at Figure5. This CMLI using IGBT, optocoupler gate driver, PCI 1710 HG interfacing and computer controller based on Matlab Simulink.

Table 2. DC voltages of CMLI using sine quantization

H-Bridge Number	DC Voltage (pu)
2	0.71; 1
3	0.5; 0.87; 1
4	0.38; 0.71; 0.92; 1
5	0.31; 0.59; 0.81; 0.95; 1

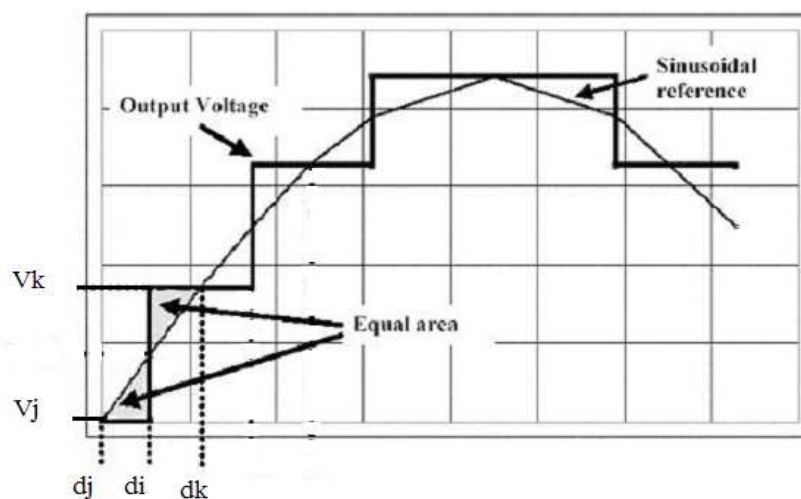


Figure 3. Total harmonic distortions minimization

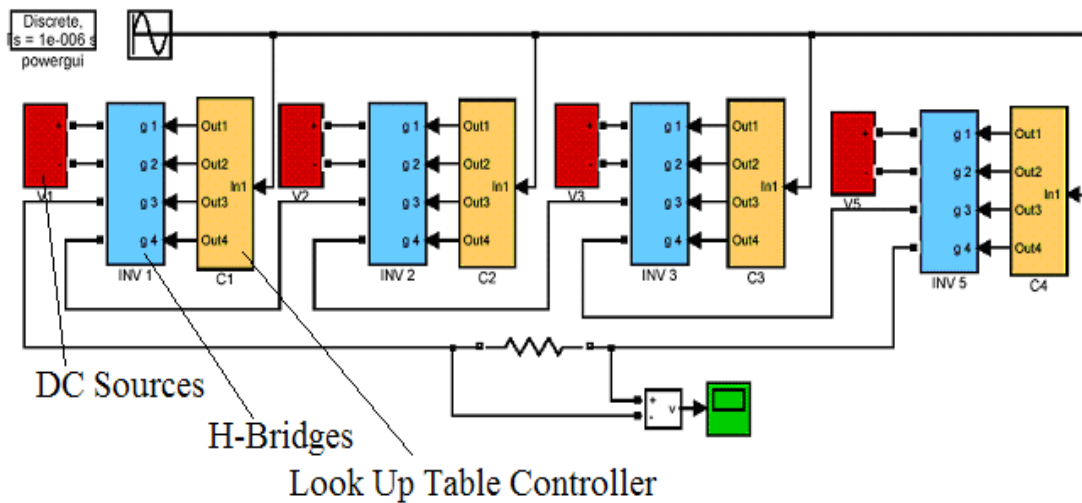


Figure4. Simulation circuit

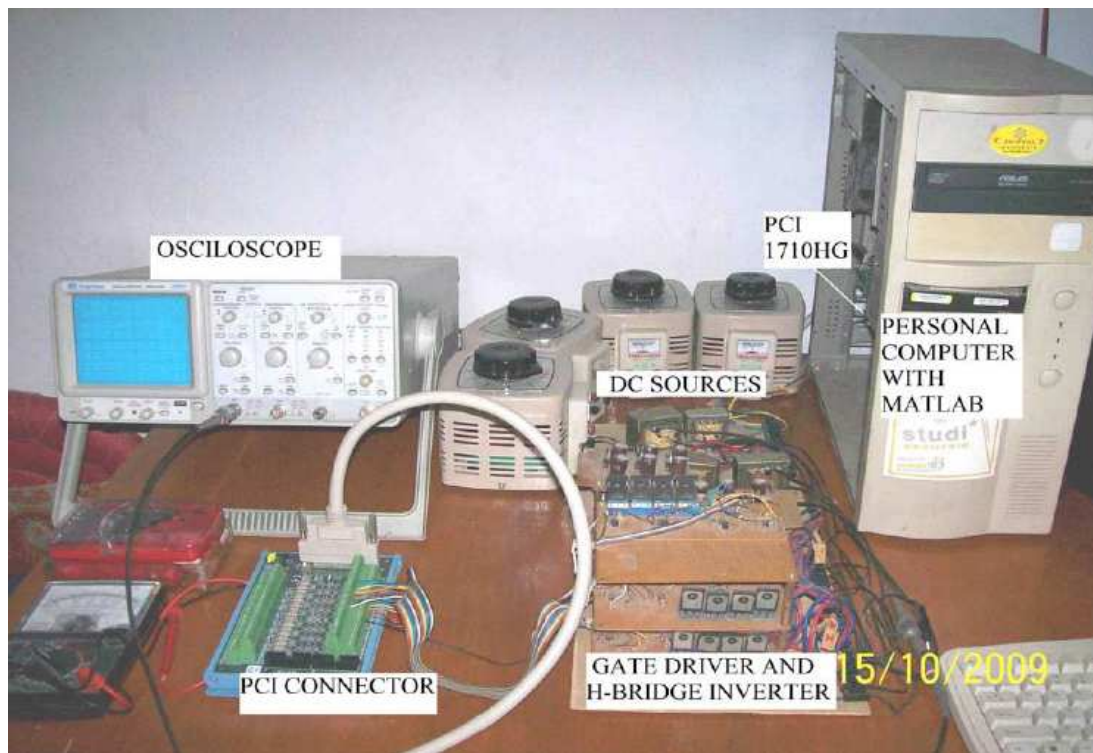


Figure5 Experiment set up.

3. RESULTS AND ANALYSIS

In the simulations and experiments, binary, trinary and sine quantization DC voltage progressions will be simulate and test. Figure 6 shows comparison of maximum output voltage of DC voltage used in CMLI. It shows that the propose DC voltage progression have the highest maximum output voltage than others. The amplitudes have linier function with slope 0.6665. This function appropriates equation (4). While binary and trinary progressions have non-linier function and limited on twice and 1.5 times of highest DC voltage.

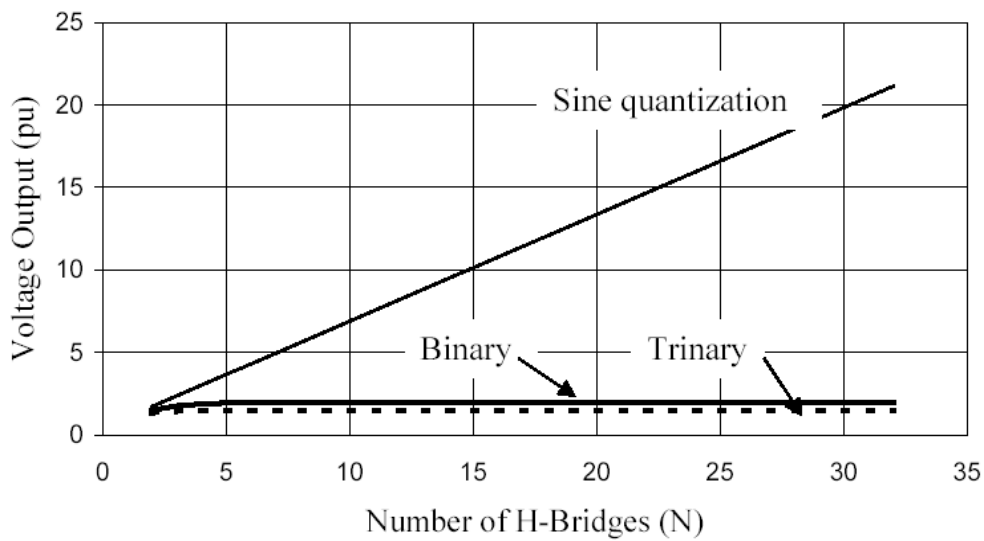


Figure 6 Output voltage of DC voltage.

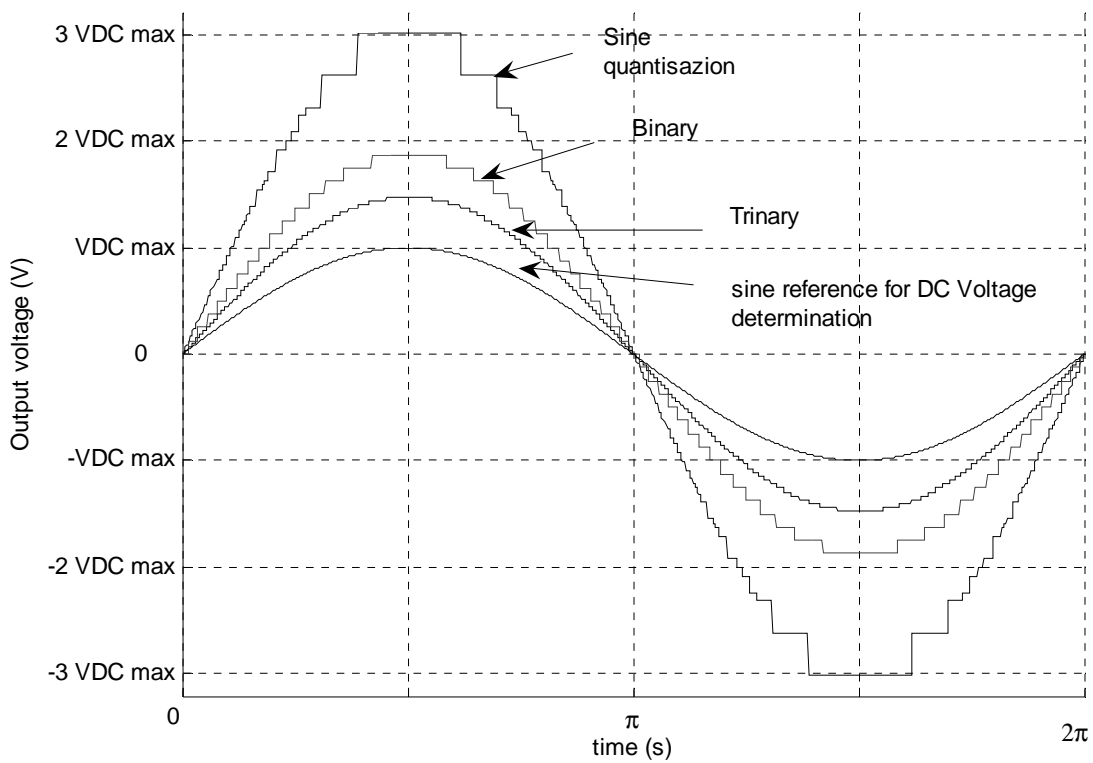


Figure 7 Output voltage waveform

The maximum output voltage and THD of simulations and experiments of some DC voltage progression are shown in Table 3. Similar to simulation result, experiment result also indicate that sine quantization progression of DC voltages have high output voltage and in the acceptance quality. Figure 8 shows a photograph of output voltage result by experiment of CMLI using sine quantization.

Table 3. Results of simulations and experiments

DC Voltage progression	H-Bridge Number	Levels number	DC Voltage (pu)	Max. output voltage (simulation)	Max. output voltage (experiment)	%THD (simulation)	%THD (experiment)
Binary	2	8	0.5; 1	1.5	1.42	12.22	18
	3	15	0.25; 0.5; 1	1.75	1.71	5.5	8
	4	31	0.125; 0.25; 0.5; 1	1.88	1.83	2.62	5
	5	63	0.06; 0.125; 0.25; 0.5; 1	1.94	1.89	1.29	3
Trinary	2	9	0.33; 1	1.33	1.31	9.37	12
	3	27	0.11; 0.33; 1	1.44	1.41	3.02	5.03
	4	81	0.03; 0.11; 0.33; 1	1.48	1.45	1	2.5
	5	243	0.01; 0.03; 0.11; 0.33; 1	1.49	1.46	0.35	1.4
Sinusoidal	2	9	0.71; 1	1.71	1.68	12.03	14
	3	21	0.5; 0.87; 1	2.37	2.35	5.93	9.2
	4	81	0.38; 0.71; 0.92; 1	3.01	2.97	3.13	4.7
	5	225	0.31; 0.59; 0.81; 0.95; 1	3.66	3.62	1.9	3.2

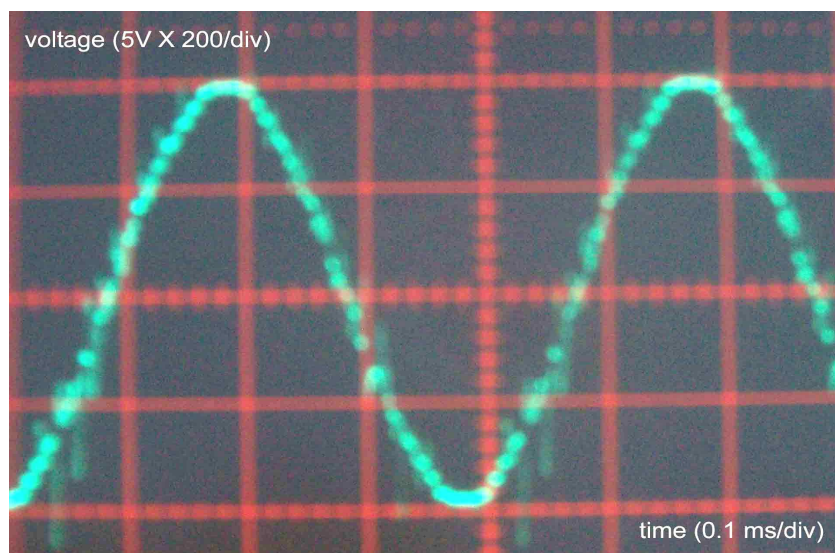


Figure 8 Photograph of output experiment

4. CONCLUSION

Sine quantization progression of DC voltages for CMLI has been proposed. Theory, simulation and experiment result show that the progression has higher output voltage than conventional progressions and has acceptance power quality. The invention can use to improve output voltage of CMLI in the amplitude and power quality using low voltage rating of power electronics, because this inverter have maximum output voltage in linier function of number of H-Bridges and have more decrease THD if number of H-Bridges increase.

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