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OFET Preparation by Lithography and Thin Film Depositions Process

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Abstract

The length of the channel OFET based thin film is determined during preparation takes place using the technique of lithography and mask during the metal deposition process. The lithography technique is the basic process steps in the manufacture of semiconductor devices. Lithography is the process of moving geometric shapes mask pattern to a thin film of material that is sensitive to light. The pattern of geometric shapes on a mask has specifications, as follows: long-distance source and drain channels varied, i.e. 100 µm, the width of the source and drain are made permanent. Bottom contact OFET structure has been created using a combination of lithography and thin film deposition processes.

Keywords: lithography, OFET, bottom contact, channel

1. Introduction

OFET (Organi field effect transistor) is a field effect transistor using an organic semiconductor material in the channel. An analytical model has been proposed by [1] for organic based thin film transistors. The main principle of the model is based on the channel length. OFET can be made either by using vacuum evaporation, by casting a polymer solution or a small molecule, or by a mechanical transfering of organic single crystal layer to the substrate. These devices have been developed for lower cost, broader electronic products, and environmentally friendly electronics. The performance of OFET continuously been improved to lead to the application in the field of industries. With a large potential as future electronic components, *e.g.* very cheap and can be a smart card candidate, the polymer can be processed by solvent method (solution process) that can be used to substitute the expensive silicon technology [2].

OFET based on copper phthalocyanine (CuPc) is a type of transistor in which the semiconductor material is an organic material or polymer. However, when it is compared to other types of inorganic transistors, OFET charge carrier mobility, in general, is still very low ranging between 10^{-5} - 10^{2} $cm^2V^{-1}s^{-1}$ [3]. OFET has been made with various forms of devices. The most common structure is the bottom gate with the drain and source electrodes above as shown in Figure 1. This structure is similar to the thin-film transistor (TFT) using a silicon thermal deposition of SiO_2 as the gate dielectric organic polymers. Such as polymethyl-methacrylate (PMMA), it can also be used as a dielectric [4].

In this reseach, the electrical and morphological configuration of OFET bottom contact (BC) using organic molecules is studied, *i.e.* phthalocyanines to form the active layer. Phthalocyanine is naturally stable at high temperature and suitable for thin film deposition by sublimation heat. On the other hand, CuPc is a semiconductor with high conductivity and can be used as an active ingredient for gas sensor devices [5]. This study suggests a single-stage LED of electrical circuits. This concept adopts a flyback converter operating in boundary conduction mode (BCM). Proposed circuit is simpler compact with minimum components involving in electrical circuits [6].

Based on research conducted by Triyana *et al.* [7], the CuPc material has LUMO (Lowest Unoccupied Molecular Orbital) energy is 3.5 eV, while the HOMO (Highest Occupied Molecular Orbital) energy is 5.2 eV. The results showed that the valuable gap energy is 1.7 eV

meaning that it almost becomes a potential candidate for organic semiconductor materials. The difference in the HOMO-LUMO orbital energy of 1.7 eV will conduct a reflection, that let electrons excitate. Thus the material sensitivity to other parts tends to be stronger. Therefore, CuPc semiconductor has a higher sensitivity to the other materials. Besides, the CuPc has special quality in the development of quantum computing that let electron exist in a quantum superposition state [8].

The purpose of this study was to provide additional information about the OFET device associated with the phthalocyanine material as a substitute for inorganic semiconductors. OFET material is an organic semiconductor, CuPc. OFET is a transistor that uses an organic semiconductor material, wherein the connection between the organic semiconducting metal is influenced by the effect of an electric field. The pioneer of OFET polythiophene films were produced at the end of 1970. This enables a fabrication of thin films organic molecules (order of micrometers) with a smaller distance. OFET has more benefit compared to the FET transistor of inorganic materials, *i.e.* environmentally friendly, easy fabrication, energy efficient operation and it can be operated at room temperature.

At this time, the thin film as a gas sensor application with more practical and high sensitivity is continuously developed, *e.g.* CuPc. This thin films is expected having optimum performance at room temperature as a gas sensor device. Gas detection is based on the oxidation-reduction events that occur between the surface of a thin film to the gas.

2. Design and Principle of Operation

OFET very similar to the inorganic field effect transistor (FET), especially concerning the design and functionality [9-11]. These devices consist of three electrodes, source (S), drain (D) and gate (G), the gate dielectric as a gate insulator of a semiconductor material and organic material that forms the active layer. Organic materials such as organic molecules [9-11] and polymer [12-14] can be used as the active layer.

OFET performance depends on the current settings and the electric field. OFET is called unipolar junction transistor (UJT) because of the way it works based on the flow of majority carriers. Current flows from D to S is controlled by a gate voltage (V_G). When no voltage V_G, the drain current (I_D) is very low, and the transistor is normal again. When V_G increases, the charge carriers accumulate on the surface of the semiconductor and the insulator. Then, when the current I_D increases, the charge carrier will be higher, and the transistor relapses on. This brief description is the working principle of OFET.
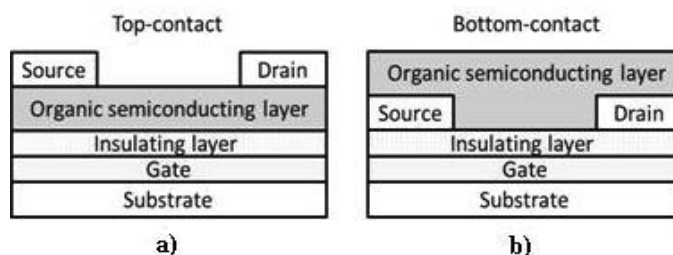

Figure 1. Schematic representations for an organic field effect transistor in a) top contact and b) bottom contact configurations

OFET based on Organic semiconductors (OSC) and operates via a reversible second electric field application [15]. Both side of the electric field is an electric field which occurs between S and D vertically, and between G and organic semiconductor. G electric field induces a charge carrier layer at the interface of the dielectric and the dielectric of the OSC (called channel). Two basic parameters of the device are channel length L (the distance between the contact electrodes S and D) and W (the channel width of organic layer). In Figure 1 shows the schematic OFET of top contact configuration as shown in Figure 1a and bottom contact as shown in Figure 1b. The difference between the two configurations lies in the position of the metal source and drain electrodes. The position of the metal source and drain electrodes over

the organic materials for OFET top contact, whereas of the organic material is bottom contact OFET. In this research, only OFET bottom-contact configuration was prepared and studied.

3. Method

This study uses an organic material, CuPc powder, as the active material in the OFET preparation. CuPc thin film was grown on the substrate Si/SiO_2 by using vacuum evaporation method. Thin film growth process using vacuum evaporation method includes several stages, *i.e.* evaporation and lithography.

Preparation of OFET-based thin film CuPc was done by growing contact bottom structure. First, the substrate Si/SiO_2 was cleaned with ethanol in the ultrasonic cleaner, then carried the electrode deposition source/drain on a layer of SiO_2 using a pure gold material with lithography method. Furthermore, CuPc deposed thin film.

Second, thin film growth technique as follows: cutting the substrate size (1.5 mm x 4.1 mm) and the distance between S to D is 100 µm, then the substrate was washed by using ultrasonic cleaner Parmer core models. CuPc material, 200 mg, was inserted into the bell-jar. Furthermore, the substrate that has been cleaned was mounted on the right holder on top of the boot which already contains CuPc. Then vacuuming until the pressure drops to 8×10^{-4} Pa (about 4 hours). The evaporation process was done by providing a steady current of 45 A until the time limit specified.

Third, mechanical lithography was done by: coating photoresist using a spinner, then process preheating (to increase the adhesion between the resist to the layer below, the alignment, and irradiation using a mask aligner), then lithography, and the last is aging (post-bake) to strengthen the resist. After lithography then the next step is etching. The purpose of etching to open the layer in places that are not covered by the resist. Resist that there should be discarded as useless and would contaminate the next process using a resist stripper.
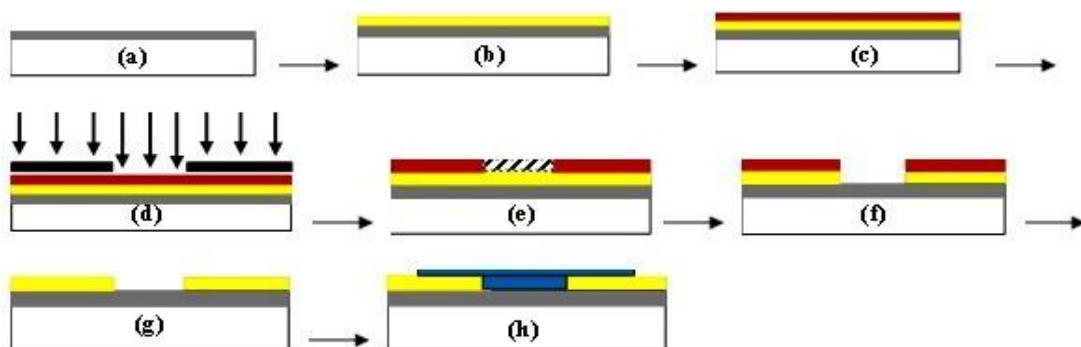

Figure 2. OFET fabrication lithography process: (a) The oxidation process on silicon wafers, (b) The coating process of gold (Au) by the method of vacuum evaporation at the top of the SiO_2 layer, (c) Positive AZ photoresist coating process with a spinner and apply technology: speed of 4000 rpm, 30 seconds, position the vacuum and heated in a clean oven for 15 minutes at a temperature of 85° C, (d) Expose to UV light for 60 seconds using a mask 1 (source and drain) Furthermore, developers with a solution timas arise until the source and drain mask pattern, then washed with DIH_2O to clean and reheated to a temperature of 120° for 30 minutes, (e) Part of the expose with UV light, (f) The process of etching of gold (Au) using $KJ + J_2 + DiH_2O$, (g) Remove positive resist AZ with acetone, (h) Thin film coating CuPc

Characterization of I-V metal contact/semiconductor showing the relationship between the current through the electronic device and the voltage applied to the terminal. Characteristics device are very important to determine the basic parameters of the devices and modeling the behavior in an electric circuit. Besides, the I-V characteristics of the active component are connected between the two electrodes utilized to estimate the material properties, such as conductivity and mobility. OFET based on organic semiconductors (OSC) and operates through

two reversible electric field application [15]. Both sides of the field is a field between the source/drain vertically and between the gate and semiconductor.

Gate field induces a charge carrier layer on the dielectric and the OSC dielectric interface, which is called a channel. The amount of channel capacitance depends on the dielectric and the gate field. Mobility in the OSC describes continuous transfer electrons to the material and collect in the channel induced by the electric field drain. I-V characterization of thin films based OFET CuPc is as follows. Electrodes from the S connected to a grounded, while the G and D each connected with a bias retreat. To determine the output characteristic graph of OFET, the need for robust measurement I_D from source to drain by varying V_D for each value of the gate voltage.

4. Result and Discussion

Lithography process of OFET fabrications based thin film of CuPc on a SiO_2 substrate to form an electrode source, drain and gate can be seen in Figure 2 and 3. The prepared OFET can be seen in Figure 4. The OFET is placed on the PCB using a gold wire and silver paste to facilitate experimentation.
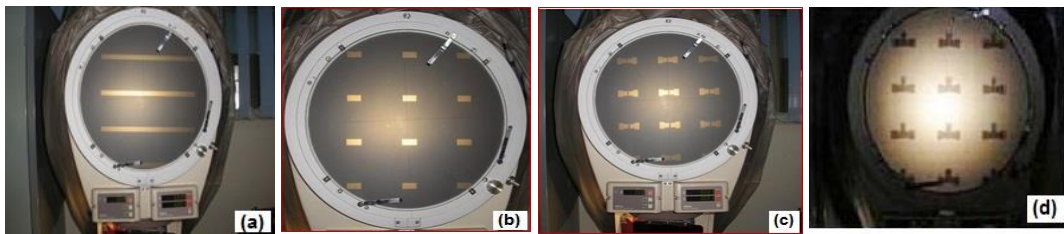

Figure 3. Gas sensor fabrication process: (a) The electrodes S and D has not been patterned, and the deposition of Au. (b) The electrodes S and D has not been done patterned and cutting each sample. (c) The electrodes S and D already patterned. (d) The electrodes S, D, and G already patterned
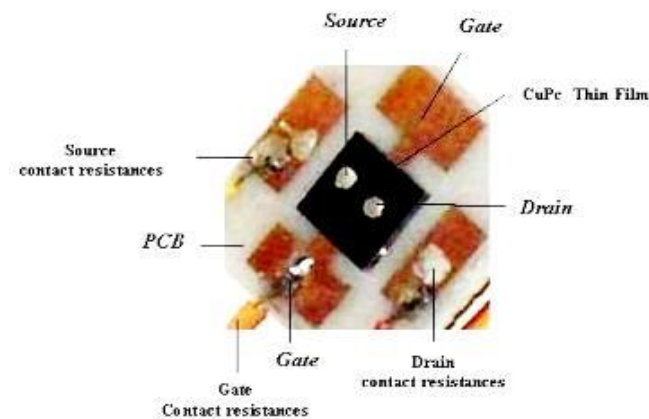

Figure 4. Results OFET fabrication on PCB

Characterization of I-V semiconductor contacts indicates the relationship between the current through the electronic device and the voltage at the terminals. Characteristics to determine the basic parameters of the device and modeling the behavior of the circuit [16]. Besides, the I-V characteristics of the active component connect two electrodes for predicting the properties of conductivity and mobility. OFET characterization the results as shown in Figure 5. The voltage V_G is varied, ie: -3 V; -1.5 V; 0 V; 1.5 V.
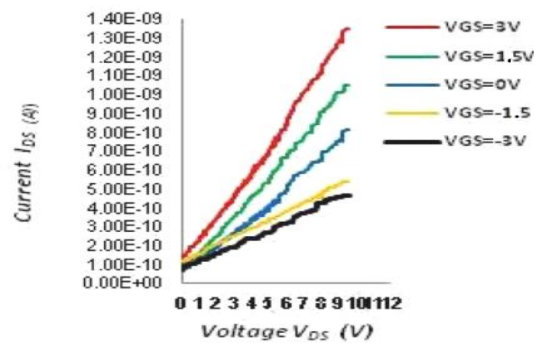
Figure 5. Characteristics OFET with channel length of 100 µm.

OFET characteristic curve in Figure 5 shows that the V_D increasing causes the I_D increasing and it will saturate, as described in Ohm's law. If V_D increased, depletion region will continue to rise until the conditions of a cut-off voltage (V_P). While the V_D at the V_P, it is called the cut-off failure. The maximum of OFET is achieved when $V_G = 0$ V and $V_D > | V_P |$. At the cut-off area, I_D has a fixed value though and V_D increases, so OFET can no longer respond. OFET as gas sensor device will detect gas only in the active region, where the changing in the I_D will change the V_D. On the characteristics of OFET with a channel length of 100 µm, an active region V_D is 1.2 V to 9.2 V and the I_D is 1×10^{-10} A until 1.28×10^{-9} A. While the OFET saturation region is at $V_D = 9.2$ V, and this is an area cut off.

In Figure 5 the I_{DS} plotted as a function of V_{DS} for a variety of different V_{GS} voltage applied to the electrodes, which serves as a gateway. Saturation region and the linear is agreed by the increasing voltage V_{DS}. At the time of the low-voltage V_{DS}, the current I_{DS} follow Ohm's law and is proportional to the V_{DS}. Therefore, the V_{DS} increases, the voltage that is measured relative to the source. This occurs during the changing of voltage channels from 0 to V_{DS}. Thus the voltage between the gate and points along the channel decreases from V_{GS} at the source V_{DS} - V_{GS} at the end of the drain.

While the channel is no longer uniform since the end of the source and drain ends have different effects. The influence of the most dominant channel increases the resistance becomes larger with the increasing of V_D. Thus the output characteristic curve (I_{DS} - V_{DS}) are not continuous as a straight line, but a non-linear curve, in this state is known as the pinch-off of the conductive channel transistor. It can be said that the observation of the situation is due to the saturation of I_{DS} pinch-off of the channel [17].

Figure 5 shows that the drain current is effectively influenced by the gate voltage. OFET I_{DS} increased by a negative gate voltage. These data indicate that the field effect device with the operation of the *p*-type accumulation mode. The characteristics of a transistor are their linear region and the saturation of the curve V_{DS} to I_{DS}. Based on Figure 5, the results did not reveal any current in a saturation state. This can be caused by the threshold voltage (V_T) OFET that is too large or unable to reach the drain and gate voltages what will make the conduction path between the drain and source. While the tendency linear region is almost similar to the current characteristics of the diodes. This can be caused by a considerable difference between the work function of the drain and source electrode-work function CuPc. Work function difference is large enough leading to the connection between electrode and CuPc non-ohmic contact or forming the junction between electrode and C_UP_C.

Like the transistor, FET sensor has three electrodes, where the active layer will interact with the others that can change the electrical properties of this layer. In the active layer, the material used is a *p*-type or *n*-type semiconductor. While the electrode G can be mounted on a semiconductor or directly on the dielectric layer. Because this gate electrode only takes the role of the electric field in the active layer, the voltage applied to the electrodes G will affect the current D-S. The more negative gate voltage is given, the greater D-S current flowing. G is given negative voltage as charge carriers in the active layer, polaron (hole). Polaron in the active layer will be attracted by the negative G-voltage side to the active layer adjacent to the dielectric layer. Then polaron will flow from the electrodes D or current D-S. If the gate voltage is fixed and the voltage of the D-S increased continuously, then the I_{DS} of the FET sensor will at

saturation region until breakdown conditions. Breakdown condition occurrs when the voltage V_{DS} is enlarged to V_{GS} until the leak.

Efforts to improve the characteristics of OFET is to use a hole transport process and utilizing semiconductor devices with a constant channel width and the channel length is varied between 100 µm to 300 µm. The channel OFET length affects the semiconductor hole transport. Here, the channel length increases the work function of the semiconductor. It can be concluded that the increased mobility of the charge carriers is caused by the shortening of the channel length.

At the time of OFET channel length is reduced, the device showed similar behavior with a long observation channel MOSFET, despite of the fact that charge transport and the operation of different devices regarding to organic structure. Study the effects of long-channel OFET shows the ratio of channel length to the thickness of the gate insulator and the electric field used for the prediction of induction conditions. Some cases, the number of channel length ratio with the thickness of the gate insulator does not show an accurate indicator, and it is advisable to do research to determine the effects of the events of the physical length of the channel.

5. Conclusions

The OFET was successfully prepared on a SiO_2 substrate with a length of 100 µm by using lithography technique and thin film deposition. The results showed that the I-V drain-source current was influenced by changing in gate voltage. The greater V_{GS} increased the I_{DS}. The characterization indicated that the active region of the channel length 100 µm was 1×10^{-10} A $- 1.28 \times 10^{-9}$ A. While the OFET saturation region was at V_D greater than 9.2 V, and this was cut off area.

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