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IEEE 802.11n Physical Layer Implementation on Field Programmable Gate Array

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Abstrak

Perancangan pada register transfer level (RTL) merupakan suatu tahapan yang membutuhkan ketekunan dan ketelitian yang besar dalam jangka waktu yang panjang untuk menghasilkan level abstraksi dari sebuah sistem rangkaian digital. Penelitian ini menyajikan dan membuktikan bahwa proses desain berbasis-model (MBDP) adalah sebuah metode yang efisien dan efektif untuk membangun sebuah sistem RTL yang kompleks seperti pada komunikasi nirkabel. Dengan menggunakan alur MBDP ini, diterjemahkan, dirancang, diuji lapisan fisik RTL dari sebuah standar yang disahkan pada akhir tahun 2009, yaitu IEEE 802.11n wireless local area network (WLAN). Hasil dari penelitian ini adalah sebuah prototype FPGA StratixII EP2S180 yang bekerja sebagai sebuah sistem 2x2 MIMO WLAN dengan throughput maksimum 144 Mbps.

***Kata kunci**: IEEE 802.11n, lapisan fisik, Model Based Design, RTL, FPGA*

Abstract

Register transfer level (RTL) development is a time cost step that requires high diligence and fidelity to get the valid interpretation of abstraction function of digital circuit. In this research, we introduce and prove that Model-Based Design Process (MBDP) is an effective and efficient way to develop a RTL complex system such as wireless communication. Using MBDP flow, we interpret, develop, and verify the physical layer RTL of a new standard that ratified on the end 2009, i.e. IEEE 802.11n wireless local area network (WLAN). The result of this research is a prototyping FPGA StratixII EP2S180 that has properly worked as a 2x2 MIMO WLAN with maximum throughput 144 Mbps.

***Keywords**: IEEE 802.11n, Physical Layer, Model Based Design, RTL, FPGA*

1. Introduction

Recently, local area network (LAN) are required for many applications widely at home, office etc. In order to meet efficiency, a power line utilization method has been introduced as alternatives of local communication [1]. However, wireless scheme is still the most convenient and popular implementation of LAN. The WLAN standard high-speed and high-reliability, IEEE802.11n [2], which enhanced with the previous standards IEEE802.11a/b/g, can achieve maximum throughput more than 100 Mbps in both Medium Access Control (MAC) and physical (PHY) layers [3]. This standard specifies implementation of new technologies such as Multiple-Input Multiple-Output (MIMO) – Orthogonal Frequency Division Multiplexing (OFDM) [4].

Register Transfer Level (RTL) design flow has important role in order to bring the next generation WLAN concept to the real world. VHDL may be used to model and simulate aspects of the complete system containing one or more devices. This may be a fully functional description of the system allowing the FPGA/ASIC specification to be validated prior to commencing detailed design. However, VHDL is a complex and sophisticated language that learning all of its features is a daunting task [5].

Model-based design process (MBDP) is selected as design flow for acceleration and simplification of developing process [6]. In Model-Based Design, a system model is the center of the development process, from requirements up to testing. After model development, simulation shows whether the model works correctly. In this project, Sinplify DSP, one of Matlab toolbox, is

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employed as the Computer Aided Design (CAD) tool of MBDP. Furthermore, we implement the model on prototyping FPGA board which has six FPGAs chips with mesh connections.

In this paper, some parts of Register Transfer Level (RTL)-Intelligent Properties (IPs) such as frame synchronizer, carrier frequency synchronizer, MIMO decoder, and Fast Fourier Transformer (FFT) have been early developed [7]. Then, physical layer (PHY) – baseband (BB) RTL model of IEEE802.11n WLAN system are developed by employing those IPs, and evaluated on Field Programable Gate Array (FPGA). The developed model accommodates the mandatory scheme that is compatible with the existing IEEE802.11a/g. The throughput can achieve 144 Mbps for 20MHz bandwidth with two antennas.

2. The Proposed Method

Figure 1 shows the concept of RTL design flow that consists of some steps. First, we design the architecture for each block on high level language such as m-file MATLAB. Then, we can execute floating point simulation and fixed point simulation on these models. Breakdown to Hardware Description Language (HDL) is the next step that followed by its verification. The next step is logic synthesis that breakdown the design to the logic level. For FPGA verification, we need Quartus or Xilinx ISE for placement and routing. However, for application-specific integrated circuit (ASIC) application, user needs ASIC CAD tools such as Synopsys CAD tool for routing process into ASIC.

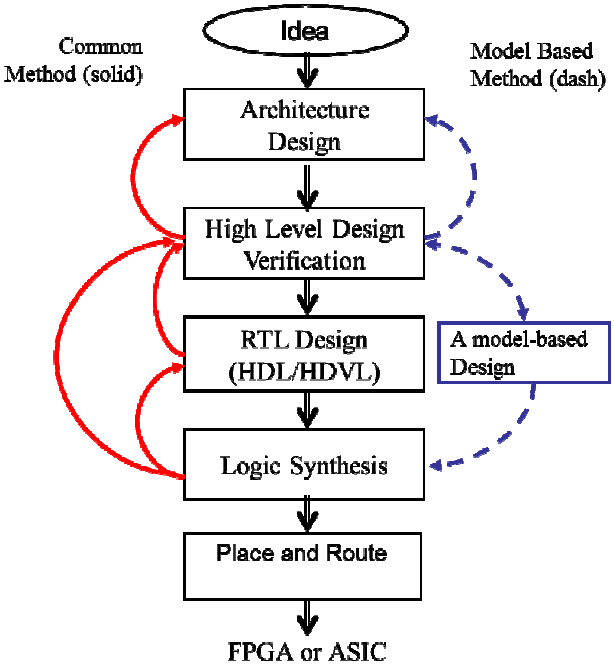


Figure 1. A RTL design flow

In common application of RTL design flow for FPGA implementation, such as in [8,9], some mistakes could appear on each step that makes a correction process in each step. However, in MBDP, correction paths exist on high level verification and HDL design only. Thus, human mistakes can be decreased as well as increasing system design efficiency.

A Synplify DSP [10] is an MBDP CADtool that used in this project to produce RTL code as an outcome of RTL design process. This tool offers easy RTL design and simulation with many Intellectual Properties (IP). Moreover, user can automatically generate code for embedded deployment and create test benches for system verification that means saving time and avoiding the coded errors.

Generally, there are mainly four advantages of this RTL design tool [6,10]. First, we can work seamlessly from architecture system design to hardware description language (HDL) level.

Second, it is easy to use by mid-class designer because special grammars are not used and many IPs are already prepared such for filtering, controlling, signal operating, and memory. Third, just uniting the block-models and RTL simulations is possible. Finally, test bench and HDL are created automatically by this tool. These advantages minimize human's mistakes so that an efficient system verification and improvement can be achieved.

Figure 2 shows the snap shoot of RTL design user interface using Synplify DSP and its simulation result. Due to the complexity of RTL design, here we only show a sub-part of GI inserter at the transmitter side.

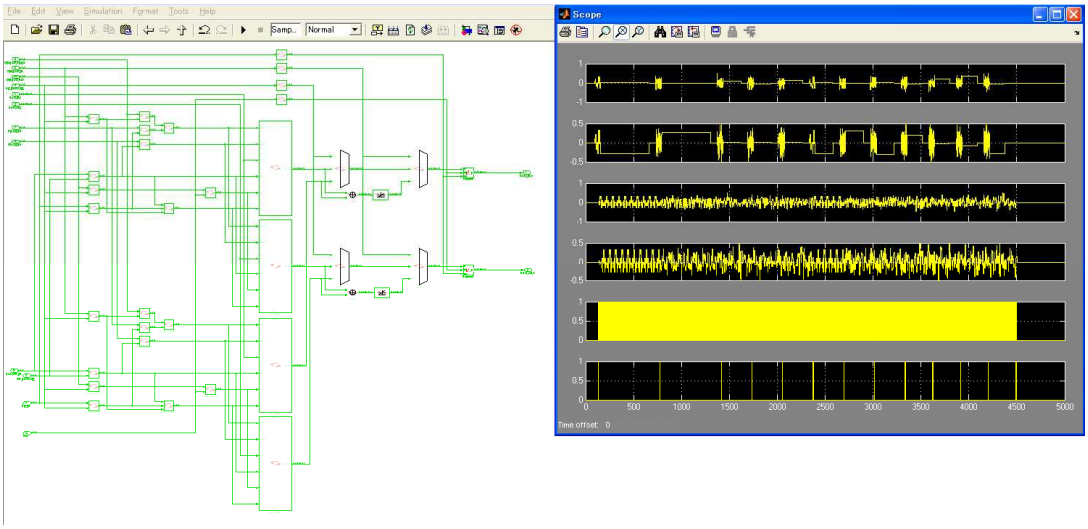


Figure 2. Snap shot of MBDP user interface

3. Research Method

3.1. Specification

802.11n PHY layer is based on MIMO OFDM technology, which allows the transmission of up to 100 Mbps over wider range of bandwidth than earlier versions. MIMO uses multiple transmitter and receiver antennas to allow higher throughput through spatial multiplexing, and increase its coverage. This standard provides three packet mode; legacy, mixed and greenfield. Legacy format provides compatibility with the previous standards such as 802.11a/g. Mixed and Greenfield format are used for high throughput. The specification of our system are 2x2 MIMO OFDM with legacy and mixed packet formats as shown in Table 1. This specifications are mandated by 802.11n standard except for the guard interval (GI) that uses short GI (400 ns) rather than long GI (800 ns).

Table 1. Design Model Specifications

Parameter	Specification
Packet Model	Legacy and mixed packet mode
Number of TX antenna	2
Number of RX antenna	2
Modulation and coding scheme	Index 0 - 15
Number of used subcarrier	52 (legacy) or 56 (mixed)
Bandwidth	20 MHz
Data rate	Up to 144 Mbps
FEC Encoder	Binary Convolutional Code (BCC)
Guard Interval (GI)	Normal GI and Short GI
System Clock	80 MHz
Carrier Frequency	5 GHz

Regarding the packet mode, Figure 3 shows the frame format of legacy and mixed packet modes. Both of them consist of Non-HT Short Training Field (L-STF), Non-HT Long

Training Field (L-LTF) and Non-HT Signal Field (LSIG), then followed by data field for legacy mode, and HT signal field (HT-SIG) and other preambles (HT-STF and HT-LTF) for mixed mode. The frame format is very important to recognize packet mode that the system used in communication as well as to optimize the designs.

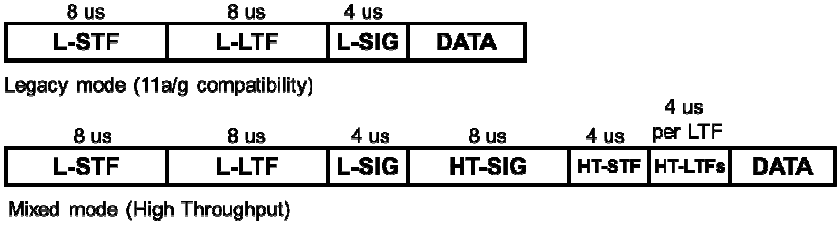


Figure 3. Frame format of legacy and mixed modes

3.2. Transmitter Model

The general transmitter block diagram is mentioned in 802.11n standard [2]. Some modifications is made to fulfil 2x2 MIMO-OFDM with specifications mentioned above. Since maximum stream is two, we reduce even remove some of parts. Interleaver, mapper, IDFT, Guard Interval (GI) inserter and TX Filter are decided to be two instead of four and eliminate encoder deparser because of one Forward Error Correction (FEC) encoder. We also removed STBC to keep 2x2 MIMO using two antennas. Moreover, we replace IDFT with IFFT to reduce computational complexity.

Figure 4 shows our transmitter model that consists of a scrambler, a FEC encoder, a spatial stream parser, two interleavers, two mappers, two cyclic shifters, a block of preamble and pilot memory, a spatial mapper, two IFFTs, two GI inserters, two windowings, two TX filters and two antennas.

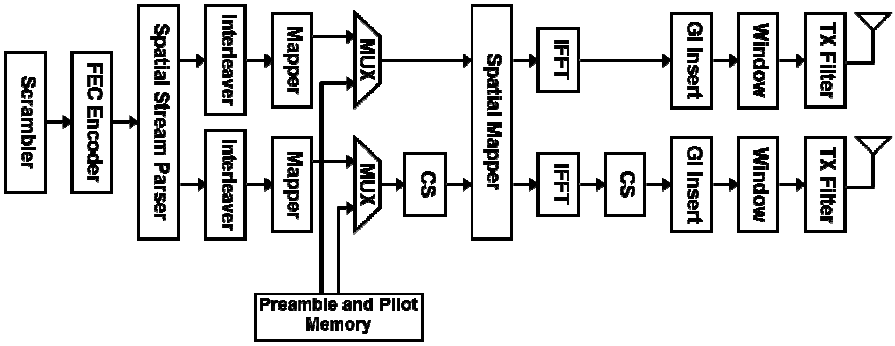


Figure 4. Transmitter diagram

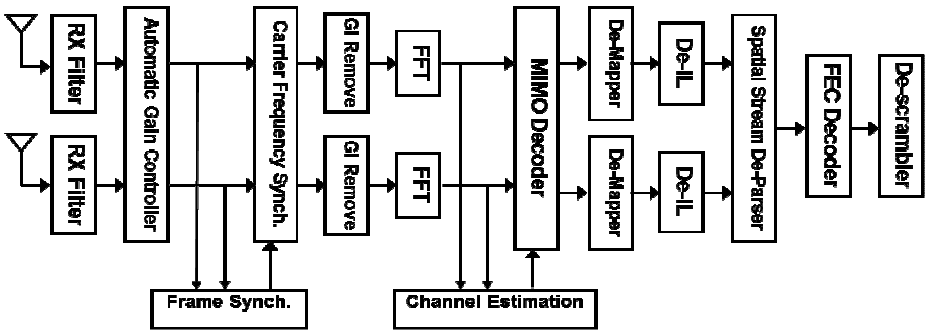


Figure 5. Receiver diagram

3.3. Receiver Model

IEEE 802.11n standard does not mention receiver block diagram. Thus, it becomes vary and depend on the designer. Based on observation on transmitter principles and frame format that sent by transmitter, we design the receiver model as shown in Figure 5. This model consists of two RX filters, an Automatic Gain Controller (AGC), a frame synchronization, a carrier frame synchronization, two GI removers, two FFTs, a channel estimation, an MIMO decoder, two demappers, two deinterleavers, a spatial stream deparser, an FEC decoder, and a descrambler.

Some blocks in receiver actually have the same concept with the transmitter such as GI inserter with GI remover, interleaver with deinterleaver, and scrambler with descrambler. Hence, there is possibility for sharing between transmitter and receiver block that will reduce resource in the implementation.

4. Result and Discussion

The IPs development and its simulations have been done on previous work [7]. In this paper, we focus on simulations, design results, and FPGA implementations of overall system. Simulations have been executed using fixed point simulation in Sinplify DSP design tools. Since we have done fixed point simulation in MBDP, we can ignore HDL simulation in the next step. However, we can consider HDL simulation which the test bench is automatically generated using Sinplify DSP.

The system consists of two main parts, i.e. transmitter and receiver that connected using a certain channel. Additive white Gaussian noise (AWGN) is considered as the channel model for fixed point simulation. We apply the highest throughput for our verifications, so that some parameters must be set for the appropriate setting. Packet format is mixed mode as shown in lower part of Figure 3. MCS index is set to the highest one, i.e. 15. However, short GI format should be considered to reach the highest throughput. Figure 6 shows a transmitted packet on antenna 1 and 2 respectively with four OFDM data packet. This signals satisfy the frame format given in Figure 3.

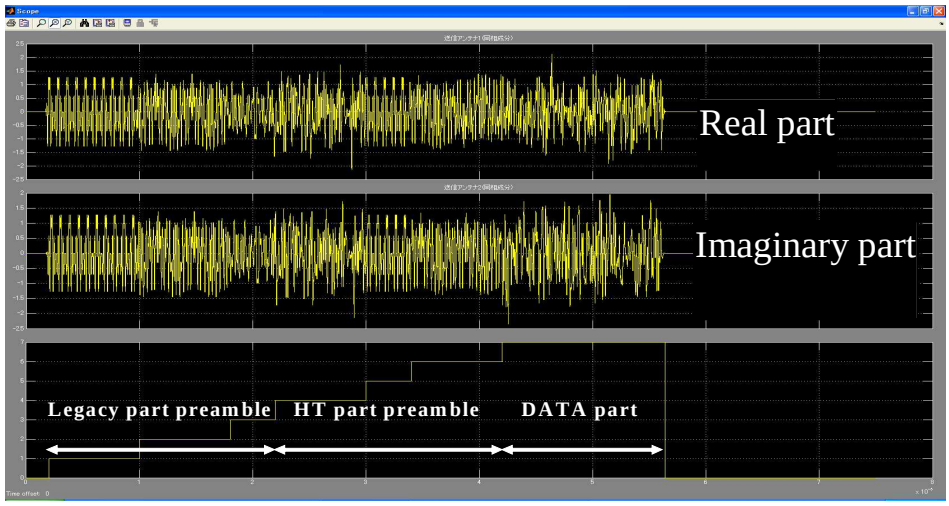


Figure 6. RTL simulation result

After verification using fixed point simulation, and reinforced with HDL simulation, there are the next two step options. First is FPGA implementation and second is ASIC implementation. In this project we choose FPGA as the target device for the hardware simulation. Considering FPGA with high resources, good performances, and reasonable price, StratixII EP2S180 (Altera, corp.) has been chosen as the target device.

Logic synthesis is required before FPGA implementation. Synplify Pro is one of Synplify design tools that used to execute HDL level design to logic level design on FPGA hardware. Table 2 shows the information regarding logic synthesis result. This result indicates the

computation resource requirement to implement the design into the target device such as number of Adaptive Logic Module (ALM), operable clock frequency, total RAM bits and number of Digital Signal Processing (DSP) block. Generally, receiver requirement especially in term of ALM and DSP block are higher than transmitter. It comes true since decoding schemes have higher computation than the encoding. Moreover, some additional components such as synchronization and channel estimation blocks are needed in receiver side. However, transmitter and receiver need same memory capabilities because the memories are used only for preambles and pilots storage that have to be known by transmitter and receiver.

Table 2. FPGA Synthesis Results

Target FPGA	Device name	Stratix II EP2S180
	Total ALMs	28,884
	Total RAM bits	34,368
	DSP blocks	687 blocks
Transmitter	Target operating frequency	80 MHz
	Maximum operating frequency	116 MHz
	Total Used ALMs	6,433
	Total Used DSP locks	234 blocks
	Total Used RAM bits	17,184 bits
Receiver	Target operating frequency	80 MHz
	Maximum operating frequency	102 MHz
	Total Used ALMs	22,451
	Total Used DSP locks	453 block
	Total Used RAM bits	17,184 bits

FPGA as hardware verification is better comparing with ASIC in term of time cost and flexibilities. The target device is FPGA StratixII EP2S180 (Altera, corp.) which has about 71,760 adaptive logic modules (ALMs) that equal to 2,200,000 gates [11]. 9,383,040 RAM bits and 1536 DSP blocks are also available in this device [11].

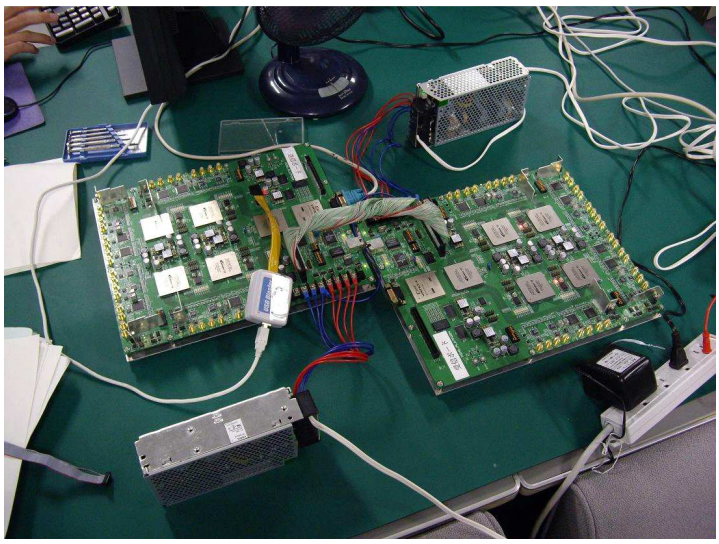
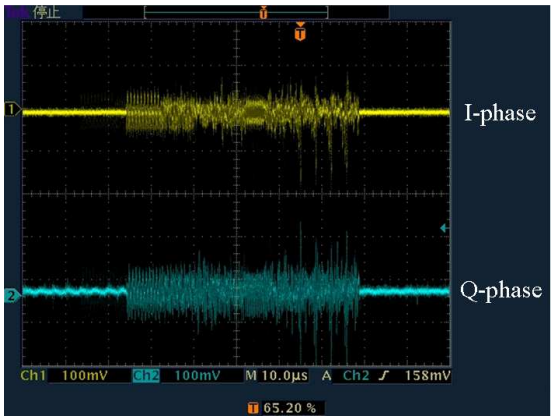


Figure 7. Prototyping the evaluation board

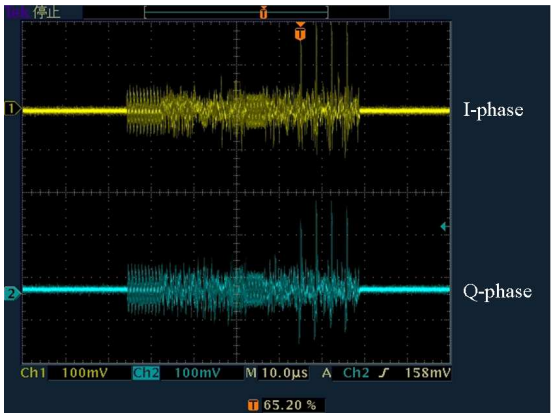
In order to implement MIMO scheme, some FPGAs are built on a board as shown in Figure 7. This prototyping board actually has six FPGA chips with mesh connections, but we only use two of them as two streams of physical layer.

Placement and routing are required before downloading the logic level design (after logic synthesis) result to FPGA. In this process, Synplify Pro is employed rather than Quartus in order to keep in line process that using Synplify DSP in the previous steps. Moreover, some modifications are required if we use Quartus in this step.

Verifications are done using test bench that generated in the previous step. Since the output of baseband signal around 80 MHz (equal to the utilized clock), high frequency oscilloscope is required to monitor the signal. Figure 8 shows the output waveform from FPGA in transmitter side for both antennas that captured by the oscilloscope. These waveform are similar with the simulation result in Figure 6 that consist of four OFDM data packet. Therefore, the board level verification for 802.11n baseband is successfully done.



Antenna 1 waveform



Antenna 2 waveform

Figure 8. The waveform captured by the oscilloscope

5. Conclusions

MBDP has been successfully implemented for RTL designs of IEEE802.11n WLAN baseband physical layer system. MBDP is proven as one of RTL design flows that provides acceleration and simplification of developing process. The developed system with target throughput up to 144 Mbps can be realized with two antennas on 20MHz bandwidth. Moreover, the design has been successfully implemented into evaluation board with 28,884 ALM, 34,368 bit memory, and 687 DSP block. Based on hardware verification, the developed system has worked properly, and met the specification given by the standard. As the future works, we will optimize the design and develop the higher specification that can reach 600 Mbps data throughput as mentioned in the standard for 4x4 scheme.

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