TELKOMNIKA, Vol.16, No.3, June 2018, pp. 1083~1091
ISSN: 1693-6930, accredited **A** by DIKTI, Decree No: 58/DIKTI/Kep/2013
DOI:10.12928/TELKOMNIKA.v16i3.7630

A New CMOS Fully Differential Low Noise Amplifier for Wideband Applications

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Abstract

In this paper, a multi-stage fully differential low noise amplifier (LNA) has been presented for wideband applications. A common-gate input stage is used to improve the input impedance matching and linearity. A common-source stage is also used as the second stage to enhance gain and reduce noise. A shunt-shunt feedback is employed to extend bandwidth and enhance linearity. The proposed low noise amplifier has been designed and simulated using RF-TSMC 0.18 µm CMOS process technology. In frequency band of 3.5-7.5 GHz, this amplifier has a flat power gain (S_{21}) of 16.5 ± 1.5 dB, low noise figure (NF) of 3dB, input (S_{11}) and output (S_{22}) return losses less than -10 dB and high linearity with input third-order intercept point (IIP_3) of -3dBm. It's power consumption is also less than 10 mw with low power supply voltage of 0.8v.

Keywords*: low noise amplifier, fully differential, noise figure, feedback*

1. Introduction

Ultra-wideband (UWB) technology has become very popular in recent years due to high demand for wireless high-speed communications. The frequency range of UWB was approved from 3.1-10.6 GHz by Federal Communication Committee (FCC) and has commercially been used since 2002 [1-2]. Low noise amplifier (LNA) has an important role in receiver as the first active block in the receiving chain. In LNA design, achieve to parameters such as low noise figure (NF), high gain and low input return loss are important respectively to reduce effect of noise from subsequent stages (especially down-conversion mixer) and provide sufficient input matching [3-4]. Since second-order harmonic distortion greatly affect the efficiency of direct conversion receivers, those are examined as an important parameter in LNAs. So far, many prototypes have been proposed to achieve convenient features of LNA [5-10]. In resistive feedback method, it is difficult to simultaneously achieve appropriate gain and noise figure despite achieving appropriate input and stability [5-6]. Although distributed amplifiers provide high gain, wide bandwidth and proper input matching, they have a high power consumption and are not suitable for low-power applications [7].

Cascode topology is proposed with current reuse technique to reduce power consumption, but there is the need for high level power supply voltage for proper biasing of its transistors [8-9]. A common-gate (CG) topology has been widely used for a wideband LNA because it features wideband impedance matching, superior reverse isolation, stability, and a high linearity compared to a common-source (CS) topology. Although common-gate LNAs feature desirable properties for wideband operation, their high NF under the input-matching condition prevents its extensive use. Additionally, the 3-dB gain bandwidth of CG LNA is rather finite. Using fully differential CG-LNAs is a suitable method to cancel second-order distortion as well as increasing linearity. However, parasitic capacitances increases in these amplifiers due to the large number of transistors which leads to poor performance of LNA in wide bandwidth [10]. In this paper, a multi-stage fully differential LNA with negative feedback is proposed to alleviate some common issues and improve the performance of conventional CG-LNAs. The objective of the design is achieving power gain (S_{21}) higher than 15 dB, noise figure (NF) less than 3 dB, input and output return losses (S_{11} and S_{22}) less than -10 dB and input-output isolation (S_{12}) less than -30 dB in the frequency band of 5-9 GHz. In addition, the design tries to reduce power

Received October 20, 2017; Revised February 28, 2018; Accepted March 10, 2018

consumption and level of power supply voltage as much as possible. The paper is organized as follows. In Section 2, the proposed LNA is first introduced and a detailed analysis including input impedance, gain, and NF is then explained. Section 3 presents the circuit level simulation results. The results are discussed and compared with recently simulation reported UWB LNAs. Finally, section 4 concludes the paper with some key findings.

2. Proposed Low Noise Amplifier

The proposed LNA topology with negative feedback along with its simplified single-ended model, shown in Figure 1 and Figure 2 respectively. Common-gate (CG) input stage (M_1 and M_2) is used for matching of suitable input impedance, bandwidth improvement and high input-outputisolation. However, there is a trade-off between the input matching and noise performance. The noise figure of a conventional CG LNA is inversely proportional to transistor transconductance (g_m), and the input impedance is simplified as $1/g_m$. Therefore, the transistor transconductance, that defines the input matching condition, limits the LNA performance in terms of noise and gain. To overcome this problem, a common-source (CS) stage (M_3 and M_4) is cascaded to increase gain and reduce noise.

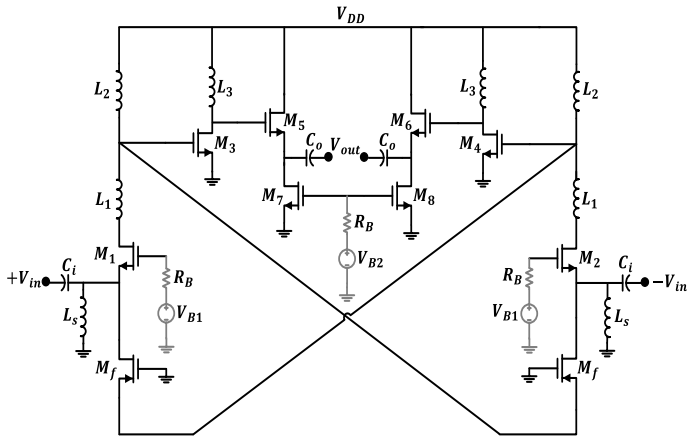

Figure 1. Proposed LNA structure

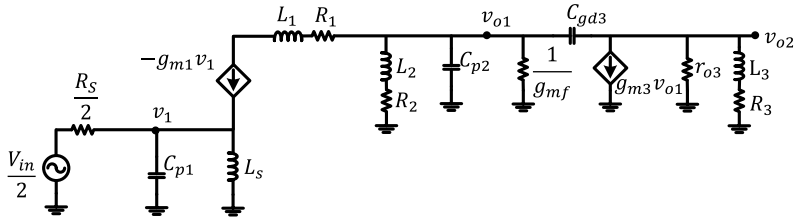

Figure 2. Small-signal equivalent circuit for single-ended model of proposed LNA

In addition, a negative feedback has been used to add a degree of freedom in determining the g_m of the input matching transistor. A gate of PMOS transistor (M_f) in CS topology is coupled to the output node to obtain a shunt-shunt feedback network. It will be shown below that using the feedback will eliminate the need for high g_{m1} for input matching which results in reduced power consumption. Moreover, using a PMOS transistor (M_f) in the feedback network eliminates an inductor used at the source of the CG input stage.

In proposed LNA, biasing of all transistors expect for M_7 and M_8, has been done through the power supply and ground. A proper constant current biasing circuit is used to generate the bias voltages of $V_B$which is not shown in Figure 1 for simplicity. The capacitors of C_i and C_o have been considered for DC bias isolation. The inductor of L_S have been designed as off-chip

inductor with quality factor (Q_s) of 70 and L_1, L_2 and L_3 are designed on-chip with Q_s=10 at center frequency of f_0=5.5 GHz. Output buffer stage is also used to achieve appropriate output matching.

2.1. Input impedance

A common-gate topology has been widely used for a wideband LNA because it features wideband impedance matching compared to a common-source topology. In conventional differential CG-LNA, the impedance matching is achieved by the size and bias current input transistors (M_1 and M_2) to ensure ($2/g_{m1}$=50 Ω). Therefore, larger g_{m1} should be chosen result in high drain current or large channel width (w_1). The design can lead to high power consumption and increasing parasitic capacitance of the input transistor.

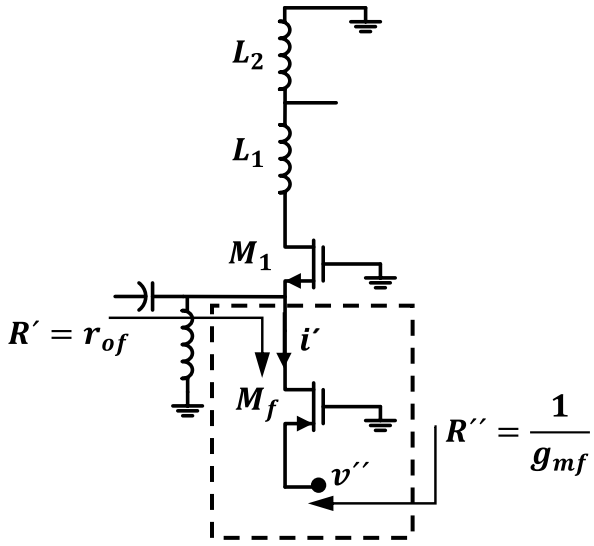

Figure 3. Transistor feedback network with feedback factor of $\beta=g_{mf}$

Hence, a shunt-shunt feedback network is employed to reduce the input resistance (R_{in}) as shown in Figure 3. The feedback theory is used to determine the LNA input impedance as follow:

$$R_{in} = (\frac{R_{in}}{2}) \| R_{if} \quad (1)$$

$$R_{in} = \frac{\frac{1}{g_{m1}}}{1+\beta R'_m} \| (\frac{R_s}{2}) \quad (2)$$

$$\beta = g_{mf} \quad (3)$$

$$R'_m = Z_x \quad (4)$$

where, β is feedback factor and Rs is source resistance. Z_1 and Z_x denote the load impedances at drain of M_1 and M_3 respectively as follow:

$$Z_x \approx (Z_1 \| \frac{1}{g_{mf}}) \quad (5)$$

where,

$$Z_1 = \left(((R_1 + JL_1\omega) \| (R_2 + JL_2\omega)) \| \frac{1}{JC_{p2}\omega} \right) \quad (6)$$

$$C_{p2}=C_{gsf}+C_{gs3}+C_{gd3}(g_{m3}r_{o3}) \quad (7)$$

R_{if} and R'_m are the input resistance and open loop transimpedance gain of the input stage with the loading effects of the feedback network, respectively. R_1 and R_2 are respectively series parasitic resistances of L_1 and L_2 at resonance. The LNA can be matched to the source resistance at the resonance frequency can be obtained by:

$$R_{in}=\frac{1}{g_{m1}(1+g_{mf}Z_x)} \quad (8)$$

According to (8), the feedback loop provides a degree of freedom so that impedance matching does not set transistor biasing current results in lower g_{m1} to achieve input matching. The input matching condition for proposed LNA is obtained by Miller approximation as follows:

$$Z_{in}\approx R_{in}\left\|\frac{1}{sC_{p1}}\right\|sL_s \quad (9)$$

where,

$$C_{p1}=C_{gs1}+C_{gdf} \quad (10)$$

As a result, the input inductor L_S can be choose such that the optimal matching frequency falls around the middle of the operation frequency range of 3.5-7.5 GHz to ensure wideband input matching condition.

2.2. Gain

The conventional CG topology suffer from the low transconductance gain due to its input matching. The CS second stage is intended to increase the gain. Therefore, it is possible to have lower g_m's and consequently a lower power consumption. To derive the bandwidth of the proposed LNA, two dominant parastitic capacitances are considered, as shown in Figure 2.

The parasitic capacitors at the input node v_1 are canceled by L_C resonance, and thus, are not considered. C_{p1} is the parasitic capacitors at the source of M_1 and drain of M_f. C_{p2} is the parasitic effects at the source of M_f, M_3 and drain of M_3 by a factor of $g_{m3}r_{03}$. When using negative feedback, the LNA gain is modified as follows:

$$A_v(s)\approx A_{v1}(s)\times A_{v2}(s) \quad (11)$$

That $A_{v1}(s)$ and $A_{v2}(s)$ are voltage gain of the first floor (including transistor $M_{1,2}$ and M_f) and second floor (including transistor $M_{3,4}$), respectively. Therefore, we have:

$$A_{v1}(s)\approx\frac{A_{v1}\times(1+\frac{L_2}{R_2}s)}{1+\frac{1}{Q_1\times\omega_{01}}s+\frac{1}{\omega_{01}^2}s^2} \quad (12)$$

$$A_{v2}(s)\approx\frac{A_{v2}\times(1+\frac{L_3}{R_3}s)}{1+\frac{1}{Q_2\times\omega_{02}}s+\frac{1}{\omega_{02}^2}s^2} \quad (13)$$

where,

$$A_{v1}=\frac{g_{m1}Z_x}{1+g_{mf}Z_x} \quad (14)$$

$$A_{v2}=g_{m3}Z_y \quad (15)$$

$$\omega_{0,1}=\sqrt{\frac{g_{mf}R_2(1+g_{mf}Z_x)}{L_2C_{p2}}} \quad (16)$$

$$\omega_{0,2} = \sqrt{\frac{R_3+r_{o3}}{L_3 C_{gd3} r_{o3}}} \quad (17)$$

$$Q_1 = \sqrt{\frac{(1+g_{mf}R_2)(1+g_{mf}Z_x)(L_2C_{p2})}{L_2 g_{mf}+C_{p2}R_2}} \quad (18)$$

$$Q_2 = \sqrt{\frac{(R_3+r_{o3})(L_3C_{gd3}r_{o3})}{R_3C_{gd3}r_{o3}+L_3}} \quad (19)$$

and

$$Z_y \approx \left((R_1+JL_3\omega) \| (r_{o3}) \| \frac{1}{J(C_{gd3}+C_{gd5})\omega}\right) \quad (20)$$

R_3 is series parasitic resistance of L_3 at resonance.

2.3. Noise figure

The noise figure of proposed LNA can be expressed with the following equation:

$$F_{total} \frac{2}{A_{vs}^2} \left(\frac{\overline{V_{n,out}^2}}{4kTR_s}\right) \quad (21)$$

Noise of the first floor has the most effect on the noise figure. Thus, noise reduction of the first stage is very important. In proposed LNA, noise of feedback network is also added to the noise of the first stage results in increases in noise figure. On the other hand, noise of the second stage has significant impact on the total noise due to low gain of the first stage.

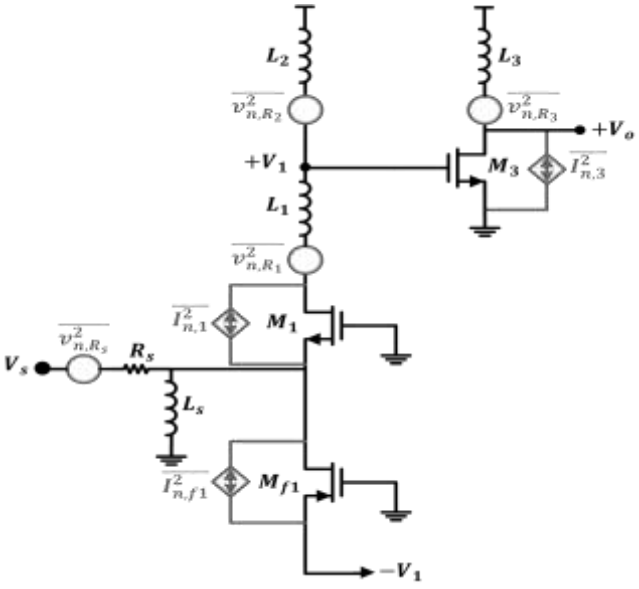

Figure 4. Transistor feedback network with feedback factor of $\beta=g_{mf}$

The noise figure at resonance is determined by inspection of the equivalent circuit of Figure 4. Apart from the noise of output buffer stage due to high gain of LNA, its noise figure is calculated at the resonance frequency as follows:

$$\overline{V_{n,out}^2} = \left(\overline{V_{n,R_s}^2} + \overline{I_{n,f_1}^2} \times \left(\frac{1}{g_{m1}} \square \frac{R_s}{2}\right)^2\right) \times A_{Vs}^2 + \left(\overline{I_{n,1}^2} \times (Z_x^2) + \overline{V_{n,R_1}^2} + \overline{V_{n,R_2}^2}\right) \times A_{V2}^2 + \left(\overline{I_{n,3}^2} \times (Z_y^2) + \overline{V_{n,R_3}^2}\right) \quad (22)$$

In which

$$\overline{I_n^2}=4KT\frac{\gamma}{\alpha}g_m \quad (23)$$

$$\overline{V_{n,R}^2}=4KTR \quad (24)$$

$$A_{V_s}=A_{V1}\times A_{V2}\approx\frac{g_{m1}Z_x}{1+g_{m1}\frac{R_s}{2}}\times g_{m3}Z_y \quad (25)$$

Equation (22) is therefore rewritten as follows:

$$F=2\left(\frac{1}{2}+\frac{R_s\left(\frac{\gamma g_{mf}}{\alpha}\right)}{Z_x^2(2+g_{m1}R_s)^2}+\frac{\gamma g_{m1}R_s}{4\alpha}+\frac{R_s(R_1+R_2)}{4Z_x^2}+\left(\left(\frac{\gamma g_{m3}}{\alpha}+R_3\right)\times\frac{R_s}{4g_{m3}^2Z_x^2Z_y^2}\right)\right) \quad (26)$$

where γ is the MOS transistor thermal noise coefficient. As shown in (26), increasing g_{mf} enhances the noise contributed by the feedback network. However, the reduction of g_{mf} will affect the matching of input impedance and gain. Thus, is calculated based on the trade-off between noise figure and input impedance matching.

3. Simulation Results and Discussion

The proposed circuit has been designed in CMOS 0.18 μm technology and has been simulated using ADS software and model of TSMC Company. The device values of the simulated LNAs and the bias current of transistors are summarized in Table 1.

Table 1. Comparison of Low-Noise Amplifier

Parameter	Proposed LNA W/L		I_D(mA)
$M_{1,2}$	42×3.8μm/0.18μm		2.8
$M_{f1,f2}$	10×1.5μm/0.18μm		0.1
$M_{3,4}$	10×6μm/0.18μm		1.6
$M_{5,6}$	14×4μm/0.18μm`		1
$M_{7,8}$	20×3.5μm/0.18μm		1
L_s	8nH	C_i	3.6pf
L_1	7.5nH	C_O	2.8pf
L_2	6nH	R_B	10KΩ
L_3	6nH	$V_{B1,2}$	0.6V

Figure 5 demonstrates the effect of changes in the inductances L_1 and L_2 on the proposed LNA power gain. As shown, increasing the inductance at the output of the first stage causes the capacitance of this node to resonate within the considered frequency range and hence increase the power gain. On the other hand, since excessive increase in the inductance interferes with the uniformity of the gain, the inductances were considered as L_1=7.5 nH and L_2=6 nH in our design.

Figure 6 shows the effect of changes in the inductance L_3 on the proposed LNA power gain. As shown, since the location of pole in the second stage is determined by the inductance L_3, its value was selected so as to produce a uniform gain in a broad bandwidth according to the location of the pole in the first stage.

Figure 7 shows the effect of transistor transconductance of the feedback network on the noise figure (NF) of the proposed LNA. As expressed in the NF relation (26), increasing g_{mf} leads to an increase in the output noise of the first stage, which in turn increases the voltage of the output noise. Hence, in the present design, the g_{mf} value was decreased to a minimum in order to decrease NF and matching an appropriate input. Figure 8 shows the effect of changes in the L_S on the input return losses of the proposd LNA. As shown by the S_{11} diagram,

increasing L_S leads to elimination of the imaginary part of the input impedance and decreases the return losses at the input.

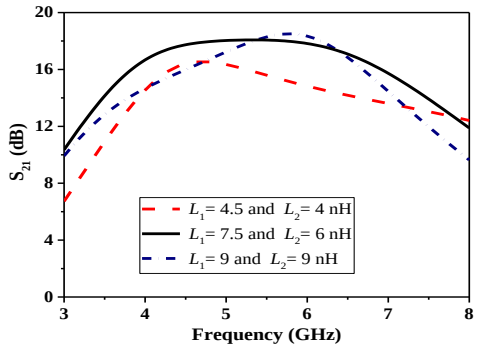

Figure 5. The effect of changes in the inductances L_1 and L_2 on the power gain

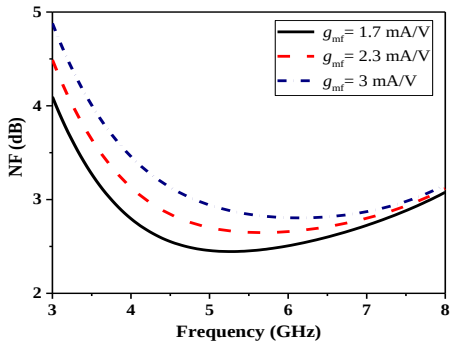

Figure 6. The effect of changes in the inductance L_3 on the power gain

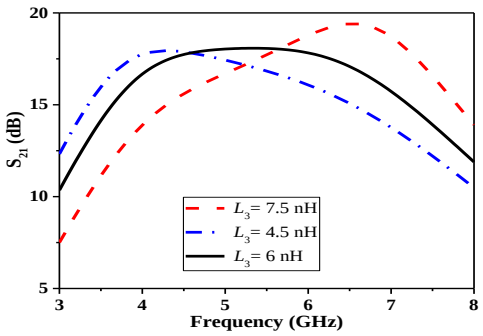

Figure 7. The effect of transistor on NF of the the proposed LNA

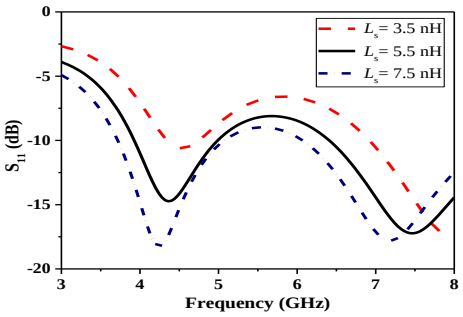

Figure 8. The effect of changes in the L_s on the S_{11} diagram

Figure 9 shows the s-parameters of the proposed LNA. The proposed LNA includes return losses of the input and output of lower than -9 dB and an input-output isolation of lower than -38 dB at a bandwidth of 3.5-7.5 GHz.

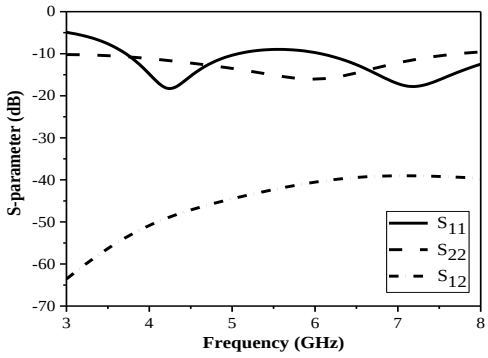

Figure 9. The s-parameters of the proposed LNA

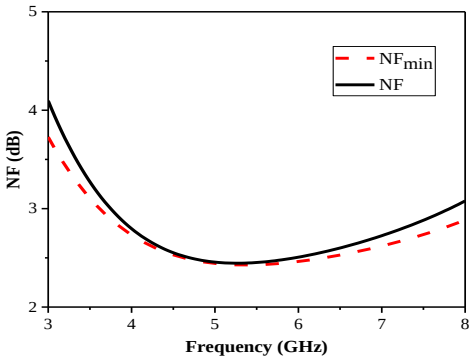

Figure 10. The NF of the proposed LNA

Figure 10 shows the NF of the proposed LNA. The associated NF to this LNA is lower than 3 dB in the frequency range. Also, as shown in Figure 11, power gain is uniform and about 16.5±1.5 dB.

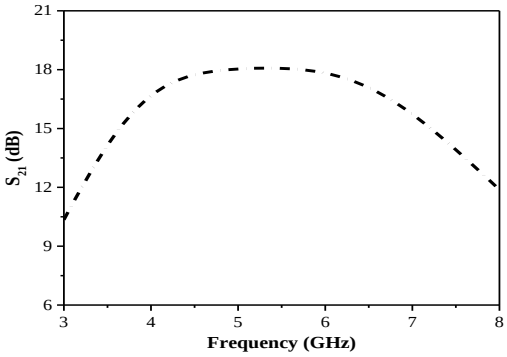

Figure 11. Power gain of proposed LNA

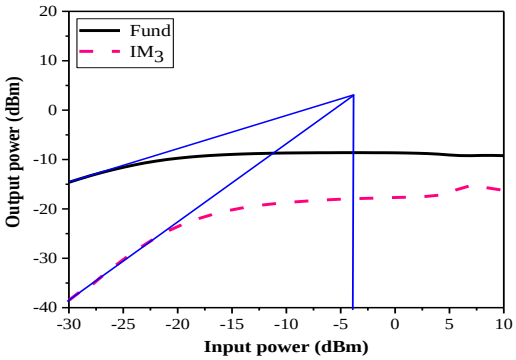

Figure 12. Third-Order Intersection Point of the proposed LNA

Given that ultra- wide band signals have a very low spectral power density, squeezing is rarely considered in Ultra-wideband low-noise amplifiers. But due to wide bandwidth of these system and possible interference signals, the third-order input intersection point (IIP_3) parameter is the most important parameter related to linearity [11]. Two-tone test is done for proposed LNA at the frequency of 5.5 GHz with frequency spacing of 1 MHz. As it can be seen in Figure 12, IIP_3 is equal to -3 dBm.

$$FOM=\frac{|S_{21}|BW_{GH_Z}IIP_{3,mW}}{(|NF|-1)P_{mW}} \quad (27)$$

As it can be observed in Table 2, eligibility criteria of proposed LNA is large which shows its proper functionality for use in ultra-wide band receivers.

Table 2. Comparison of Low-Noise Amplifier

Reference	[12]	[13]	[14]	[15]	[16]	[17]	This Work
Tech. (µm)	0.18 µm	0.18 µm	0.18 µm	0.18µm	0.65 µm	0.18 µm	**0.18 µm**
Structure	Single	Single	Differential	Single	Differential	Differential	Differential
BW**(**GHz**)**	1.05-3.05	3.1-10.6	0.3-0.96	3.1-10.6	0.1-1.6	5-7	**3.5-7.5**
NF (dB)	2.57	6.2	2-3.7	4.4	3.5	3	**2.4-3**
S_{21} (dB)	16.9	13.2	21	9.7	13	7.1	**16.5±1.5**
S_{11} (dB)	-10	-9.5	-10	-10	-8	-10	**-9**
IIP_3 (dBm)	-0.7	-1	-3.2	-8.5	5.5	8	**-3.5**
Power(mW**)**	12.6	28	3.6	11	20.8	6	**9**
FOM	**8.3**	**1.4**	**12**	0.51	**4.12**	**11**	**13**

4. Conclusion

In this paper, a low noise amplifier has been presented using CMOS 0.18 µm technology in ultra-wide band of 3.5-7.5 GHz. A multi-stage differential amplifier has been used in proposed LNA for increasing gain and high linearity. Also, a parallel-parallel negative feedback transistor has been used to increase the bandwidth which can provide a good compromise between power gain and bandwidth while achieving a very low noise figure. In addition to having high linearity and good bandwidth in this method, the use of PMOS and NMOS transistors have led to lack of need of the proposed LNA to biasing circuit and reduction of supply voltage level by 0.8 v which will result in low power consumption in about 9 mW.

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