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Silicon Germanium Heterojunction Bipolar Transistor for Digital Application

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Abstrak

Kinerja transistor bipolar dinyatakan dengan figure of merit, antara lain: frekuensi cut-off, frekuensi osilasi maksimum dan emitter coupled logic gate delay. Pada makalah ini dibahas figure of merit yang tepat untuk aplikasi digital dan pengaruh penskalaan pada arah lateral serta vertikal terhadap figure of merit heterojunction bipolar transistor SiGe. Penskalaan pada arah lateral dilakukan dengan memperkecil lebar lengan emiter pada arah lateral dari 0,25 menjadi 0,12 μm sedangkan penskalaan pada arah vertikal dititikberatkan pada penskalaan lebar basis. Juga dipelajari pengaruh bentuk profil Ge dan fraksi Ge pada basis. Penelitian dilakukan dengan perangkat lunak Bipole3 versi 5.3.1G. Simpulan penting yang dapat diambil antara lain: Heterojunction Bipolar Transsistor SiGe untuk aplikasi digital sebaiknya mempunyai frekuensi cutoff dan frekuensi osilasilasi maksimum yang tinggi serta emitter coupled logic gate delay yang rendah. Penskalaan pada arah lateral dapat meningkatkan frekuensi osilasi maksimum dan emitter coupled logic gate delay secara signifikan sedangkan penskalaan basis pada arah vertikal dapat meningkatkan frekuensi cutoff dan penguatan arus.

Kata kunci: *HBT SiGe, basis SiGe, aplikasi digital*

Abstract

Bipolar transistor performances can be characterized by figures of merit such as cut-off frequency, maximum frequency of oscillation and Emitter Coupled Logic gate delay. We studied the required figures of merit for digital application and the effects of lateral and vertical scaling to the figures of merit of SiGe Heterojunction Bipolar Transistor. With lateral scaling, the width of emitter finger is scaled down from 0.25 to 0.12 μm while with the vertical scaling, the base width is scaled down to reduce the base delay. We also observed the effects of Ge profile and Ge fraction to the devices performances. Bipole3 5.3.1G is used to help us in the study. We found that high frequency cut-off and maximum frequency of oscillation as well as low Emitter Coupled Logic gate delay are all important for digital applications. Scaling down the emitter finger width enhanced the maximum frequency of oscillation and reduced Emitter Coupled Logic gate delay significantly while scaling down the base width increased the cutoff frequency and current gain.

Keywords*: Silicon Germanium, SiGe, HBT, digital application*

1. Introduction

The consumer demand for data from the internet, for digital audio and video is increasing rapidly [1]. According to Cisco Visual Networking Index (VNI) 2009 – 2014, the global internet traffic will increase more than fourfold to 767 exabytes or 767 million gigabytes or 2.1 million gigabytes daily by 2014. The traffic is dominated by video, exceeding 91% of global traffic as a result from improvements in network bandwidth capacity and internet speed along with the increasing popularity of High-Definition Television [2]. To support this growth of internet traffic, faster data transmission rate is needed.

Telecommunication systems operated at 10 Gbps were quickly reaching capacity and to meet immediate trafic growth, the 40 Gbps systems have been developed and dominated telecommunication systems for the last two years. Now, data growth requires deployment of higher capacity and higher data rate (100 Gbps) systems [3-4]. To achieve such high data rate, higher speed semiconductor devices are required. Target Heterojunction Bipolar Transistor (HBT) specification for 160 Gbps systems include cut-off frequency f_T and maximum frequency of oscillation f_{max} higher than 440 GHz [5]. Therefore, SiGe HBT is the major candidate for the

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needs of this new telecommunication system. In research lab, it was possible to realize SiGe HBTs with f_T up to 375 GHz [6] and f_{max} up to 350 GHz [7], which is comparable to III-V technologies [8]. While SiGe HBT has been used as low power high speed devices, Insulated Gate Bipolar Transistors (IGBTs) could be used as medium and high power application [9].

Bipolar transistor performances can be characterized by figures of merit such as f_T, f_{max} and Emitter Coupled Logic (ECL) gate delay. However, the relevance or significance of a particular figure of merit depends on the application [10]. In designing high speed analog application, additional figure of merit such as current gain β, early voltage V_A and noise figure NF are the special concerns [11]. However, there are different opinions about which figures of merit are more important in designing digital application. In this paper, we report the design of SiGe HBT specific for digital application using Bipole3 device simulation software.

2. Research Method

We first study figures of merit of a bipolar transistor from published paper and book [10, 12 – 18], and then determines which particular figures of merit are important for digital applications design. Next, we define a reference device, which is basically a two base contacts SiGe HBT with emitter finger area A_E 0.25x8 μm^2 as shown in Figure 1.

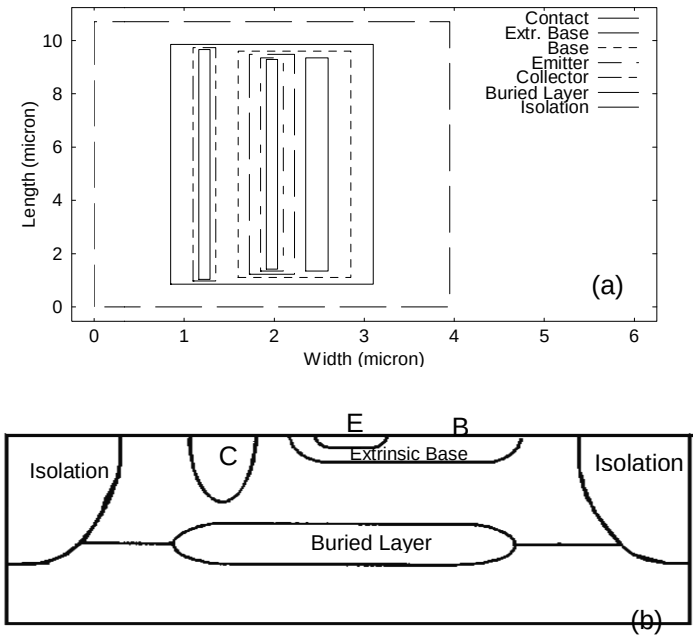

Figure 1. Schematic of (a) lateral structure and (b) vertical cross section of the reference devices

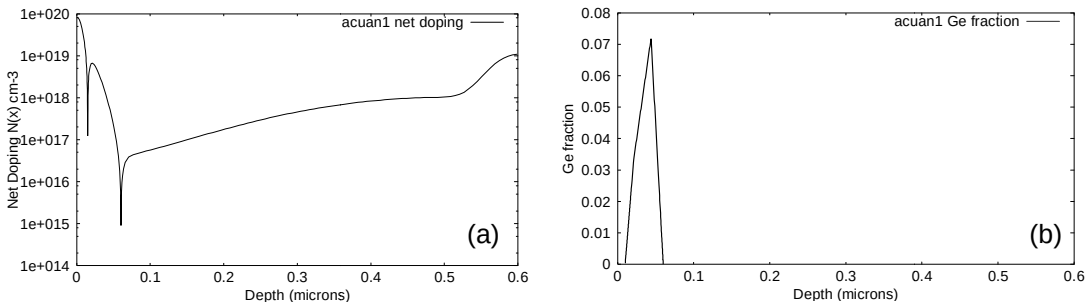

Figure 2. (a) Vertical doping and (b) Ge profile of the reference devices

In the vertical direction, the reference device has 15 nm emitter widths with 10^{20} cm^{-3} peak doping concentration, 45 nm base width with $1.7x10^{19}$ cm^{-3} peak doping concentration and about 440 nm collector width with selected implanted collector (SIC) profile. The Ge profile in the base has trapezoid shape with 0.077 Ge fractions as shown in Figure 2. The reference device has 67 GHz peak f_T, 65 GHz peak f_{MAX}, 15 ps ECL gate delay, 3.6 Volt collector-emitter breakdown voltages (BV_{CEO}) and about 120 peak dc current gain (β_{DC}). The reference device is then scaled down laterally and vertically, and the scaling effects to the certain figures of merit are observed.

3. Results and Discussions

3.1. Figures of Merit

Researchers have different opinions in what particular figures of merit are required for digital application as shown below. According to Cressler, the f_T and f_{max} cannot directly predict the performance of large-signal circuits, such as digital circuits, ECL ring oscillator speed or frequency divider data are more direct and accurate measure of digital switching speed [10]. For digital applications, a transistor is designed to function as a switch. One of the most important parameters for switching transistors is the minority carrier life time [12]. To increase the switching speed, one must increase the cutoff frequency [13, 14].

As SiGe HBTs are typically structured as a vertical device, their speed performance is mostly determined by the vertical transport of the carriers [15]. The common trend in HBT technology development is to achieve a device with balance f_T and f_{max}. However, improvement in f_T trades off and limits f_{max} of device [16]. Heterojunction bipolar transistor's higher intrinsic f_{max} value, lower base resistance and lower substrate capacitance will permit higher speed for digital applications [17]. To achieve high switching speeds, it is not sufficient to just reduce the HBT's dimensions, but the transistors parasitics like the base resistance or the collector-base capacitance must also be minimized [18]. For a digital circuit, the gate delay itself is often used as a figure of merit for the transistors in the circuit [10].

Based on the opinions stated above, we separate the parameters into input parameters and output parameters of the SiGe HBT design. The input parameters such as minority carrier life time, base resistance, substrate capacitance, device dimensions, collector-base capacitance can be controlled by adjusting the doping profiles and densities as well as device dimension in the vertical and lateral dimension. The output parameters such as the f_T, f_{max} and ECL gate delay are the figures of merit that we need to observed and optimized.

3.2. Lateral Scaling

The emitter finger width (in the lateral direction) of the reference device is scaled down from 0.25 μm to 0.18 μm and 0.12 μm, while maintaining the emitter area at $2\mu m^2$, other lateral and vertical dimensions are preserved. We used Bipole3 automated mask option which only need the definition of emitter finger area as an input parameter. The other lateral dimensions are calculated automatically by Bipole3 and the detail of the device dimension can be observed at the output file.

The simulation results show that all SiGe HBTs have 3.6 Volt emitter-collector breakdown voltages BV_{CEO}. The effects of lateral scaling to the SiGe HBTs f_T and f_{max} at collector-base voltage V_{CB} 1V are shown in Figure 3, for the ECL gate delay are shown in Figure 4, and the value of peak f_T, f_{max} and β_{dc} and the minimum ECL gate delays are presented in Table 1.

From Figure 3, Figure 4 and Table 1, we know that scaling down the emitter finger width enhance the maximum oscillation frequencies, lower the current gains and ECL gate delay, while the cut-off frequencies are stable at around 68 GHz. Scaling down the emitter finger width from 0.25 μm to 0.18 μm yields 24 GHz higher f_{max} and from 0.18 μm to 0.12 μm gives us another 37 GHz enhancement. Further observation shows that SiGe HBT with narrower emitter finger has smaller base resistance and according to Eq. (1), smaller base resistance yields higher f_{max}. Our results are consistent with previous research by Zhang et.al. [19].

$$f_{\max} = \left(\frac{f_t}{8\pi R_b C_{bc}} \right)^{1/2} \quad (1)$$

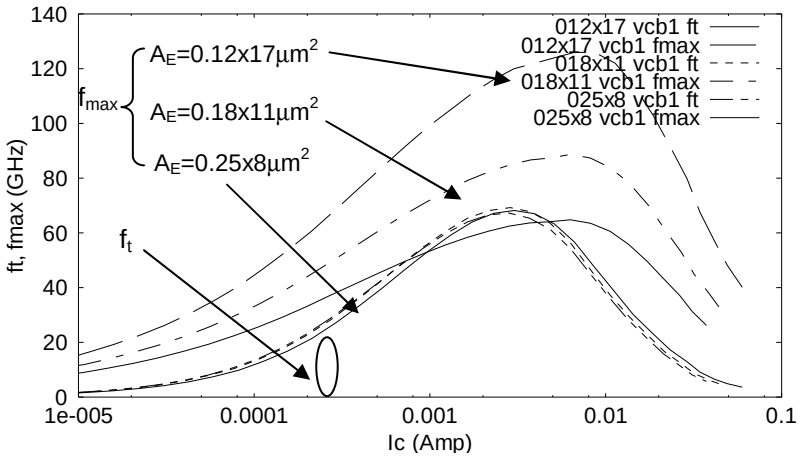

Figure 3. The f_t and f_{max} curve of SiGe HBTs with emitter area A_E 0.25x8, 0.18x11 and 0.12x17μm^2 at V_{CB}=1V

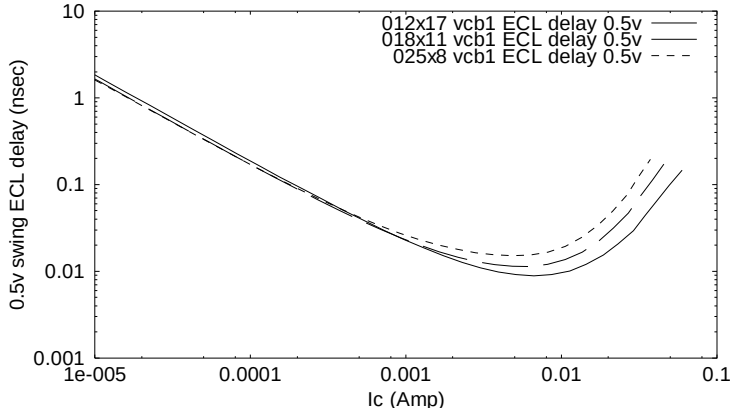

Figure 4. The ECL gate delays of SiGe HBTs with emitter area A_E 0.25x8, 0.18x11 and 0.12x17μm^2.

Table 1 The effects of A_E to the SiGe HBT figure of merit.

A_E (μm^2)	Peak f_T (GHz)	Peak f_{max} (GHz)	Peak β_{dc}	Min. ECL gate delay (ps) (swing 0.5V)
0.25 x 8	67	65	130	15
0.18 x 11	69	89	114	11
0.12 x 17	68	126	98	9.8

Table 2 The effects of base width to SiGe HBT figure of merit (V_{CB}=1V)

W_B (nm)	Peak f_t (GHz)	Peak f_{max} (GHz)	Peak β_{dc}	Min ECL gate delay (ps) (swing 0.5V)
45 (0.25 x 8μm^2)	67	65	130	15
36 (0.25 x 8μm^2)	72	64	159	15
30 (0.25 x 8μm^2)	77	68	188	15

3.3. Vertical Scaling

In this section, we focused the study on the base design including Ge profile design because the base and collector-base space charge layer delays are higher compared to the

other delays at high current. The base width is scaled down from 45 nm to 36 nm and then to 30 nm. The effects of base width to the SiGe HBT figures of merit are shown in Table 2. Scaling down the base width from 45 to 30 nm enhances the peak f_T of SiGe HBT around 15% from 67 to 77 GHz. Reduction in vertical delay is the main contributor to enhance the f_T of SiGe HBTs with narrower base width. Base width scaling also has the same effects to the β_{dc} with enhancement in current gain about 45%. Table 2 also shows that scaling down the base width has stronger effects to the f_T and β_{dc} but weaker to the f_{max} and ECL gate delay.

Besides the flat shape Ge profile with 0.077 and 0.144 Ge mole fraction, the trapezoid shape Ge with 0.077 and 0.144 peak Ge mole fraction in the base are also observed. The Ge profiles in the base are shown in Figure 5. The effects of Ge profile in the base of SiGe HBT to the device performances are summarized in Table 3.

For both Ge profiles, higher Ge mole fraction yields lower peak f_T and f_{max}. Our results show that SiGe HBTs with trapezoid Ge profiles have higher cutoff frequencies and higher maximum frequencies of oscillation, but lower current gain compared to SiGe HBT with flat Ge profiles ,which is consistent with previous research [20, 21], which used trapezoid Ge profil for optimum SiGe HBT performance. The simulation results show that base width scaling, Ge profiles and Ge mole fraction have no significant effect to the ECL gate delay.

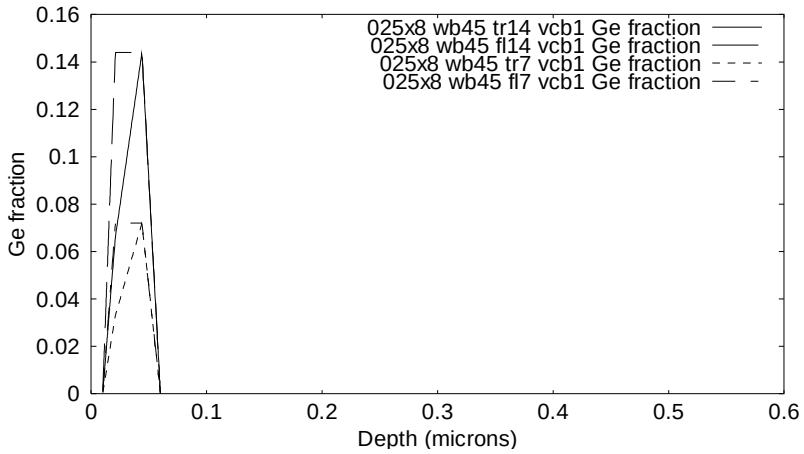

Figure 5. Ge profiles in the base of SiGe HBTs
(base width 45nm and A_E=0.25x8μm^2)

Table 3 The effects of Ge profiles and mole fraction to the SiGe HBT performance

Ge profiles	Peak f_t (GHz)	Peak f_{max} (GHz)	Peak β_{dc}	Min ECL gate delay (ps) (swing 0.5V)
Trapezoid 0.077	67	65	130	15
Trapezoid 0.144	61	61	292	16
Flat 0.077	64	63	226	16
Flat 0.144	60	61	720	16

4. Conclusion

Scaling down the emitter finger width in the lateral direction enhance the maximum frequency of oscillation due to smaller base resistance and reduce the ECL gate delay. However, it also decreases the current gain while the cut-off frequencies are steady. Scaling down the base width enhance the cutoff frequency of SiGe HBT due to reduction in vertical delay. Base width scaling also enhances the current gain. Base width scaling has stronger effects to the f_T and β_{dc} but weaker to the f_{max} and ECL gate delay. SiGe HBTs with trapezoid Ge profiles have higher cutoff frequencies and higher maximum frequencies of oscillation but lower current gain compared to SiGe HBT with flat Ge profiles. Base width scaling, Ge profiles and Ge fraction have no significant effect to the ECL gate delay.

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