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A Low Cost C8051F006 SoC-Based Quasi-Static C-V Meter for Characterizing Semiconductor Devices

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Abstrak

Berbasiskan SoC (system on-a-chip) C8051F006, pengukur kapasitansi-tegangan (CV) kuasi-statis berbiaya rendah dirancang dan dikembangkan untuk memperoleh karakteristik C-V perangkat semikonduktor. Pengukur C-V terdiri dari pengukur kapasitansi, sumber tegangan yang dapat program, slave-controller berbasis SoC C8051F006, dan komputer pribadi (PC) sebagai master controller. Komunikasi antara master dan slave-controller dilakukan melalui komunikasi serial RS 232. Keakuratan pengukur C-V dijamin oleh fungsi kalibrasi yang dikerjakan oleh program di PC dan diperoleh melalui proses kalibrasi konversi analog ke digital (ADC), konversi digital ke analog (DAC) pada SoC C8051F006, dan sumber tegangan yang dapat diprogram. Percobaan telah dilakukan pada kapasitor 33-pF dan 1000-pF serta tiga diode p-n didapatkan bahwa nilai kapasitor berada dalam rentang nilai tertentu dan diperoleh kurva C-V untuk dioda p-n.

Kata Kunci: *ADC, kuasi-statis, DAC, pengukur C-V, pengukur kapasitansi, SoC*

Abstract

Based on a C8051F006 SoC (system on-a-chip), a simple and low cost quasi-static capacitance-voltage (C-V) meter was designed and developed to obtain C-V characteristics of semiconductor devices. The developed C-V meter consists of a capacitance meter, a programmable voltage source, a C8051F006 SoC-based slave controller, and a personal computer (PC) as a master controller. The communication between the master and slave controllers is facilitated by the RS 232 serial communication. The accuracy of the C-V meter was guaranteed by the calibration functions, which are employed by the program in the PC and obtained through the calibration processes of analog to digital converter (ADC), digital to analog converters (DACs) of the C8051F006 SoC, and the programmable voltage source. Examining 33-pF and 1000-pF capacitors as well three different p-n junction diodes, it was found that the capacitances of common capacitors are in the range of specified values and typical C-V curves of p-n junction diodes are achieved.

Keywords: *ADC, capacitance meter, C-V meter, DAC, quasi-static, SoC*

1. Introduction

Capacitances of semiconductor devices are relatively easily measured, and are usually associated with relevant physical parameters. From determining the capacitances, a number of characterization techniques have been developed to assess the geometry of devices, component materials and interfaces. Various methods called as capacitive measurements are available and frequently in the form of capacitance-voltage (C-V) characteristics, such as: phase-sensitive detection, time-encoded ballistic, resonance, and AC bridge methods [1-6].

C-V curves are generally obtained by using an AC measurement technique in which semiconductor devices are usually biased at increasing voltages in a stepped sequence and superimposing a small ac voltage with the frequency in the range of 1 kHz to 10 MHz [6]. The AC measurement technique is also termed as high-frequency (HF) C-V measurement. On the other hand, there is a DC measurement technique, which is required by some capacitive

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measurement applications. This technique is called quasi-static C-V or low frequency (LF) C-V measurements because they are performed at a very low frequency, that is, almost DC. These measurements usually involve stepping a DC voltage and measuring the resulting current or charge [6].

Compared to the HF C-V measurements, the intrinsic advantages of the quasi-static C-V ones lie in the convenience of the data acquisition and the simplicity of circuits [7]. Although the circuits are simple, there are only few papers describing the development of quasi-static C-V meters [8-10]. Unfortunately, microcontrollers were not employed to control the quasi-static C-V meters.

In this paper, we report the development of a quasi-static C-V meter based on the Silicon Laboratories C8051F006 SoC (system on-a-chip). After calibrating the developed C-V meter, the C-V meter is employed to characterize semiconductor devices such as capacitors and diodes. The capacitance–voltage (C–V) curves obtained by the C-V meter are analyzed and discussed.

2. Design and Method

Figure 1 demonstrates the block diagram of a quasi-static C-V meter, which is composed of a capacitance meter, a programmable voltage source that generates a DC bias voltage and a voltage step, a C8051F006 SoC acts as a slave controller, and a personal computer (PC) functions as a master controller. The communication between the master and slave controllers is provided by RS 232 serial communication. The output of voltage source is fed to the device under test (DUT) and its capacitance is measured by the capacitance meter.

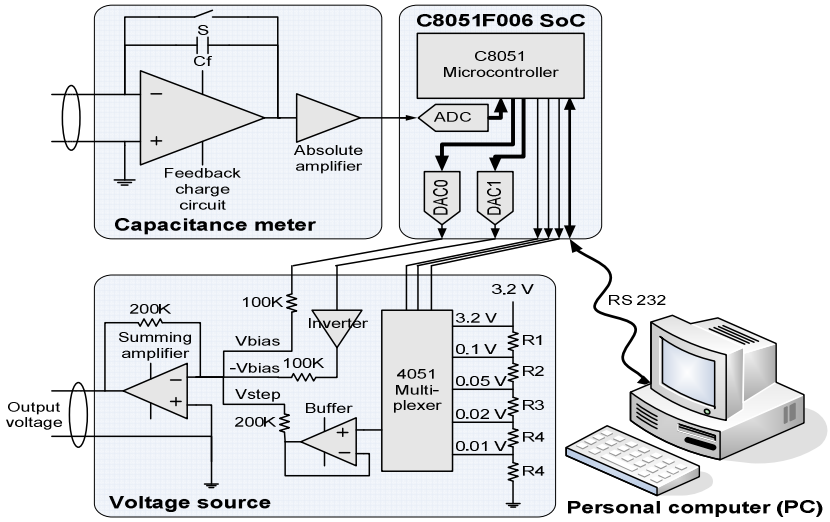


Figure 1. Block diagram of a C-V meter based on C8051F006 SoC

As explicitly shown by its name, the C8051F006 SoC provides enormous features [11]. The important subsystems utilized by the quasi-static C-V meter are two 12-bit digital to analog converters (DACs), i.e., DAC0 and DAC1, a 12-bit analog to digital converter (ADC), and an 8051 family microcontroller. As a slave controller, the C8051F006 SoC controls directly and communicates to the capacitance meter and the voltage source. Through the slave controller, pairs of applied voltages and measured capacitances are saved in the PC for further processing.

The capacitance meter uses a feedback charge method and utilizes a quasi-static measurement method to measure a capacitance. The advantages of employing the feedback charge method are higher signal to noise ratio at frequencies of interest, the independence of signal size from measurement time, and the ease of distinction of signal charge from error currents at the time of measurement [12]. Since the DC bias voltage supplied to the DUT can be

negative, which is in contrast to the input voltage of an ADC of the C8051F006 SoC, an absolute amplifier is required. The quasi static measurement method applies a small voltage step across the DUT and a displacement charge is therefore stimulated and measured.

The voltage source supplies a DC voltage fulfilling the requirements of the quasi static measurement method. A DC bias voltage can be positive or negative, V_{bias} or $-V_{bias}$, respectively. The DC bias voltages are generated by the outputs of DACs of the C8051F006 SoC. The positive bias is directly delivered by DAC0. As the output of the DAC is positive, the negative bias is achieved by employing DAC1 and an inverter amplifier. A small voltage step ranging from 100 mV to 3.2 V is produced by resistor ladders along with a precision voltage supply, a 4051 multiplexer, and a buffer amplifier. The selection of voltage step is performed by the C8051 microcontroller of the C8051F006 SoC. Making use of a summing amplifier, the output of the voltage source is a small voltage step (V_{step}) superimposing a DC bias voltage that can be positive or negative, V_{bias} or $-V_{bias}$, respectively.

A circuit diagram of the feedback charge method is given in Figure 2. It is an integrator circuit with a feedback capacitor C_f, a switch S, and a capacitance to be measured C_x. Before performing measurement, the feedback capacitor C_f is discharged by closing the switch S. When the measurement is ready, S is opened to charge C_f. As a result, there is a charge ΔQ, which is supplied by the bias voltage, transferred to C_x of the integrator. This charge results in a change of the integrator output, which is given by

$$\Delta V_{out} = -\Delta Q / C_f \cdot \tag{1}$$

Applying the quasi static measurement method, the voltage source is changed by a small amount dV (a voltage step). This voltage step produces a displacement charge dQ to be transferred to the DUT (C_x). The displacement charge in C_x is proportional to the voltage change and is given as $dQ= C_x dV$. The charge in the feedback capacitor C_f is determined by measuring the integrator output before and after the application of the voltage step and is written as

$$\Delta dQ = -C_f \Delta V_{out} \cdot \tag{2}$$

The unknown capacitance C_x of the DUT is therefore given as

$$C_x = \Delta Q / \Delta V = -C_f \Delta V_{out} / \Delta V \cdot \tag{3}$$

The way of measuring the capacitance C_x of the DUT is described as follows. The voltage waveform fed to the DUT by the voltage source at a bias voltage is shown in Figure 3(a). A DC bias voltage (V_{bias1}) is applied during the time of t_{step}. A voltage step (V_{step}) is then given during the next t_{step}. Because of the action of integrator, the charge waveform is given in Figure 3(b). Charge measurements are made at three specific times, which are represented by Q_1, Q_2, and Q_3. Q_1 is the baseline charge, which is measured prior to the voltage step by t_1. Q_3 is measured after specified delay time t_{delay}, where $t_{step} = t_{delay} + t_1$, and is an indication of the final charge transferred to C_x. Q_2 is measured before Q_3 by t_0. Q_2 is used to determine the slope of charge waveform. This slope indicates the amount of current Q/t flowing in C_x during the final portion of t_0. Q/t represents the leakage in C_x and corrected capacitance is calculated as follows:

$$C_x = (Q_2 - Q_1)/V_{step} ,$$

$$Q/t = (Q_2 - Q_1)/t_0 ,$$

$$C_{x,corrected} = C_x - \frac{(Q/t)(t_{delay} + t_1)}{V_{step}} . \tag{4}$$

A flowchart of measuring capacitance is described in Figure 4. The PC feeds a bias voltage, a voltage step, and a time delay to the microcontroller of the C8051F006 SoC. Before

doing measurement, C_f is discharged. As the measurement is ready, V_{bias} is applied to $C_x$for a given delay time. The output voltage of capacitance meter is read by the ADC and sent to the PC via the RS-232 serial communication.

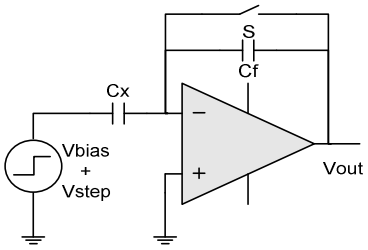


Figure 2. Feedback charge circuit

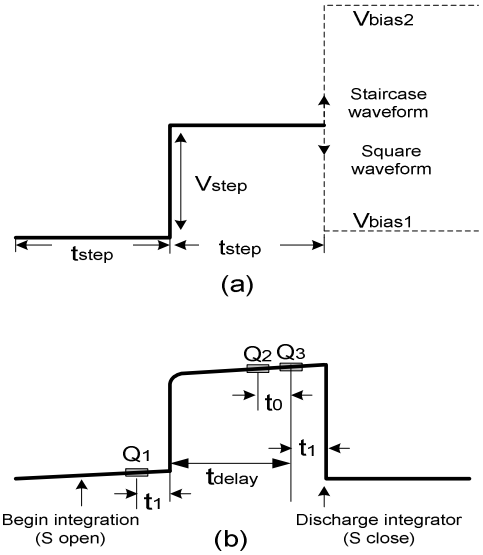


Figure 3. (a) Input voltage waveform and (b) measured charge waveform of the feedback charge circuit [9]

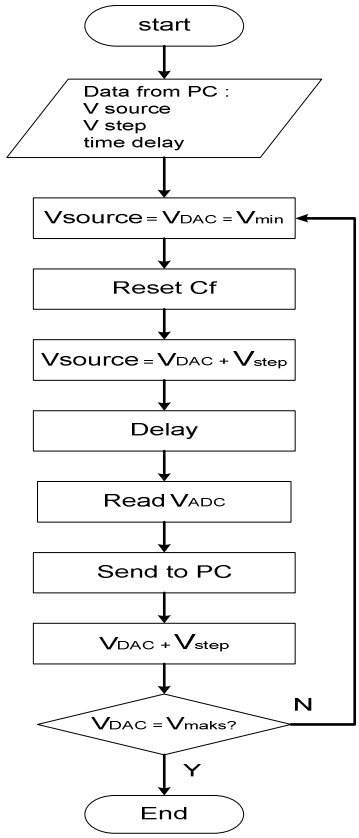


Figure 4. Flowchart of capacitance measurement to obtain a C-V curve

3. Examination Results and Discussion

In order to ensure the accuracy of measurements, the developed C-V meter was calibrated as illustrated in Figure 5. The calibration of the ADC of C8051F006 SoC was first done as given in Figure 5(a). A precision voltage source supplied a voltage, which was also read by the Fluke 45 voltmeter, to the ADC. Connecting the C8051F006 SoC to the PC by the RS 232 serial communication, the output of ADC was saved into the PC. The voltages measured by the voltmeter were compared to those saved in the PC to obtain a calibration function for the ADC. Figure 5(b) shows the calibration of DACs with the voltage source. The PC sent digital data, which represent certain voltages, to the DAC and the Fluke 45 voltmeter measured the output of the voltage source. The voltages provided by the PC were compared to those measured by the voltmeter to get a calibration function for the DAC and the voltage source.

Figure 6 shows a transfer function, which is the relationship between an input and an output, of the ADC. Here, the 12-bit digital output of the ADC is given as decimal numbers. Symbols are measured values and the straight line is a fitting function to the data. It is shown that the straight line is represented by $y(x)= (5.98\times10^{-4})x$, where y is the input voltage and x is the digital output voltage. The equation is a calibration function of the ADC and it will be used by the program in the PC.

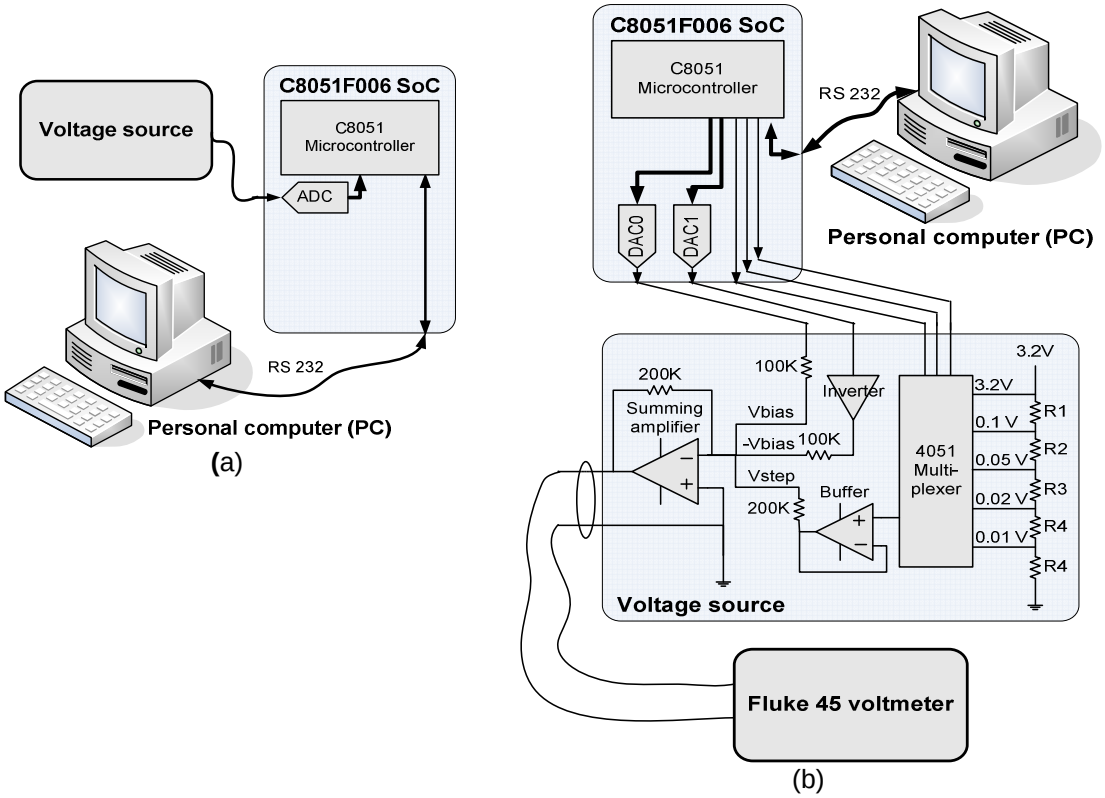


Figure 5. Calibrations of (a) an ADC and (b) DACs along with a voltage source

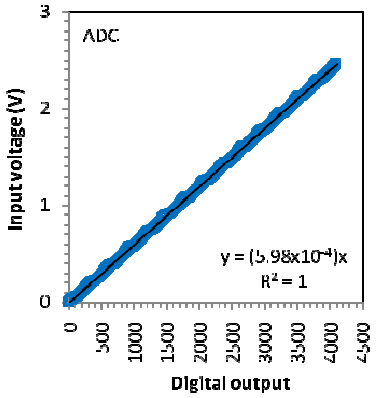


Figure 6. A transfer function of the ADC

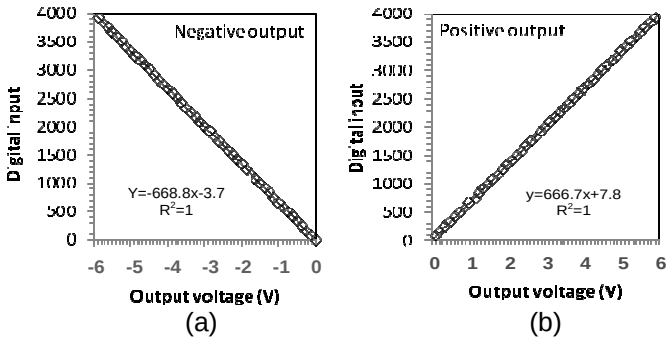
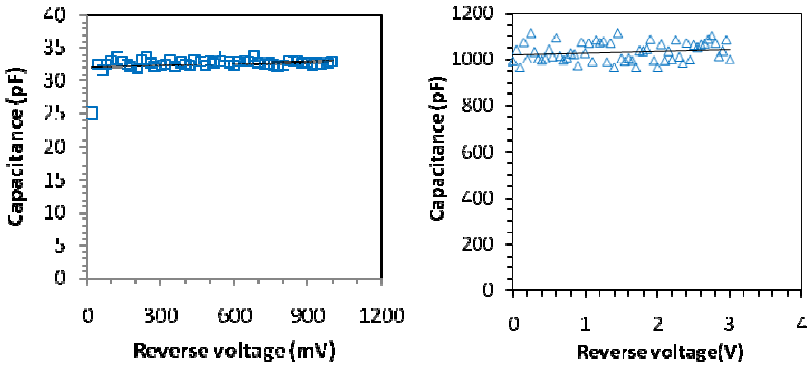


Figure 7. Transfer functions of the DACs with the voltage source. (a) Negative output and (b) Positive output

Transfer functions of the DACs with the voltage source are shown in Figure 7. The 12-bit digital input of the DAC is presented as decimal numbers. Symbols are measured values and the straight lines are fitting functions to the data. The straight lines act as calibration functions of the DACs with the voltage source that will be employed by the program in the PC. In addition, it is found that the calibration functions are y(x)= -668.8x-3.7 and y(x)= 666.7x+7.8 for negative and positive outputs, respectively, where y is the digital input voltage and x is the output voltage.

The developed quasi-static C-V meter was examined to obtain C-V characteristics of semiconductor devices. The devices were 33- and 1000-pF capacitors as well as three different diodes. Applying the voltage step of 20 mV and the delay time of 500 ms to 33- and 1000-pF

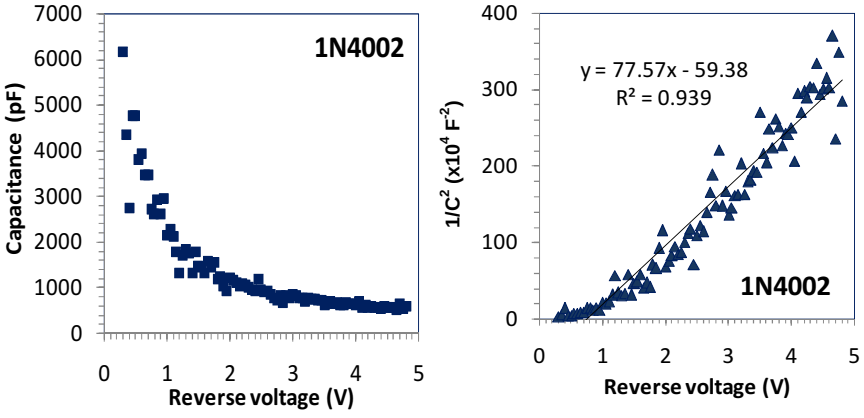
capacitors, the C-V curves are found as given in Figures8(a) and 8(b). Since these are common capacitors, their capacitances are independent of bias voltages. The measured results confirmed the characteristics. The obtained variations are related to the precision of the repeated measurements. However, the measured values are within the range of specified capacitances.



(a) (b)

Figure 8.C-V characteristics of capacitors of (a) (33± 5%) pF and (b) (1000± 15%) pF

The C-V characteristic of 1N4002 general rectifier diode with reverse bias voltages is demonstrated in Figure 9(a). The curve was obtained by employing the voltage step of 10 mV and the time delay of 1000 ms. The datasheet gives the diode capacitance of 15 pF at a frequency of 1 MHz and a reverse voltage of 4 V [13]. On the other hand, the diode capacitance measured at very low frequency is about 600 pF. It seems that the diode capacitance depends on operating frequency and the increase in operating frequency would decrease the diode capacitance. Plotting $1/C^2$ versus voltage, it is shown in Figure 9(b) that the plot can be represented by a straight line. This result implies that the diode has an abrupt junction [14].



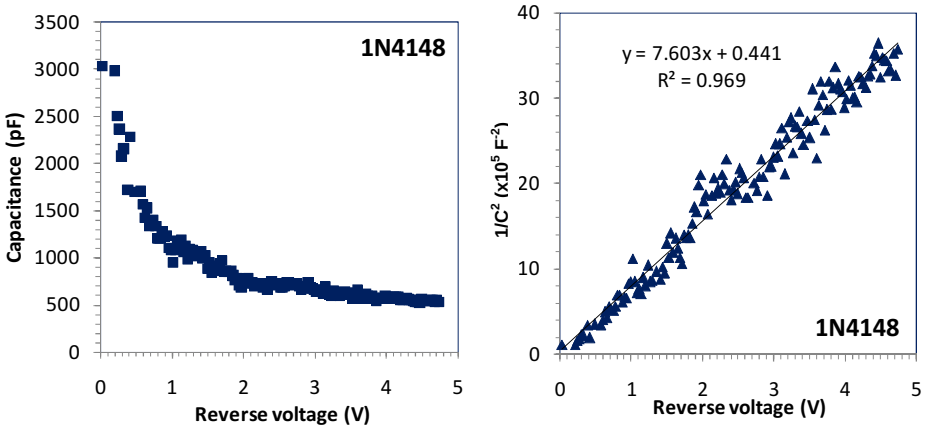
(a) (b)

Figure 9.1N4002 rectifier diode in reverse bias with V_{step}= 10 mV and t_{delay}= 1000 ms. (a)C-V characteristic, (b) $1/C^2$vs V plot

A 1N4148 high-speed switching diode has a C-V characteristic under reverse bias voltages as depicted in Figure 10(a). A voltage step of 10 mV and the time delay of 1000 ms were used to achieve the curve. In contrast to the datasheet giving the diode capacitance of about 0.8 pF at a frequency of 1 MHz and a reverse voltage of 4 V [15], the diode capacitance obtained at very low frequency is about 500 pF. Again, it looks that the increase in operating

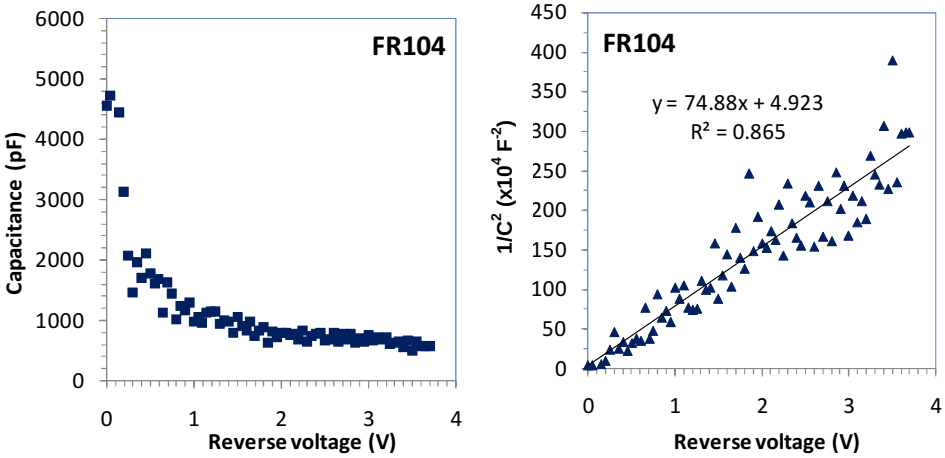
frequency would decrease the diode capacitance. Figure 10(b) gives a plot of $1/C^2$ versus voltage as a straight line. It means that the diode has also an abrupt junction.

Figure 11(a) shows a C-V characteristic of an FR104 fast recovery diode under reverse bias voltages. The curve was obtained by employing a voltage step of 10 mV and the time delay of 400 ms. The datasheet provides the diode capacitance of 15 pF at a frequency of 1 MHz and a reverse voltage of 4 V [16]. On the contrary, it is found that diode capacitance obtained at very low frequency is about 600 pF. Once more, it appears that the increase in operating frequency would decrease the diode capacitance. A straight line of $1/C^2$ versus voltage in Figure 11(b) indicates that the diode has also an abrupt junction.



(a) (b)

Figure 10.1N4148 rectifier diode in reverse bias with V_{step}= 10 mV and t_{delay}= 1000 ms. (a)C-V characteristic, (b) $1/C^2$vs V plot



(a) (b)

Figure 11.FR104 fast recovery diode in reverse bias with V_{step}= 10 mV and t_{delay}= 400 ms. (a)C-V characteristic, (b) $1/C^2$vs V plot

4. Conclusion

We have built a simple and low cost quasi-static C-V meter based on a C8051F006 SoC to characterize semiconductor devices. The C-V meter is composed of a capacitance meter, a programmable dc voltage source, a C8051F006 SoC-based slave controller and a personal computer as a master controller. The C-V meter has been calibrated to obtain calibration functions, which are used by the program in the master controller. It has been shown that capacitances of 33- and 1000-pF capacitors are constants independent of bias voltages and

their values agree with the indicated values. Moreover, typical C-V curves of p-n junction diodes have also obtained.

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